

Transistors

4V Drive Nch MOS FET

2SK2503

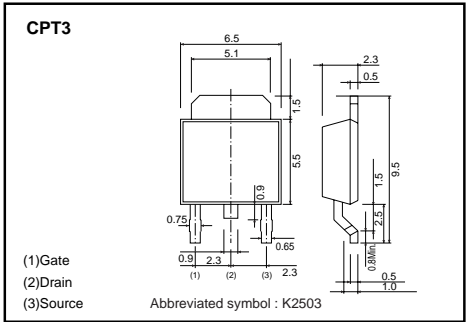
●Structure

Silicon N-channel MOS FET

●Features

- 1) Low On-resistance.
- 2) Fast switching speed.
- 3) Wide SOA (safe operating area).
- 4) 4V drive.
- 5) Drive circuits can be simple.
- 6) Parallel use is easy.

●External dimensions (Unit : mm)



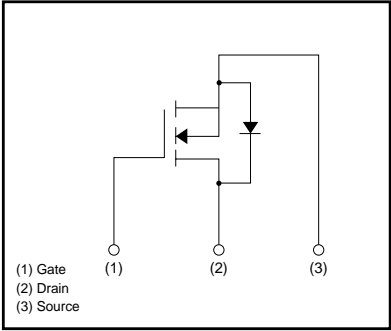
●Applications

Switching

●Packaging specifications

Type	Package	Taping
	Code	TL
	Basic ordering unit (pieces)	2500
2SK2503		○

●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-source voltage	V _{DSS}	60	V
Gate-source voltage	V _{GSS}	±20	V
Drain current	Continuous	I _D	5 A
	Pulsed	I _{DP} *	20 A
Reverse drain current	Continuous	I _{DR}	5 A
	Pulsed	I _{DRP} *	20 A
Total power dissipation(Tc=25°C)	P _D	20	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

* Pw ≤ 10μs, Duty cycle ≤ 1%

Transistors

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-source leakage	I _{GSS}	–	–	±100	nA	V _{GS} = ±20V, V _{DS} =0V
Drain-source breakdown voltage	V _{(BR)DSS}	60	–	–	V	I _D =1mA, V _{GS} =0V
Zero gate voltage drain current	I _{DSS}	–	–	10	μA	V _{DS} =60V, V _{GS} =0V
Gate threshold voltage	V _{GS(th)}	1.0	–	2.5	V	V _{DS} =10V, I _D =1mA
Static drain-source on-state resistance	R _{DS(on)}	–	0.11	0.135	Ω	I _D =2.5A, V _{GS} =10V
		–	0.17	0.20		I _D =2.5A, V _{GS} =4V
Forward transfer admittance	Y _{fs} *	4.0	–	–	S	I _D =2.5A, V _{DS} =10V
Input capacitance	C _{iss}	–	520	–	pF	V _{DS} =10V
Output capacitance	C _{oss}	–	240	–	pF	V _{GS} =0V
Reverse transfer capacitance	C _{rss}	–	100	–	pF	f=1MHz
Turn-on delay time	t _{d(on)}	–	5.0	–	ns	I _D =2.5A, V _{DD} =30V
Rise time	t _r	–	20	–	ns	V _{GS} =10V
Turn-off delay time	t _{d(off)}	–	50	–	ns	R _L =12Ω
Fall time	t _f	–	20	–	ns	R _G =10Ω

* P_w ≤ 300μs, Duty cycle ≤ 1%

Transistors

●Electrical characteristics curve

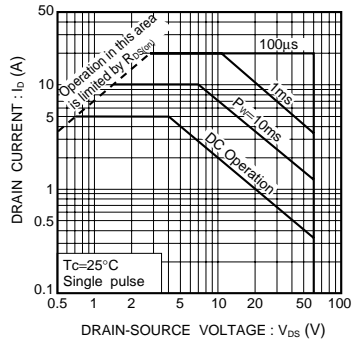


Fig.1 Maximum Safe Operating Area

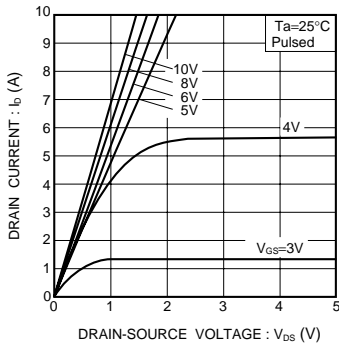


Fig.2 Typical Output Characteristics

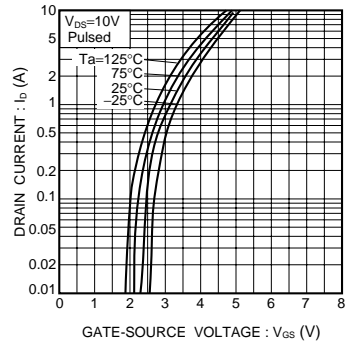


Fig.3 Typical Transfer Characteristics

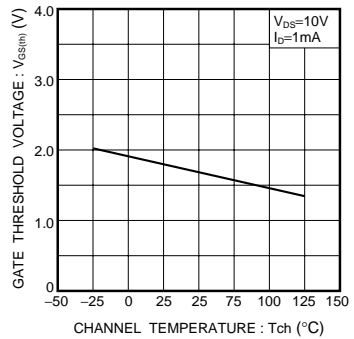


Fig.4 Gate Threshold Voltage vs. Channel Temperature

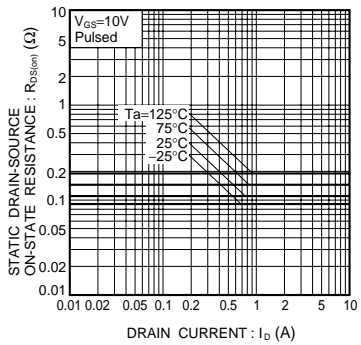


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (I)

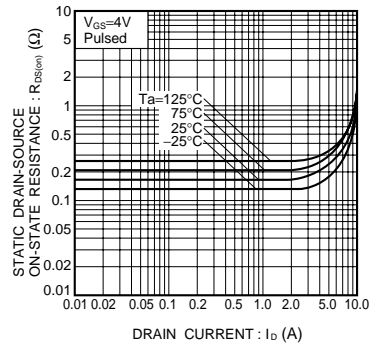


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (II)

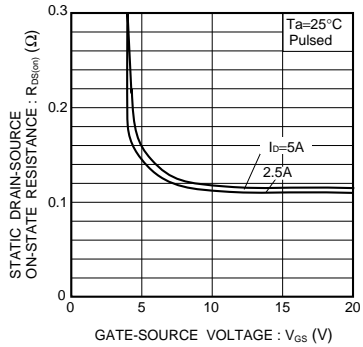


Fig.7 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

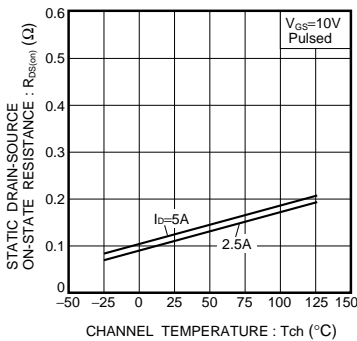


Fig.8 Static Drain-Source On-State Resistance vs. Channel Temperature

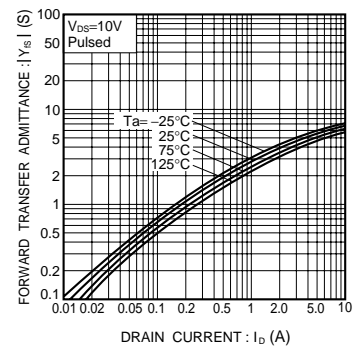


Fig.9 Forward Transfer Admittance vs. Drain Current

Transistors

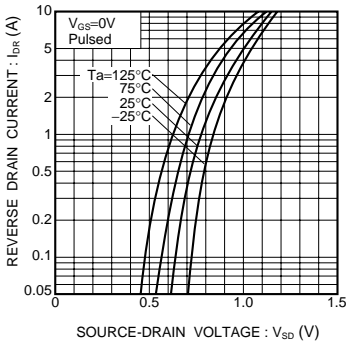


Fig.10 Reverse Drain Current vs. Source-Drain Voltage (I)

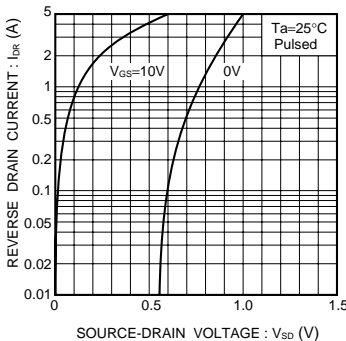


Fig.11 Reverse Drain Current vs. Source-Drain Voltage (II)

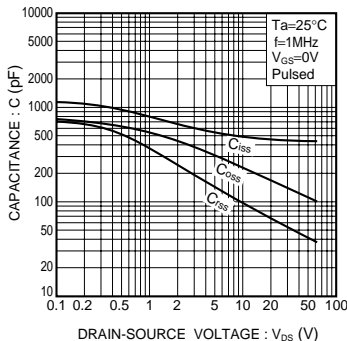


Fig.12 Typical Capacitance vs. Drain-Source Voltage

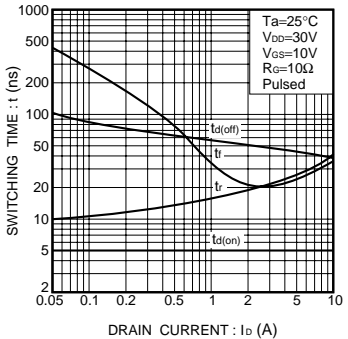


Fig.13 Switching characteristics (See Figures 16 and 17 for the measurement circuit and resultant waveforms)

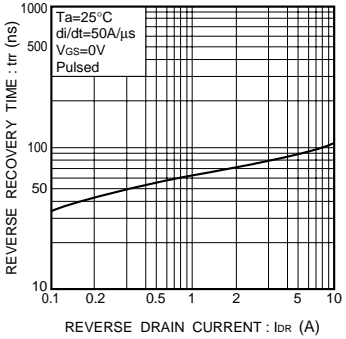


Fig.14 Reverse Recovery Time vs. Reverse Drain Current

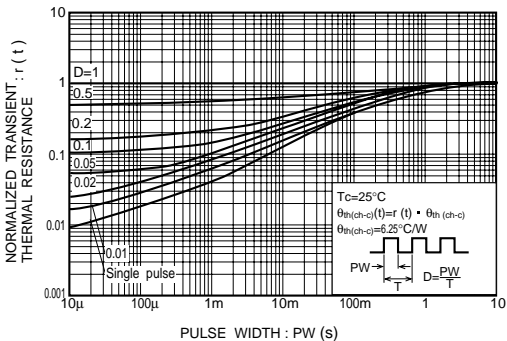


Fig.15 Normalized Transient Thermal Resistance vs. Pulse Width

Transistors

● Switching characteristics measurement circuit

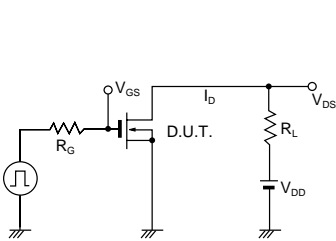


Fig.15 Switching Time Test Circuit

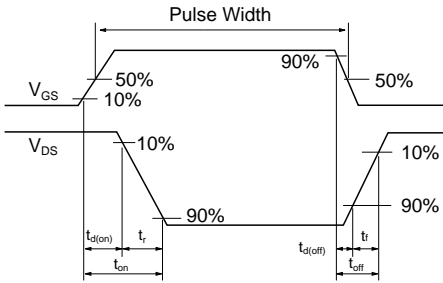


Fig.16 Switching Time Waveforms

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