

SPICE Device Model Si7923DN

Vishay Siliconix

Dual P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

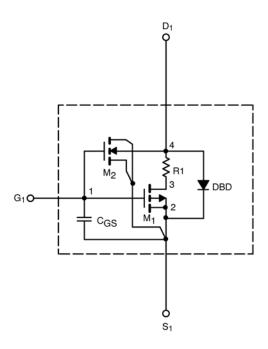
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

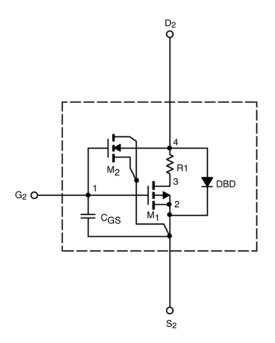
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC





This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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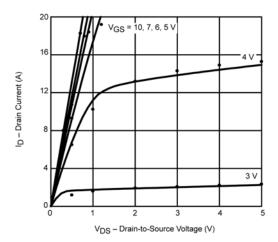
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static				•	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	2		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	24		Α
Drain-Source On-State Resistance ^a	r _{DS(on)}	$V_{GS} = -10 \text{ V}, I_D = -6.4 \text{ A}$	0.038	0.038	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$	0.059	0.060	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -6.4 \text{ A}$	13	13	S
Diode Forward Voltage ^a	V _{SD}	$I_{S} = -2.3 \text{ A}, V_{GS} = 0 \text{ V}$	-0.82	-0.80	V
Dynamic ^b					
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -6.4 \text{ A}$	13	14	nC
Gate-Source Charge	Q _{gs}		2.4	2.4	
Gate-Drain Charge	Q_{gd}		3.8	3.8	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = -15 \text{ V}, \text{ R}_L = 15 \Omega$ $I_D \cong -1 \text{ A}, \text{ V}_{GEN} = -10 \text{ V}, \text{ R}_G = 6 \Omega$	11	10	ns
Rise Time	t _r		8	12	
Turn-Off Delay Time	t _{d(off)}		40	38	
Fall Time	t _f		12	28	

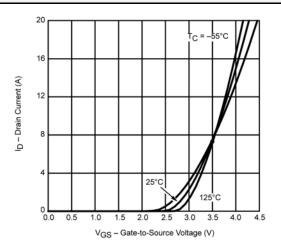
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

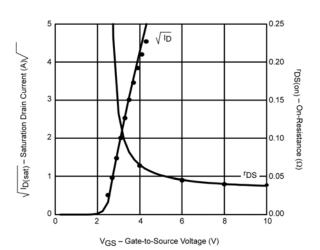


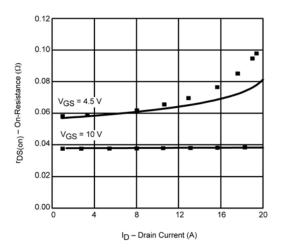
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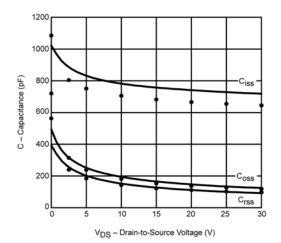
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

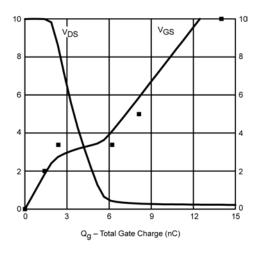












Note: Dots and squares represent measured data





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