

N-Channel Depletion-Mode MOSFET

#### **Ordering Information**

BV <sub>DSX</sub> /	R <sub>DS(ON)</sub>	I <sub>DSS</sub>	Order Number / Package			Product marking for TO-243AA:
BV <sub>DGX</sub>	(max)	(min)	TO-92	TO-243AA*	Die	LN1E*
500V	1.0KΩ	1.0mA	LND150N3	LND150N8	LND150ND	Where <b>*</b> = 2-week alpha date code

\* Same as SOT-89. Product shipped on 2000 piece carrier tape reels.

#### **Features**

- ESD gate protection
- □ Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling

ApplicationsSolid state relays

Converters

Normally-on switches

Power supply circuits

Constant current sources

Input protection circuits

Drain-to-Source Voltage

Drain-to-Gate Voltage

Gate-to-Source Voltage

Soldering Temperature\*

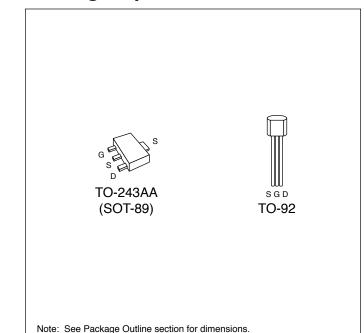
- Excellent thermal stability
- Integral source-drain diode
- $\hfill\square$  High input impedance and low  $C_{ISS}$

# Advanced DMOS Technology

The LND1 is a high voltage N-channel depletion mode (normallyon) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND1 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

# **Package Options**



\* Distance of 1.6 mm from case for 10 seconds.

Operating and Storage Temperature

Absolute Maximum Ratings

#### 12/13/01

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 $BV_{DSX}$ 

BV<sub>DGX</sub> ±20V

300°C

-55°C to +150°C

# Thermal Characteristics

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)	Power Dissipation @T <sub>A</sub> = 25°C	θ <sub>ic</sub> °C/W	θ <sub>ja</sub> °C/W	I <sub>DR</sub>	I <sub>DRM</sub> *
TO-92	30mA	30mA	0.74W	125	170	30mA	30mA
TO-243AA	30mA	30mA	1.6W <sup>†</sup>	31	105†	30mA	30mA

\*  $I_{\rm D}$  (continuous) is limited by max rated  $T_{\rm f}$ .

† Mounted on FR5 Board, 25mm x 25mm x 1.57mm. Significant Pp increase possible on ceramic substrate.

## Electrical Characteristics (@ 25°C unless otherwise specified)

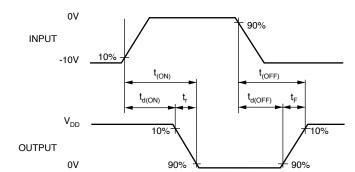
Symbol	Parameter	Min	Тур	Max	Unit	Conditions	
BV <sub>DSX</sub>	Drain-to-Source Breakdown Voltage	500			V	$V_{GS} = -10V, I_{D} = 1.0mA$	
V <sub>GS(OFF)</sub>	Gate-to-Source OFF Voltage	-1.0		-3.0	V	$V_{DS} = 25V, I_{D} = 100nA$	
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			5.0	mV/°C	$V_{DS} = 25V, I_{D} = 100nA$	
I <sub>GSS</sub>	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
I <sub>D(OFF)</sub>	Drain-to-Source Leakage Current			100	nA	V <sub>GS</sub> = -10V, V <sub>DS</sub> = 450V	
				100	μΑ	$V_{GS}$ = -10V, $V_{DS}$ = 0.8V max rating $T_A$ =125°C	
I <sub>DSS</sub>	Saturated Drain-to-Source Current	1.0		3.0	mA	$V_{GS} = 0V, V_{DS} = 25V$	
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance		850	1000	Ω	$V_{GS} = 0V, I_{D} = 0.5mA$	
$\Delta R_{DS(ON)}$	Change in RDS(ON) with Temperature			1.2	%/°C	$V_{GS} = 0V, I_{D} = 0.5mA$	
G <sub>FS</sub>	Forward Transconductance	1.0	2.0		m છ	$V_{GS} = 0V, I_{D} = 1.0mA$	
C <sub>ISS</sub>	Input Capacitance		7.5	10		V <sub>GS</sub> = -10V, V <sub>DS</sub> = 25V f = 1 MHz	
C <sub>OSS</sub>	Output Capacitance		2.0	3.5	pF		
C <sub>RSS</sub>	Reverse Transfer Capacitance		0.5	1.0			
t <sub>d(ON)</sub>	Turn-ON Delay Time		0.09				
tr	Rise Time		0.45		1	$V_{DD} = 25V, I_{D} = 1.0mA,$	
t <sub>d(OFF)</sub>	Turn-OFF Delay Time		0.1		μS	$R_{GEN} = 25\Omega$	
t <sub>f</sub>	Fall Time		1.3		1		
$V_{\rm SD}$	Diode Forward Voltage Drop			0.9	V	$V_{GS} = -10V, I_{SD} = 1.0mA$	
t <sub>rr</sub>	Reverse Recovery Time		200		ns	V <sub>GS</sub> = -10V, I <sub>SD</sub> = 1.0mA	

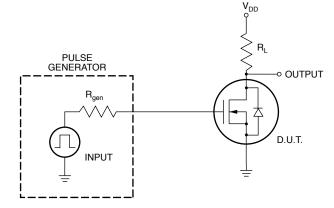
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)

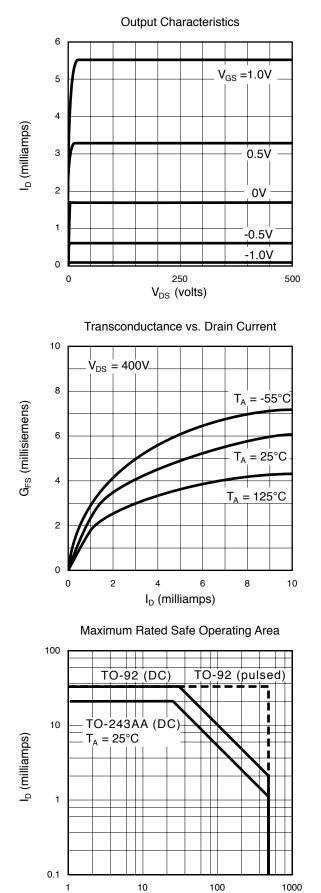
2. All A.C. parameters sample tested.

# **Switching Waveforms and Test Circuit**

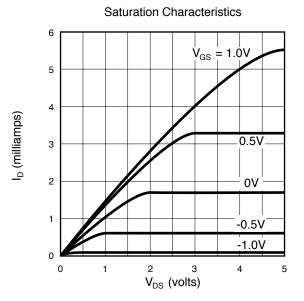




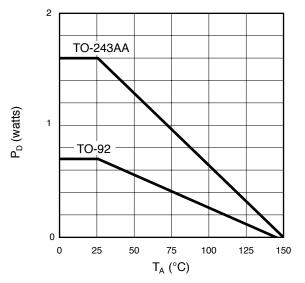
## **Typical Performance Curves**



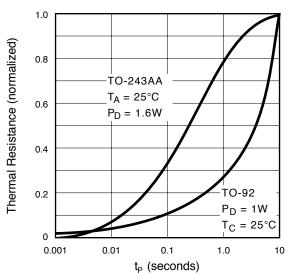
V<sub>DS</sub> (volts)



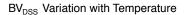
Power Dissipation vs. Ambient Temperature

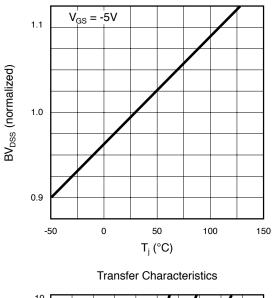


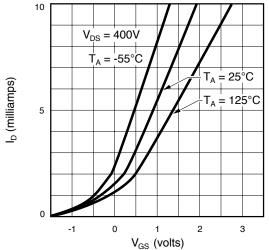
Thermal Response Characteristics



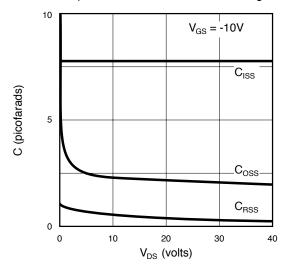
## **Typical Performance Curves**





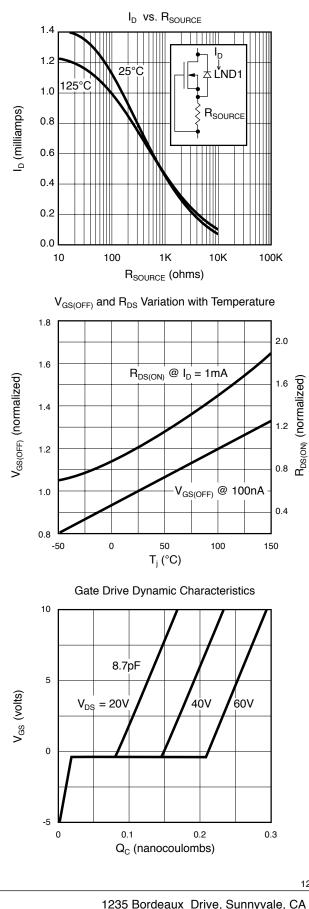


Capacitance vs. Drain-to-Source Voltage









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