

Dual P-Channel 12-V (D-S) MOSFET

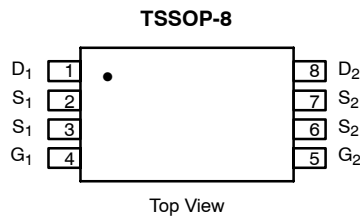
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-12	0.021 @ $V_{GS} = -4.5$ V	-5.8
	0.028 @ $V_{GS} = -2.5$ V	-5.0
	0.037 @ $V_{GS} = -1.8$ V	-4.4

FEATURES

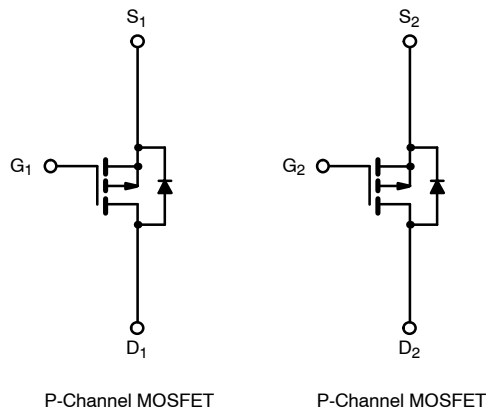
- TrenchFET® Power MOSFET

APPLICATIONS

- Load Switch
- Battery Switch



Ordering Information: Si6913DQ-T1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	-12		V
Gate-Source Voltage	V_{GS}	± 8		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-5.8	A
		$T_A = 70^\circ\text{C}$	-4.6	
Pulsed Drain Current (10 μs Pulse Width)	I_{DM}	-30		
Continuous Source Current (Diode Conduction) ^a	I_S	-1.0	-0.7	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.14	W
		$T_A = 70^\circ\text{C}$	0.73	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	86	$^\circ\text{C}/\text{W}$
		Steady State	124	
Maximum Junction-to-Foot (Drain)	R_{thJF}	52	65	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

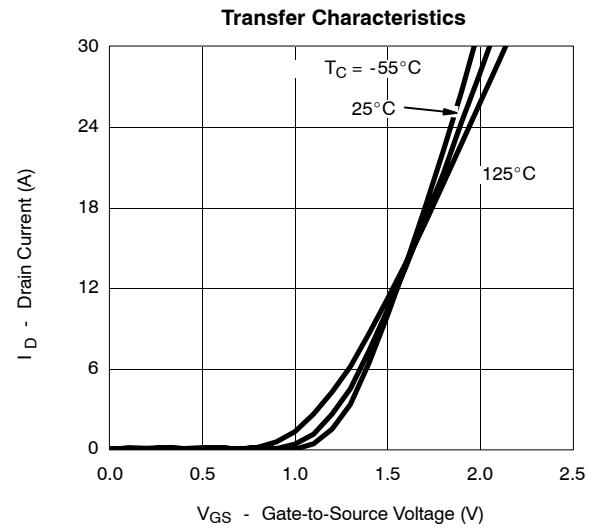
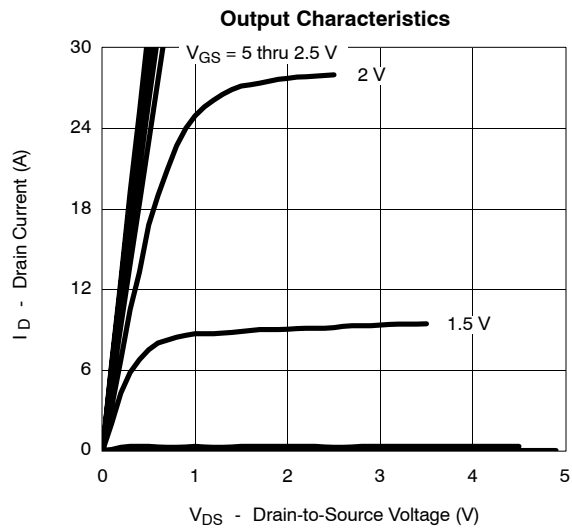


SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -400 μA	-0.40		-0.9	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -12 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -12 V, V _{GS} = 0 V, T _J = 70 °C			-25	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -5.8 A		0.016	0.021	Ω
		V _{GS} = -2.5 V, I _D = -5.0 A		0.021	0.028	
		V _{GS} = -1.8 V, I _D = -4.4 A		0.029	0.037	
Forward Transconductance ^a	g _{fs}	V _{DS} = -5 V, I _D = -5.8 A		25		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.0 A, V _{GS} = 0 V		-0.61	-1.1	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -5.8 A		18.5	28	nC
Gate-Source Charge	Q _{gs}			2.7		
Gate-Drain Charge	Q _{gd}			5.0		
Gate Resistance	R _g	f = 1.0 MHz		4.6		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		45	70	ns
Rise Time	t _r			80	120	
Turn-Off Delay Time	t _{d(off)}			130	200	
Fall Time	t _f			80	120	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -1.0 A, di/dt = 100 A/μs		65	100	

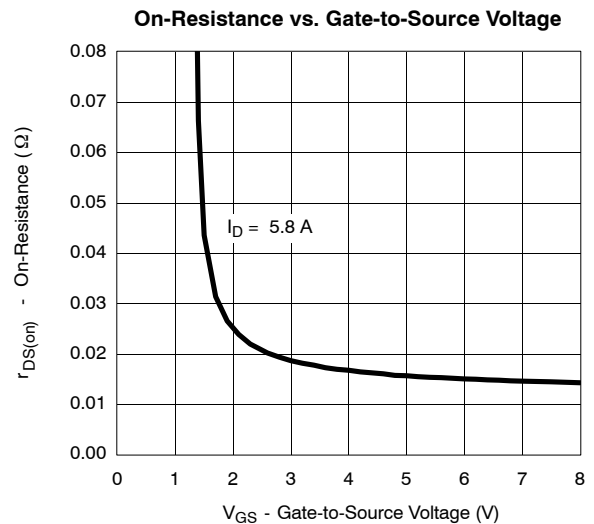
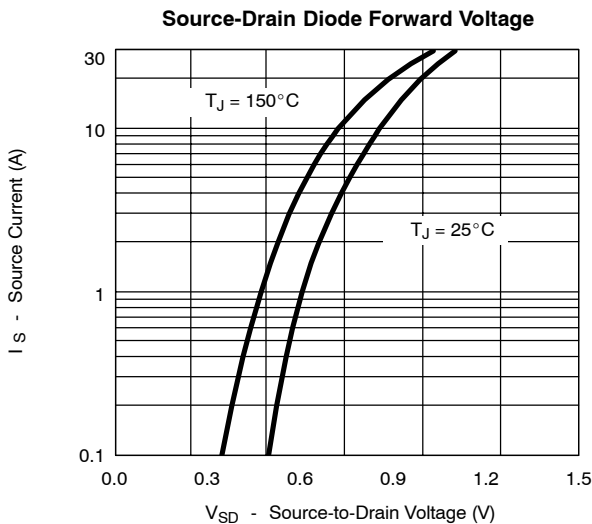
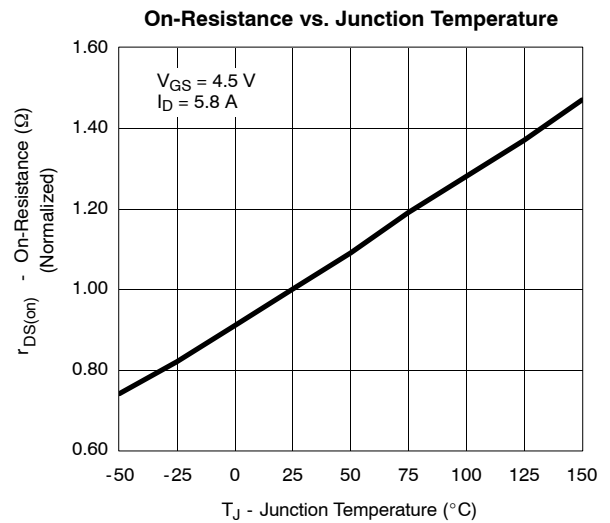
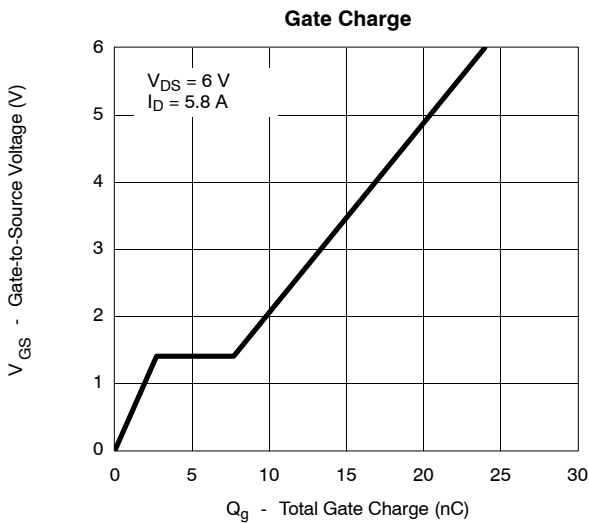
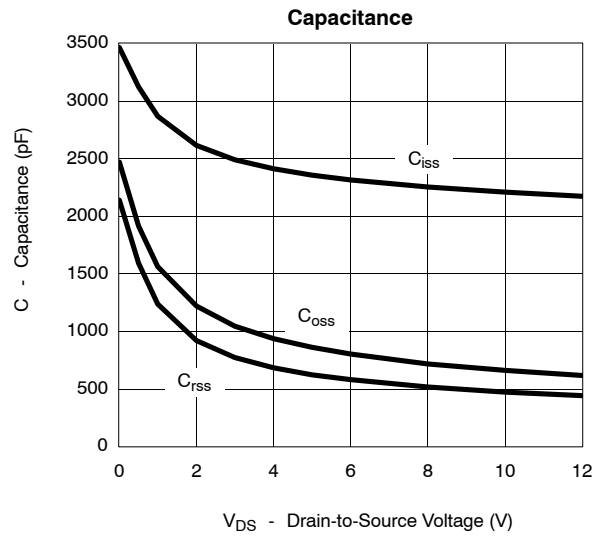
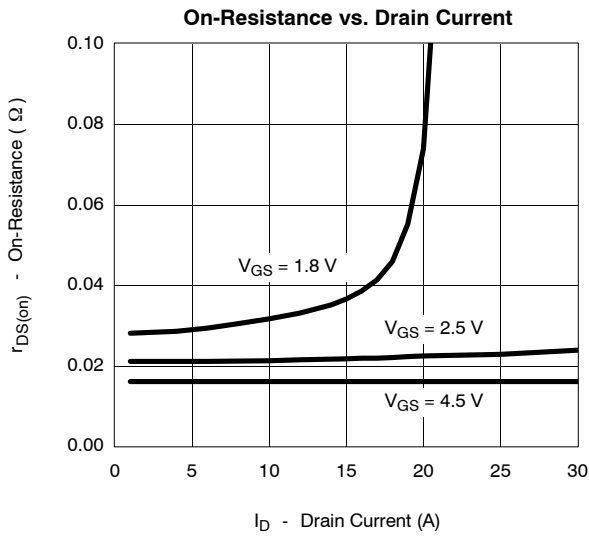
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

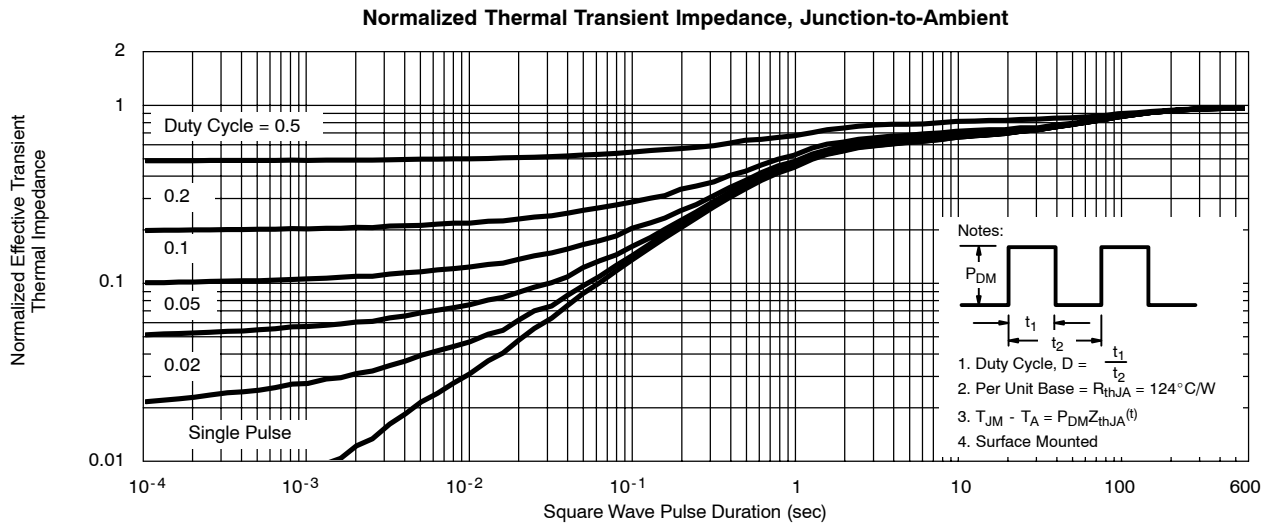
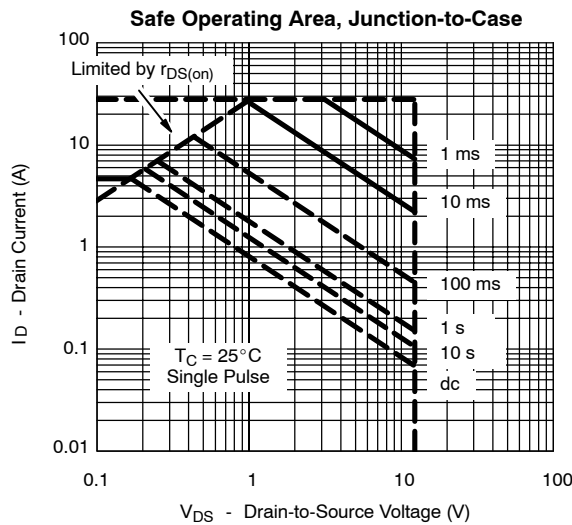
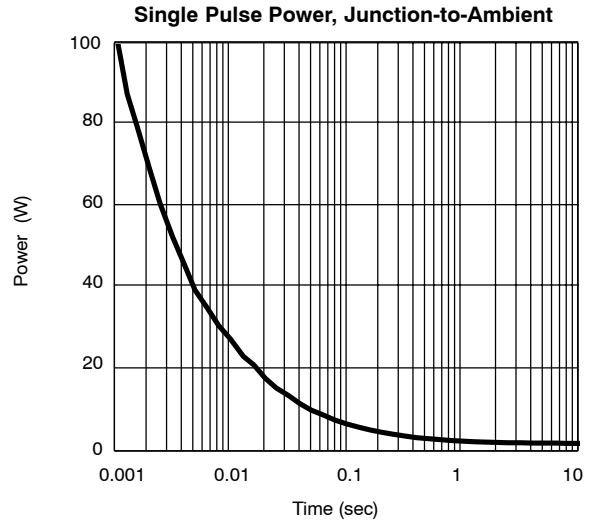
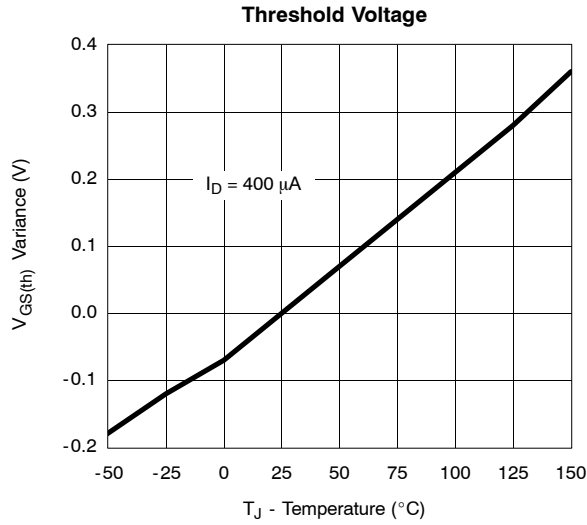


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