VP213

Dual 90MHz 6-Bit Analog to Digital Converter

Preliminary Information

DS4067 - 1.4 May 1996

The VP213 is a dual 90MHz 6-bit Analog to Digital Converter designed for use in consumer satellite receivers and decoders, video systems, multimedia and communications applications.

Operating from a single +5V supply, the VP213 includes an on-chip high bandwidth ADC driver amplifier, a 6-bit ADC and digital I/O that can be interfaced to either +5V or +3V. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

FEATURES

- 90MHz Conversion Rate
- TTL Clock/Data Interface
- 1 Volt Analog Input Range
- Internal ADC Reference
- Digital I/O's compatible with +5V or +3V logic
- Single 5 Volt Supply
- Dual ADC System for good channel matching

APPLICATIONS

- Satellite Decoders
- Multimedia
- Communications

ORDERING INFORMATION

VP213A CG MP1S (Commercial - 28 pin plastic SO)

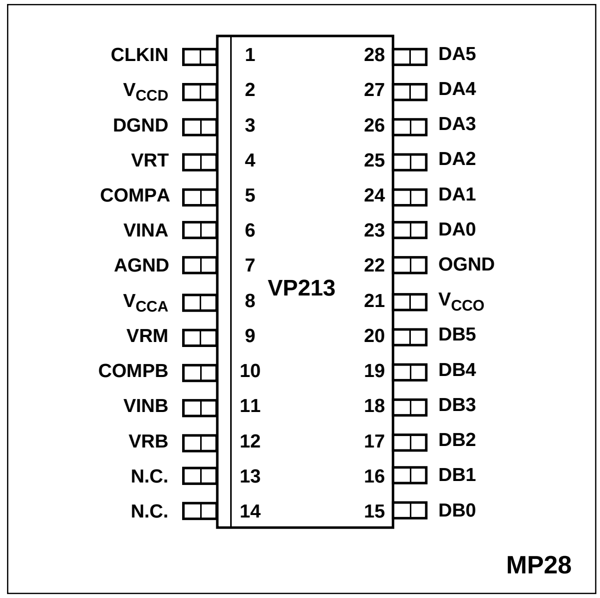


Fig.1 Pin connections - top view (wide body)

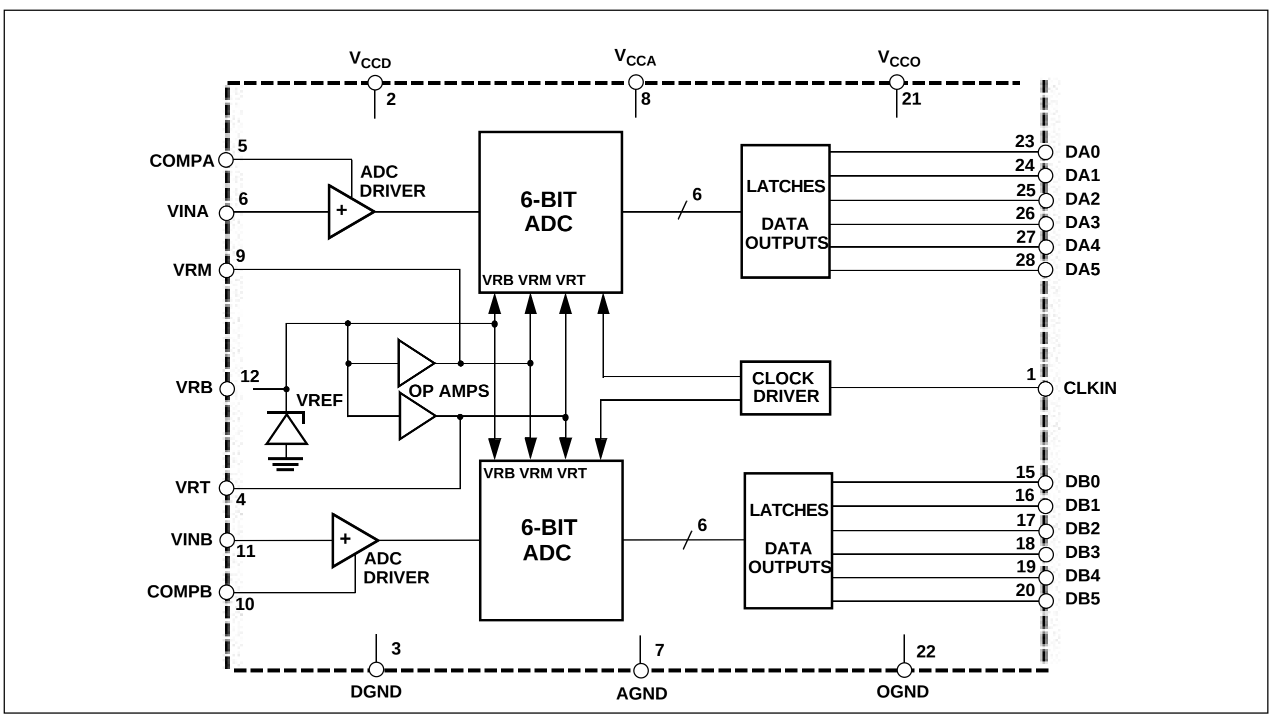


Fig.2 System block diagram

ABSOLUTE MAXIMUM RATINGS

DC supply voltage (V_{CCA}, V_{CCD}, V_{CCO})	-0.3 to+7V
Analog input voltage (VIN)	-0.3 to V_{CC}+0.3V
Digital inputs (CLKIN)	V_{CC}
Digital output current (Ioh, Iol, Isc)	-20 to +20mA
Ambient operating temperature (Tamb)	0°C to +70°C
Storage temperature (Tstorage)	-55°C to +125°C

THERMAL CHARACTERISTICS

THERMAL RESISTANCES

Junction to case(Θjc)	32°C/W
Junction to ambient(Θja)	84°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) Tamb = 25°C, $V_{CCA/D/O}$ = +5V, full temperature range = 0°C to +70°C

DC CHARACTERISTICS All specifications apply to either of the two ADCs

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution	-	-	-	6	-	-	Bits	
Static performance								
Differential non-linearity	DNL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
Integral non-linearity	INL	+25°C	4	-	-	±0.5	LSB	
		Full	4	-	-	±0.5	LSB	
No missing codes		Full	4		Guaranteed			
Power supply								
Analog supply voltage	V_{CCA}	Full	4	4.75	5.0	5.25	V	
Digital supply voltage	V_{CCD}	Full	4	4.75	5.0	5.25	V	
Output supply voltage	V_{CCO}	Full	4	4.75	5.0	5.25	V	
Analog supply current	AI_{CC}	+25°C	1	14	19	26	mA	
		Full	4	-	-	-	mA	
Digital supply current	DI_{CC}	+25°C	1	34	42	51	mA	
		Full	4	-	-	-	mA	
Output supply current	OI_{CC}	+25°C	1	3	11	15	mA	
		Full	4	-	-	-	mA	
Power dissipation	PD	+25°C	1	260	360	460	mW	
Analog input								
Input range	V_{in}	Full	5	-	1.0	-	V	Pk to Pk
Input resistance	R_{in}	+25°C	1	20k	25k	30k	Ω	
Input capacitance	C_{in}	+25°C	5	-	4.0	-	pF	
Gain variation	G_V	+25°C	4	-	-	0.25	dB	Fin=300Hz to 20MHz
Gain matching	G_m	+25°C	1	-	-	0.25	dB	Fin=15.36MHz
Input -3dB bandwidth	F3dB	+25°C	4	-	200	-	MHz	
Ain input voltage	Aindc	+25°C	1	3.35	3.6	3.85	V	
Comp output	Vcomp	+25°C	1	1.8	2.0	2.2	V	
CLKIN								
Input voltage high	V_{ih}	+25°C	1	2.0	-	-	V	
		Full	4	-	-	-	V	
Input voltage low	V_{il}	+25°C	1	-	-	0.8	V	
		Full	4	-	-	-	V	
Input current high	I_{ih}	+25°C	1	-	-	1	µA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 2.7V
Input current low	I_{il}	+25°C	1	–0.2	–0.35	–0.5	mA	V_{CCD} = 5.25V
		Full	4	-	-	-		V_{in} = 0.4V
TTL digital outputs								
Output voltage high	V_{oh}	+25°C	1	2.4	-	3.0	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{oh} = 400µA
Output voltage low	V_{ol}	+25°C	1	-	-	0.4	V	V_{CCO} = 4.75V
		Full	4	-	-	-	V	I_{ol} = 1mA
Output current high	I_{oh}	+25°C	1	-	-	-400	µA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	
Output current low	I_{ol}	+25°C	1	-	-	1	mA	V_{CCO} = 4.75V
		Full	4	-	-	-	-	

DC CHARACTERISTICS (cont.)

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Reference voltage								
V_{ref} ladder bottom	VRB	+25°C	1	2.367	2.525	2.671	V	
V_{ref} ladder middle	VRM	+25°C	1	2.848	3.04	3.212	V	
V_{ref} ladder top	VRT	+25°C	1	3.337	3.55	3.763	V	

AC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test Level	Value Min.	Value Typ.	Value Max.	Units	Conditions
Switching performance								
Clock high pulse width	$T_{pw}1$	+25°C	4	5.7	-	-	ns	
Clock low pulse width	$T_{pw}0$	+25°C	4	5.7	-	-	ns	
Max. conversion rate	F_{max}	+25°C	1	90	-	-	MHz	
Data output setup time	T_{setup}	+25°C	4	4	6	8	ns	Cload=10pF
Data output hold time	T_{hold}	+25°C	4	3	6	8	ns	Cload=10pF
Aperture delay	T_{ad}	+25°C	4	2	3	4	ns	
Aperture delay matching	$T_{ad\delta}$	+25°C	4	-	0.25	0.5	ns	
Aperture jitter	T_{aj}	+25°C	4	10	25	50	ps rms	
Dynamic performance								
Differential non-linearity	DNL	+25°C	4	–0.95	-	+1.2	LSB	F_{CLK} = 90.11MHz
Integral non-linearity	INL	+25°C	4	-	-	±1	LSB	
Signal to noise ratio	SNR	+25°C	1	31.8	-	-	dB	
Total harmonic distortion	THD	+25°C	4	40	-	-	dBc	
Effective No. of bits	ENOB	+25°C	1	5.0	5.6	-	bits	F_{IN} = 11.26MHz
Crosstalk rejection	CTR	+25°C	5	-	50	-	dBc	
Input offset	V_{os}	+25°C	1	-	±0.5	±1	LSB	
Error rate	BER	+25°C	5	-	$10e^{-8}$	-		

NOTES
1. An input voltage of 0.0 volts ±0.5 LSB should nominally correspond to the '011111' to '100000'B transition edge.

TEST LEVELS
Level 1 - 100% production tested.
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures.
Level 3 - Sample tested only.
Level 4 - Parameter is guaranteed by design and characterisation testing.
Level 5 - Parameter is typical value only.

Code	Input Voltage 1.0 Volt Full Scale	Digital Output Binary
00	Least positive valid input	000000
01	-	000001
●	●	●
31	-	011111
32	0	100000
33	-	100001
●	●	●
62	-	111110
63	Most positive valid input	111111

Table 1: Output coding

PIN DESCRIPTIONS - 28 Pin Plastic SO Package

Pin	Name	Description
1	CLKIN	TTL clock input
2	V_{CCD}	Digital voltage supply for ADC's and input clock
3	DGND	Digital ground
4	VRT	Reference voltage- ladder top
5	COMPA	Capacitor compensation - A channel
6	VINA	Analog signal input - A channel
7	AGND	Analog ground
8	V_{CCA}	Analog voltage supply for drivers and references
9	VRM	Reference voltage- ladder middle
10	COMPB	Capacitor compensation - B channel
11	VINB	Analog signal input - B channel
12	VRB	Reference voltage- ladder bottom
13	N.C.	Not connected
14	N.C.	Not connected
15	DB0	TTL digital output - channel B - LSB
16	DB1	
17	DB2	
18	DB3	
19	DB4	
20	DB5	TTL digital output - channel B - MSB
21	V_{CCO}	Output voltage supply for TTL data outputs
22	OGND	Output ground
23	DA0	TTL digital output - channel A - LSB
24	DA1	
25	DA2	
26	DA3	
27	DA4	
28	DA5	TTL digital output - channel A - MSB

Table 2: Pin descriptions

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by FFT analysis is reduced by 3dB.

Aperture Delay

The delay between the rising edge of the 90MHz clock signal and the instant the analog input signal is sampled.

Aperture Jitter

The sample to sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occurring outside the histogram cusp for a 1/2 FS sinewave.

Data Outputs, Set-up and Hold Time

Data output timings are measured from the 50% threshold to the 50% threshold on the rising edge of the output clock.

Differential Non-linearity

The deviation in any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve test fit according to the following expressions:

ENOB = SNR-1.76/6.02 or

ENOB = N-log2[rms error (actual)/rms error (ideal)]

where N is the conversion resolution and the actual rms error is the deviation from an ideal sine wave, calculated from the converter outputs with a sine wave input.

Integral Non-linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Signal-to-Noise Ratio (SNR)

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including the harmonics, but excluding D.C. with a full-scale analog input signal.

Device Description

The VP213 is a dual 90MHz 6-bit ADC system, (see Fig.2). Included on chip is a high bandwidth ADC driver amplifier, a 6-bit analog to digital converter, latches and TTL compatible data outputs. The VP213 also has the necessary bias voltages for the reference resistor chain in the 'flash' architecture of the ADC.

Analog Input

The analog inputs, (VIN_A,B) are A.C. coupled into the non-inverting input of the ADC driver amplifiers, which provide the necessary bandwidth, gain, offset and low impedance required to drive the ADC. The amplifier has been designed so that an input of 0 volts will produce an output level equal to the voltage present at the middle of the ADC resistor chain, VRM (3.00V typ.). This is achieved by an internal feedback loop within each amplifier which compares the amplifier output with VRM, (see Fig.3). This voltage will produce a transition binary code of 011111 to 100000 at the output of the ADC.

Reference Voltage

An on chip band gap voltage reference circuit combined with two op-amps provides all the necessary bias voltages for the ADC reference resistor chain, bottom (VRB), middle (VRM) and top(VRT). VRB, VRM and VRT have been brought out to pins 12, 9 and 4 respectively and should be decoupled with 100nF capacitors close to the package pins.

ADC Circuit

The VP213 employs a 'flash' architecture consisting of a reference resistor chain, an array of 64 comparators, encoding logic and a 6-bit latch. The 63 reference levels generated by the resistor chain are compared with the analog output signal from the ADC driver amplifier using the comparator array. This produces a thermometer code which the encoding logic converts into a 6-bit word.

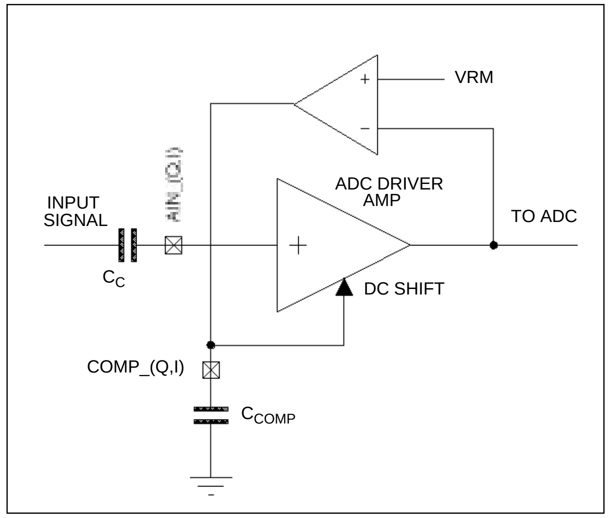


Fig.3 DC offset internal feedback loop

Digital Interface

The TTL data output pins, (DA0-DA5) and (DB0-DB5), have been optimized to interface with devices in close proximity to the VP213 and are designed to provide satisfactory logic levels at speeds up to 90MHz into a fanout of one and a total load capacitance of 10pF. All data outputs should have approximately equivalent loading to ensure proper setup and hold times. For capacitive loads in excess of 10pF, output buffers are recommended.

Clock Interface

The clock signal to the ADC synchronizes the sampling, conversion and output stages of the device as shown in the timing diagram (see Fig.4). The output of the ADC driver amp is sampled when the comparator array is latched on the rising edge of the input clock. Data is then presented to the TTL data outputs and latched on the falling edge of the input clock.

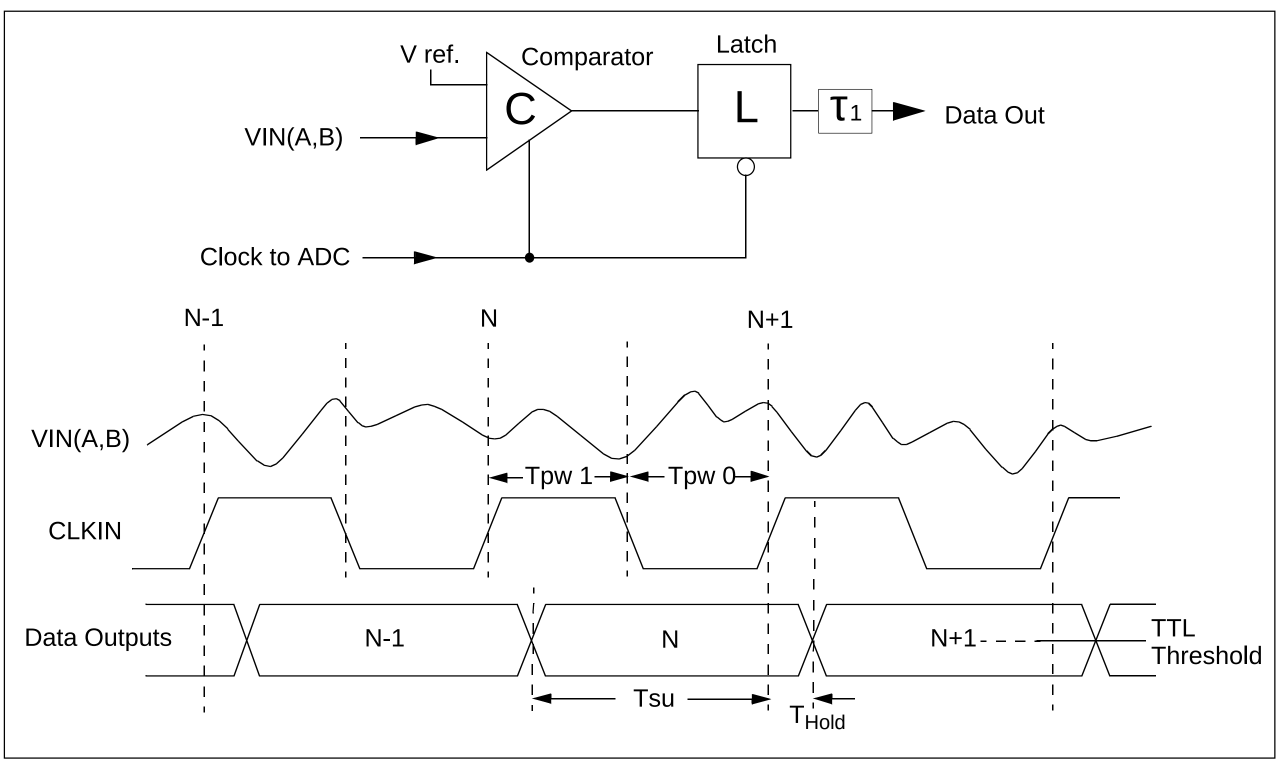


Fig.4 System timing diagram

Layout And Grounding

As with all high speed A to D converters, careful consideration must be given to the PCB layout. High performance can be obtained from the VP213 by tying all grounds to a solid low impedance ground plane. Separate analog and digital ground planes with a single common link under the device can also be used to help reduce the amount of digital noise fed back into the analog section of the converter.

The VP213 should be decoupled with low impedance 100nF ceramic capacitors close to the package pins to avoid lead inductance effects and the decoupling on supply lines should further be improved by using a 47µF tantalum capacitor in parallel with a 100nF ceramic capacitor. If VCCA is derived from VCCD, a small inductor should be used to reduce digital noise on the analog power supply. Jitter and noise on clock input pins must be minimised. Long clock lines should therefore be avoided and all clock lines correctly terminated. Cross talk of digital signals to the analog inputs must also be prevented as sampling cross talk produces DC offsets on the sampled data, for this reason analog inputs should not be run next to clock or data lines. Device connections to the ground plane should be as short as possible.

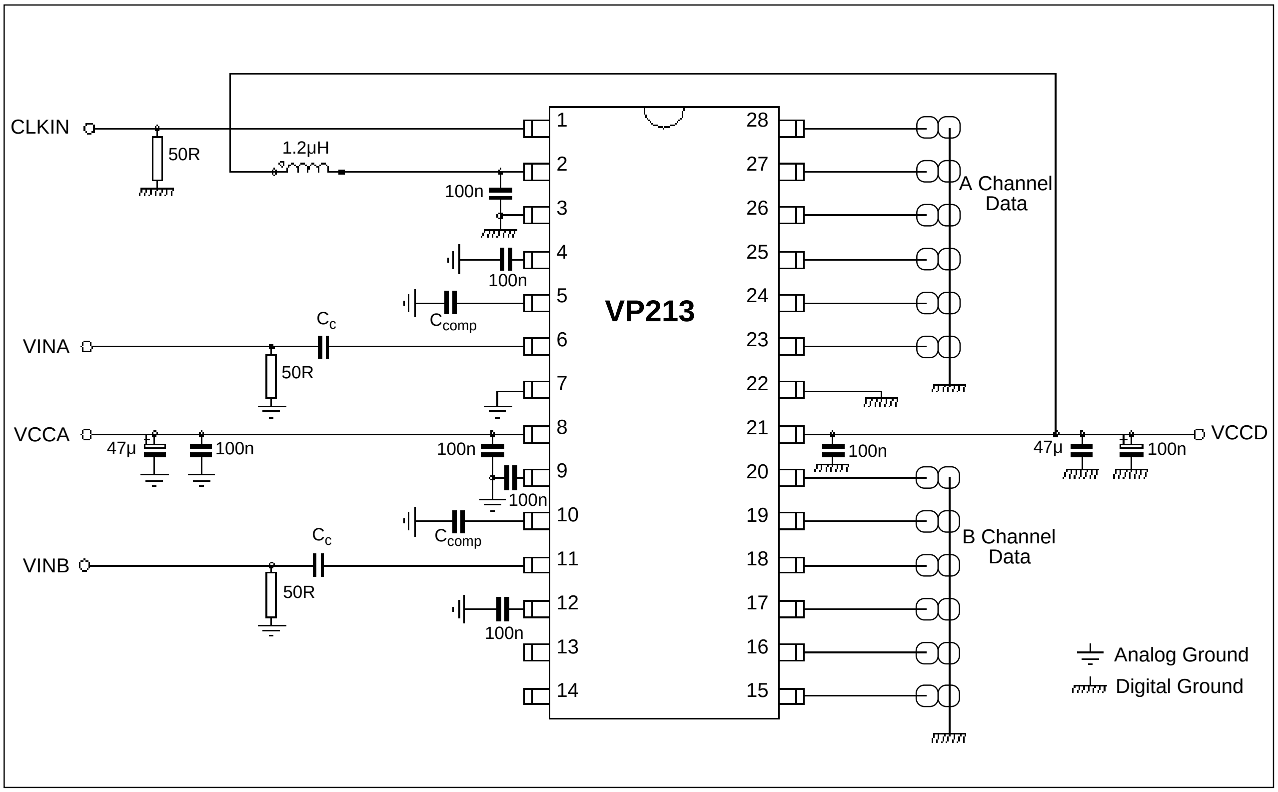


Fig.5 Applications diagram

Application Circuit

Fig.5 shows a typical applications circuit for the VP213. The supply connections are made using separate low noise digital and analog power supplies and VCCD is further isolated from VCCO using a 1.2µH inductor.

The COMPA and COMPB pins must be decoupled to reduce any ripple at low frequencies which may distort the ADC driver amplifier output, (see Fig.2.) The decoupling capacitor value is determined by the required low frequency performance of the system and can be obtained from the following equation.

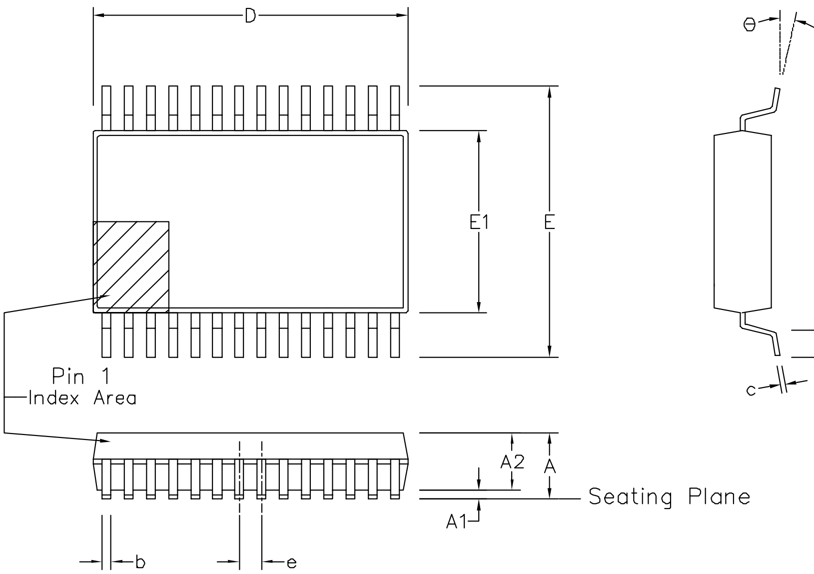
$$C_{Comp} = \frac{75x10^{-6}}{F_{in} \times V_{Ripple}}$$

A ripple voltage ≤ 10mV is recommended for good system performance, e.g. If the analog input frequency F_{in}= 10KHz a value of 0.75µF is required for C_{Comp}.

To ensure effective A.C. coupling at low input frequencies, the coupling capacitors on pins 6 and 11 can be calculated from the high pass filter corner frequency equation,

$$F_c = \frac{1}{2 \times \pi \times RC}$$

where
F_c = Lower -3dB corner frequency
(R = Input Resistance, 25K typ. - 20K min)



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	9.90		10.50		0.390		0.413
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
Θ	0°		8°		0°		8°
	Pin features						
N	28						
Conforms to JEDEC MO-150 AH Iss. B							

This drawing supersedes:-
418/ED/51481/004 (Swindon/Roborough)
TD/D 993 (Oldham)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

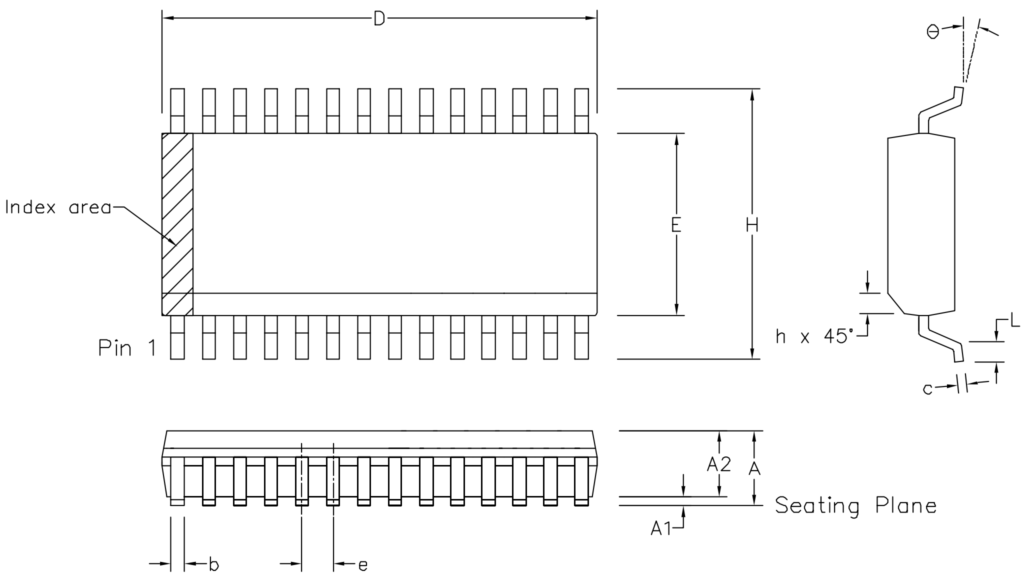
ORIGINATING SITE: SWINDON

ISSUE	1	2			
ACN	201935	205232			
DATE	27FEB97	25SEP98			
APPD.					

MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 28 lds SSOP-5.3 mm Body Width (NP)

Drawing Number
GPD00296



Symbol	Control Dimensions in millimetres MIN	Nominal	MAX	Altern. Dimensions in inches MIN	Nominal	MAX
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2	2.25		2.35	0.089		0.092
D	17.70		18.10	0.697		0.713
H	10.00		10.65	0.394		0.419
E	7.40		7.60	0.291		0.299
L	0.40		1.27	0.016		0.050
e	1.27 BSC.			0.050 BSC.		
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.013
Θ	0°		8°	0°		8°
h	0.25		0.75	0.010		0.029
	Pin features					
N	28					
Conforms to JEDEC MS-013AE Iss. C						

Notes:

1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ORIGINATING SITE: SWINDON

ISSUE	1	2			
ACN	006746	201943			
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APPROVED					

MITEL SEMICONDUCTOR

Title: Package Outline Drawing for 28 lds SOIC(W)-0.300" Body Width (MP)

Drawing Number
GPD00017

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