



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{iss}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral Source-Drain diode
- ▶ High input impedance and high gain
- ▶ Complementary N- and P-channel devices

### Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

### Ordering Information

$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ max ( $\Omega$ )	$V_{GS(th)}$ max (V)	Package Option
			TO-236AB (SOT-23)
240	15	2.0	TN2124K1-G

-G indicates package is RoHS compliant ('Green')



### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

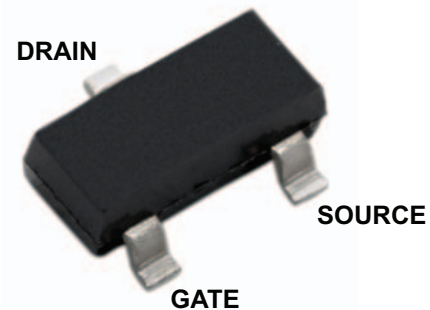
\* Distance of 1.6mm from case for 10 seconds.

### General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Pin Configuration



TO-236AB (SOT-23) (K1)

### Product Marking



W = Code for week sealed

TO-236AB (SOT-23) (K1)

### Thermal Characteristics

Package	I <sub>D</sub> (continuous) <sup>(*)</sup> (mA)	I <sub>D</sub> (pulsed) (mA)	Power Dissipation @T <sub>A</sub> = 25°C (W)	θ <sub>jc</sub> (°C/W)	θ <sub>ja</sub> (°C/W)	I <sub>DR</sub> <sup>(*)</sup> (mA)	I <sub>DRM</sub> (mA)
TO-236AB (SOT-23) (K1)	134	250	0.36	200	350	134	250

**Notes:**

\* I<sub>D</sub> (continuous) is limited by max rated T<sub>J</sub>.

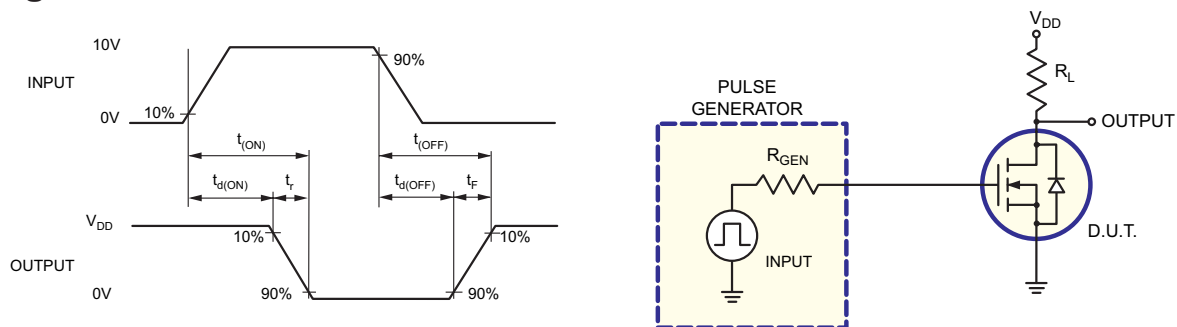
### Electrical Characteristics (@25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV <sub>DSS</sub>	Drain-to-source breakdown voltage	240	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate threshold voltage	0.8	-	2.0	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with temperature	-	-	-5.5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate body leakage	-	0.1	100	nA	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero gate voltage drain current	-	-	1.0	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
		-	-	100	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0.8 Max Rating, T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	ON-state drain current	140	-	-	mA	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static drain-to-source ON-state resistance	-	-	30	Ω	V <sub>GS</sub> = 3.0V, I <sub>D</sub> = 25mA
		-	-	15	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 120mA
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with temperature	-	0.7	1.0	%/°C	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 120mA
G <sub>FS</sub>	Forward transductance	100	170	-	mmho	V <sub>DS</sub> = 25V, I <sub>D</sub> = 120mA
C <sub>ISS</sub>	Input capacitance	-	38	50	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz
C <sub>OSS</sub>	Common source output capacitance	-	9.0	15		
C <sub>RSS</sub>	Reverse transfer capacitance	-	3.0	5.0		
t <sub>d(ON)</sub>	Turn-ON delay time	-	4.0	7.0	ns	V <sub>DD</sub> = 25V, I <sub>D</sub> = 140mA, R <sub>GEN</sub> = 25Ω
t <sub>r</sub>	Rise time	-	2.0	5.0		
t <sub>d(OFF)</sub>	Turn-OFF delay time	-	7.0	10		
t <sub>f</sub>	Fall time	-	9.0	12		
V <sub>SD</sub>	Diode forward voltage drop	-	-	1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 120mA
t <sub>rr</sub>	Reverse recovery time	-	400	-	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 120mA

**Notes:**

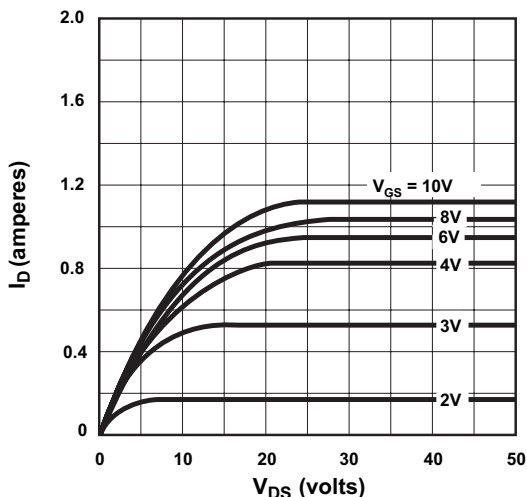
- (1) All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
- (2) All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit

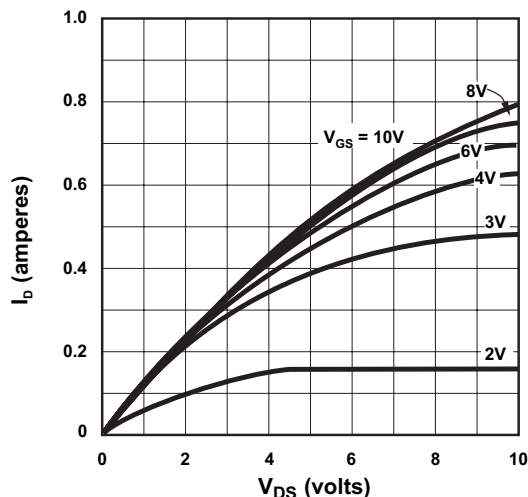


# Typical Performance Curves

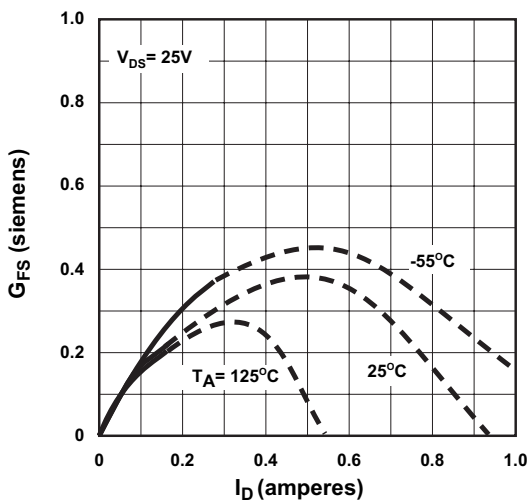
Output Characteristics



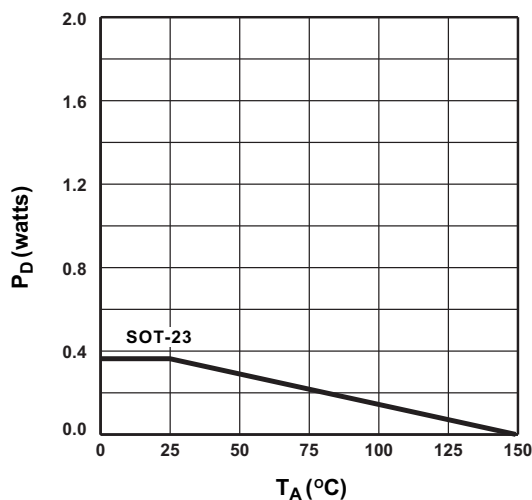
Saturation Characteristics



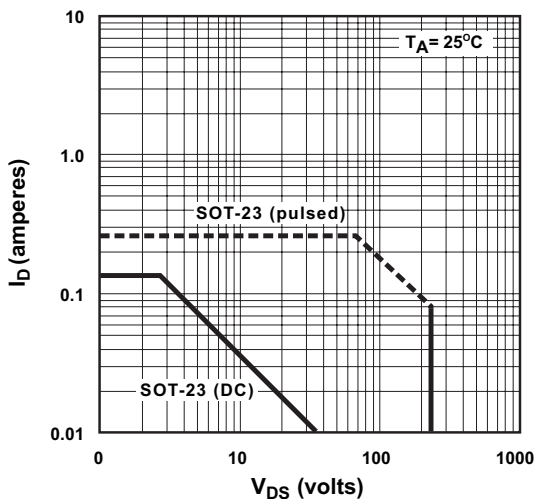
Transconductance vs. Drain Current



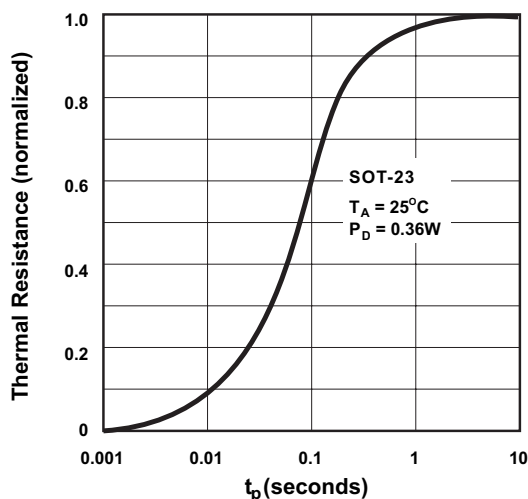
Power Dissipation vs. Temperature



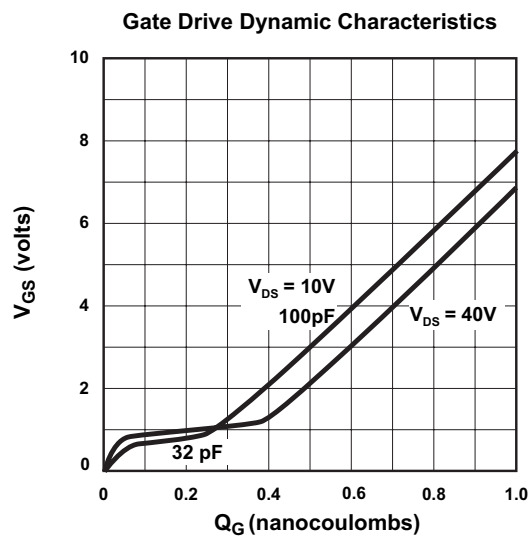
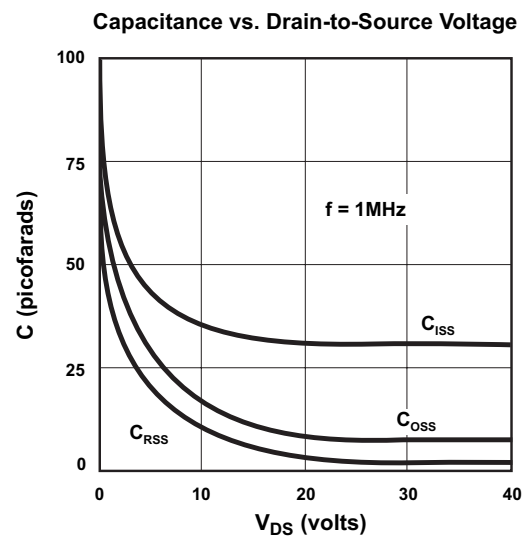
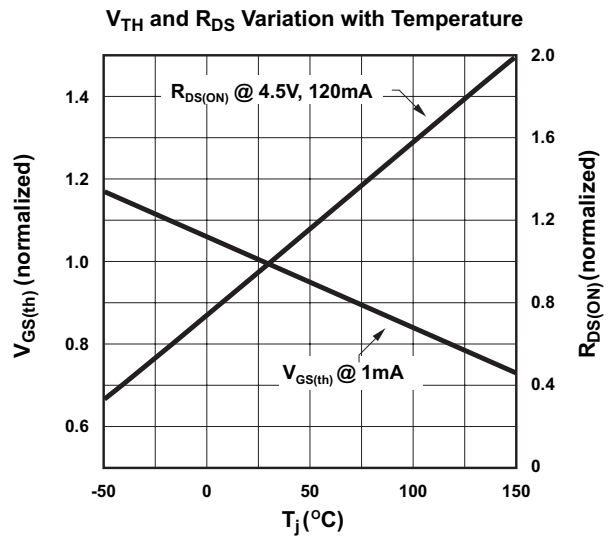
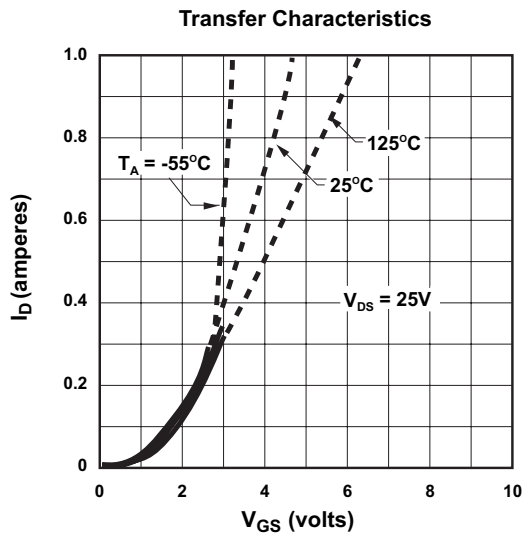
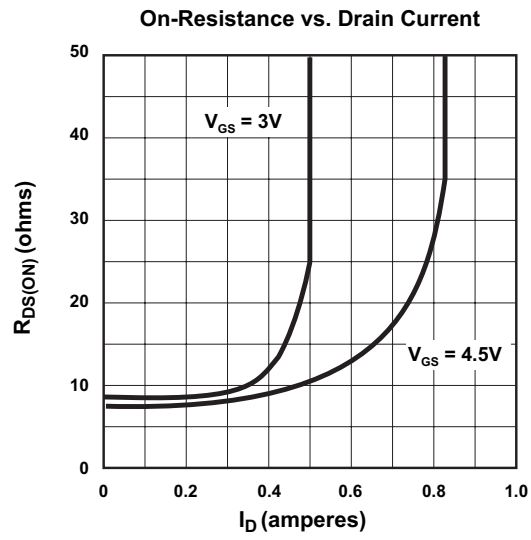
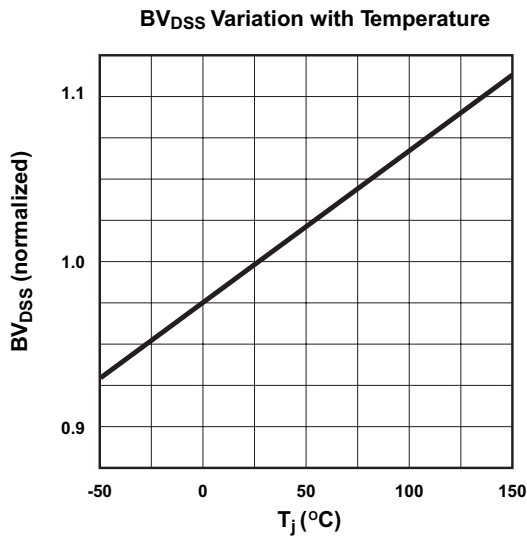
Maximum Rated Safe Operating Area



Thermal Response Characteristics

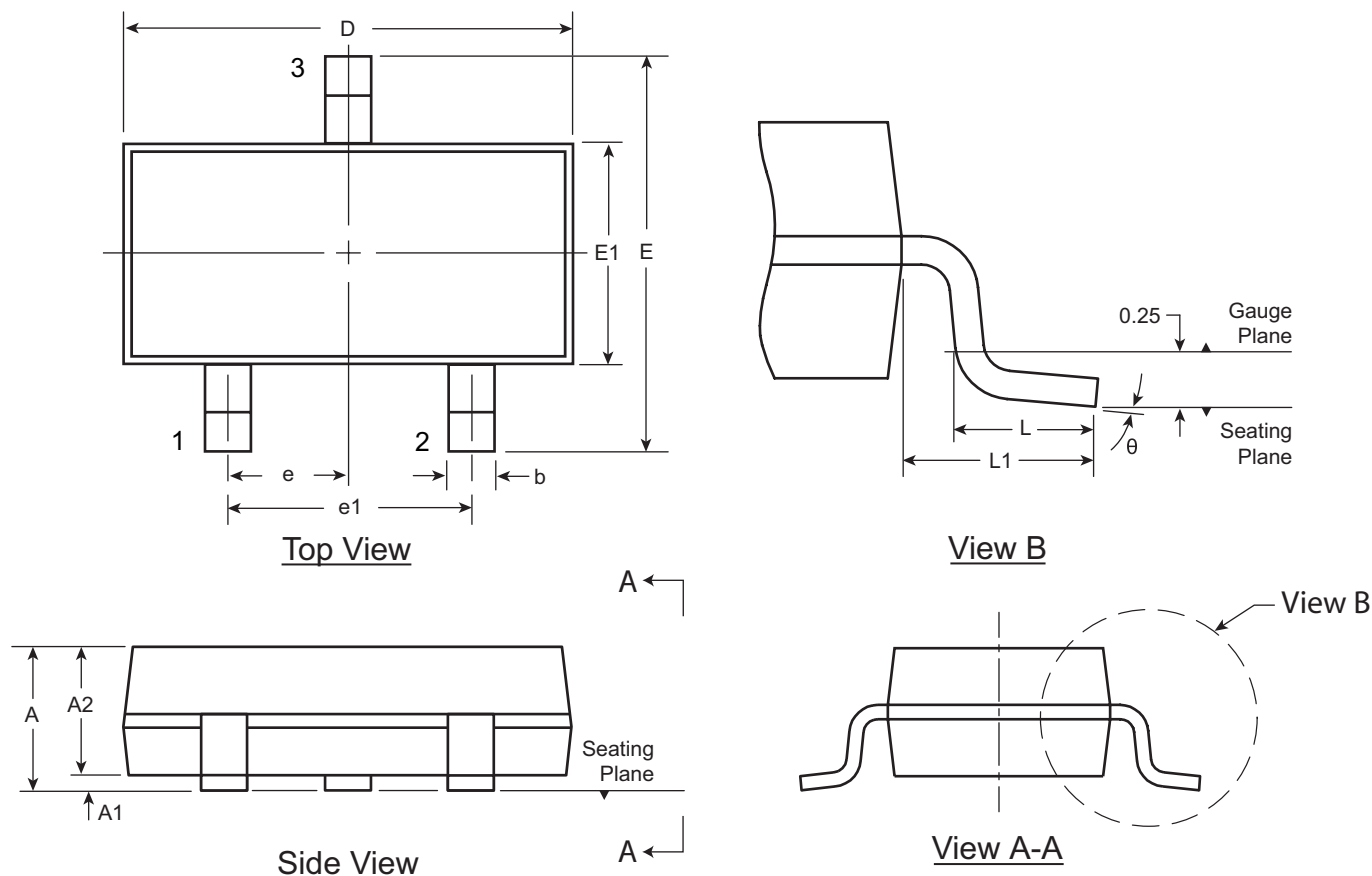


Typical Performance Curves (cont.)



### 3-Lead TO-236AB (SOT-23) Package Outline (K1)

2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	$\theta$
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.40	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.  
 Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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