



## P-Channel 40-V (D-S), 175 °C MOSFET

## PRODUCT SUMMARY

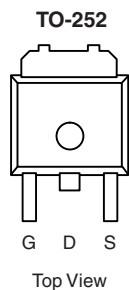
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>d</sup>
- 40	0.0094 at $V_{GS} = - 10$ V	- 50
	0.0145 at $V_{GS} = - 4.5$ V	- 50

## FEATURES

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature

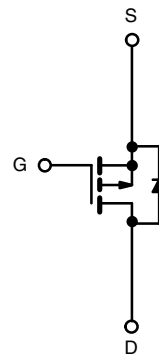


Available  
RoHS\*  
COMPLIANT



Drain Connected to Tab

Ordering Information: SUD50P04-09L  
SUD50P04-09L (Lead (Pb)-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS  $T_A = 25$  °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$I_D$	$T_C = 25$ °C	- 50 <sup>d</sup>
		$T_C = 125$ °C	- 50 <sup>d</sup>
Pulsed Drain Current	$I_{DM}$	- 100	A
Avalanche Current	$I_{AS}$	- 50	
Single Avalanche Energy <sup>a</sup>	$L = 0.1$ mH	$E_{AS}$	125
Power Dissipation	$P_D$	$T_C = 25$ °C	136 <sup>c</sup>
		$T_A = 25$ °C	3 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 175	°C

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>b</sup>	$R_{thJA}$	$t \leq 10$ sec	15	°C/W
		Steady State	40	
Junction-to-Case	$R_{thJC}$	0.82	1.1	

## Notes:

- Duty cycle  $\leq 1$  %.
- When Mounted on 1" square PCB (FR-4 material).
- See SOA curve for voltage derating.
- Package limited.

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1		-3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-50	
		$V_{DS} = -32\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			-150	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	-50			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		0.0075	0.0094	$\Omega$
		$V_{GS} = -10\text{ V}, I_D = -50\text{ A}, T_J = 125\text{ }^\circ\text{C}$			0.014	
		$V_{GS} = -10\text{ V}, I_D = -50\text{ A}, T_J = 175\text{ }^\circ\text{C}$			0.017	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{GS} = -4.5\text{ V}, I_D = -18\text{ A}$		0.0115	0.0145	S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1\text{ MHz}$		4800		$\mu\text{F}$
Output Capacitance	$C_{oss}$			700		
Reverse Transfer Capacitance	$C_{rss}$			550		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = -20\text{ V}, V_{GS} = -10\text{ V}, I_D = -50\text{ A}$		102	150	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			18.5		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			27		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -20\text{ V}, R_L = 0.4\text{ }\Omega$ $I_D \cong -50\text{ A}, V_{GEN} = -10\text{ V}, R_G = 6\text{ }\Omega$		10	15	ns
Rise Time <sup>c</sup>	$t_r$			60	90	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			145	220	
Fall Time <sup>c</sup>	$t_f$			140	220	
<b>Source-Drain Diode Ratings and Characteristics</b> ( $T_C = 25\text{ }^\circ\text{C}$ ) <sup>b</sup>						
Continuous Current	$I_S$				-50	A
Pulsed Current	$I_{SM}$				-100	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = -50\text{ A}, V_{GS} = 0\text{ V}$		-1.0	-1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = -50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		55	85	ns

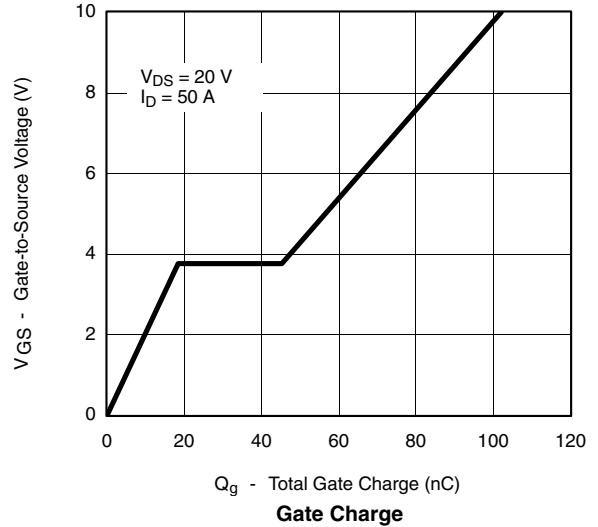
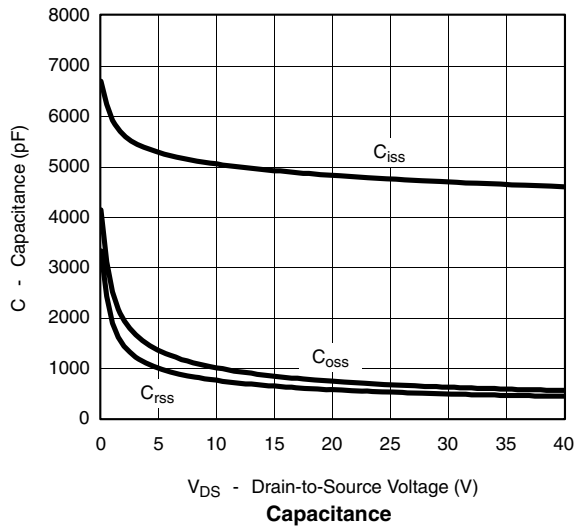
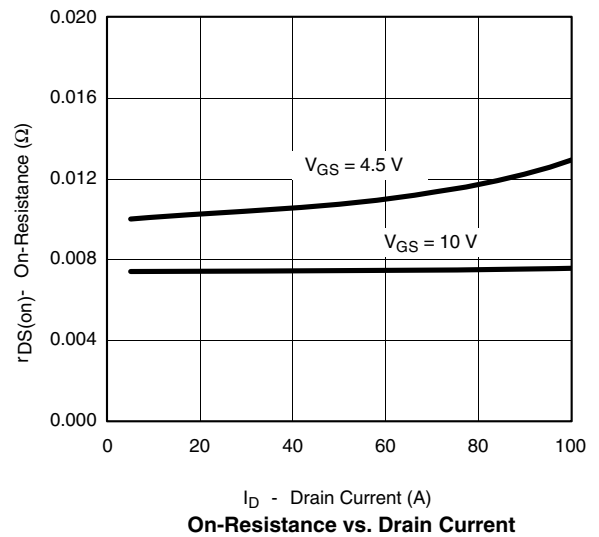
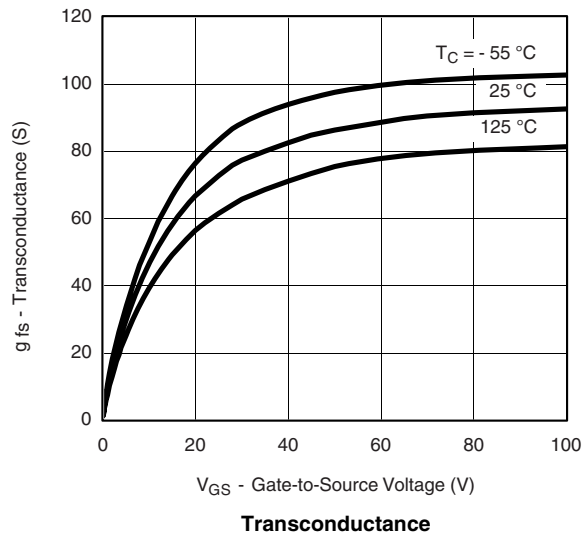
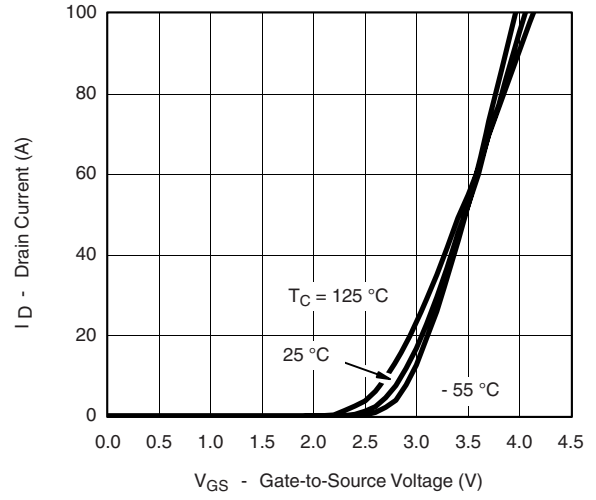
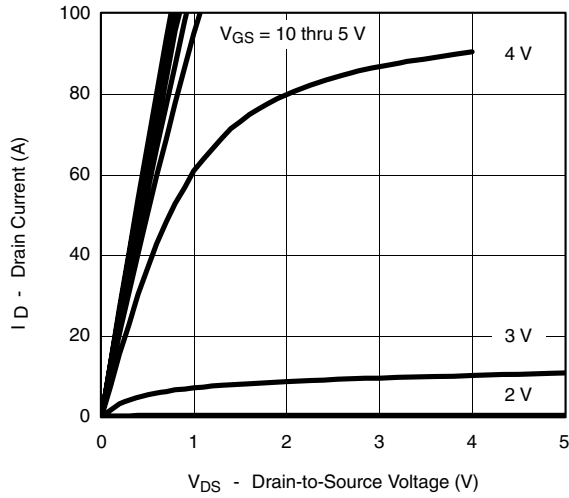
## Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



**TYPICAL CHARACTERISTICS** 25 °C unless noted

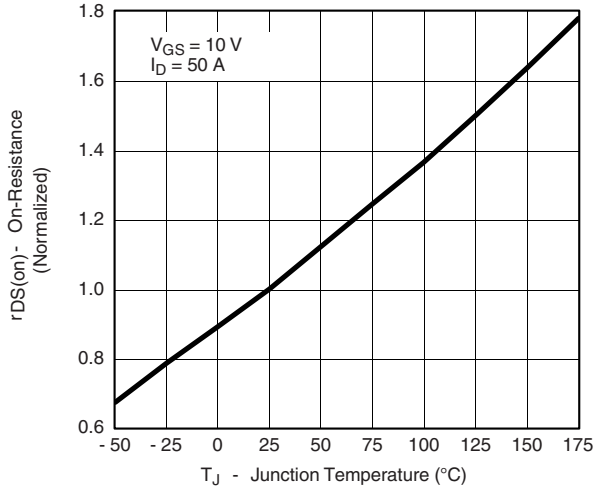


# SUD50P04-09L

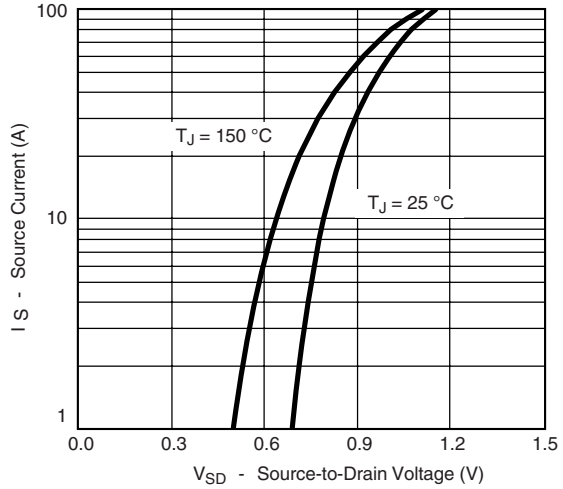


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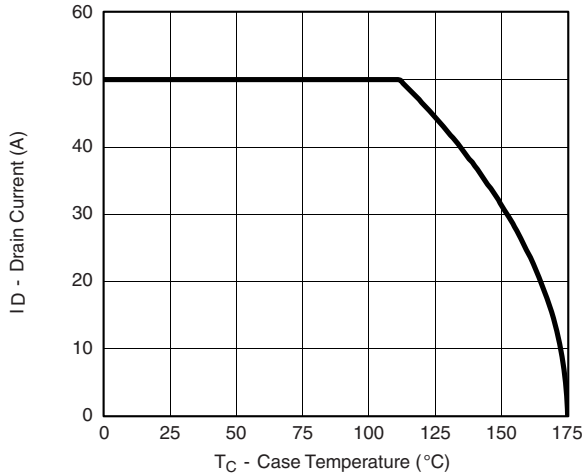


On-Resistance vs. Junction Temperature

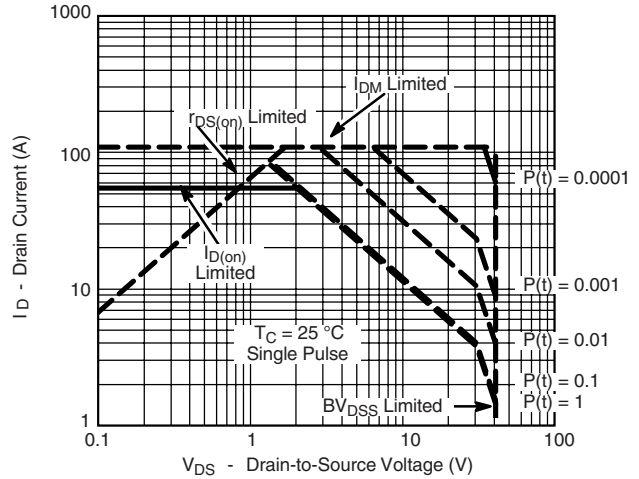


Source-Drain Diode Forward Voltage

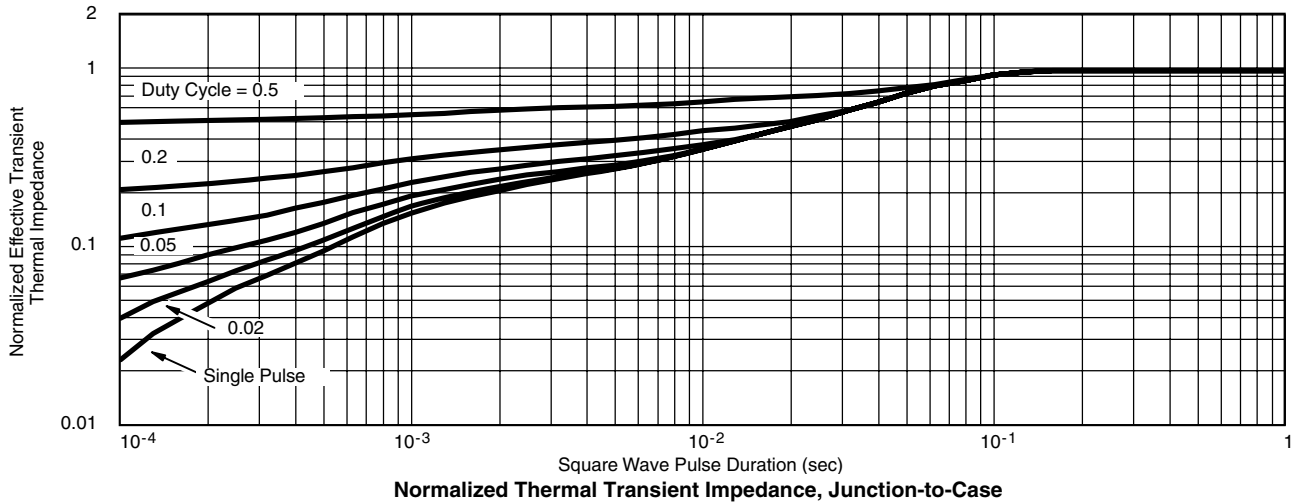
## THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72243>.



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