



N-Channel Depletion-Mode Vertical DMOS FET

Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Linear amplifiers
- ▶ Constant current sources
- ▶ Battery operated systems
- ▶ Telecom

General Description

The DN2470 is a low threshold depletion-mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FET is ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

| BV_{DSX}/BV_{DGX} | $R_{DS(ON)}$ (max) | I_{DSS} (min) | Package Options |
|---------------------|--------------------|-----------------|-----------------|
| | | | TO-252 (D-PAK) |
| 700V | 42Ω | 500mA | DN2470K4-G |



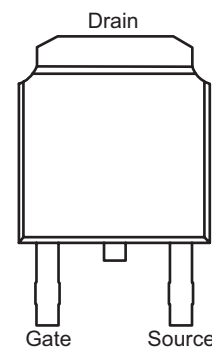
Absolute Maximum Ratings

| Parameter | Value |
|-----------------------------------|-----------------|
| Drain-to-source voltage | BV_{DSX} |
| Drain-to-gate voltage | BV_{DGX} |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

*Distance of 1.6mm from case for 10 seconds.

Package Option



TO-252 (D-PAK)
(top view)

Thermal Characteristics

| Package | I_D (continuous) ¹ | I_D (pulsed) | Power Dissipation @ $T_A = 25^\circ\text{C}$ | θ_{jc} ($^\circ\text{C}/\text{W}$) | θ_{ja} ($^\circ\text{C}/\text{W}$) | I_{DR}^1 | I_{DRM} |
|---------|------------------------------------|-------------------|---|---|---|------------|-----------|
| TO-252 | 170mA | 500mA | 2.5W ² | 6.25 | 50 ² | 170mA | 500mA |

Notes:

- I_D (continuous) is limited by max rated T_j .
- Mounted on FR4 board, 25mm x 25mm x 1.57mm

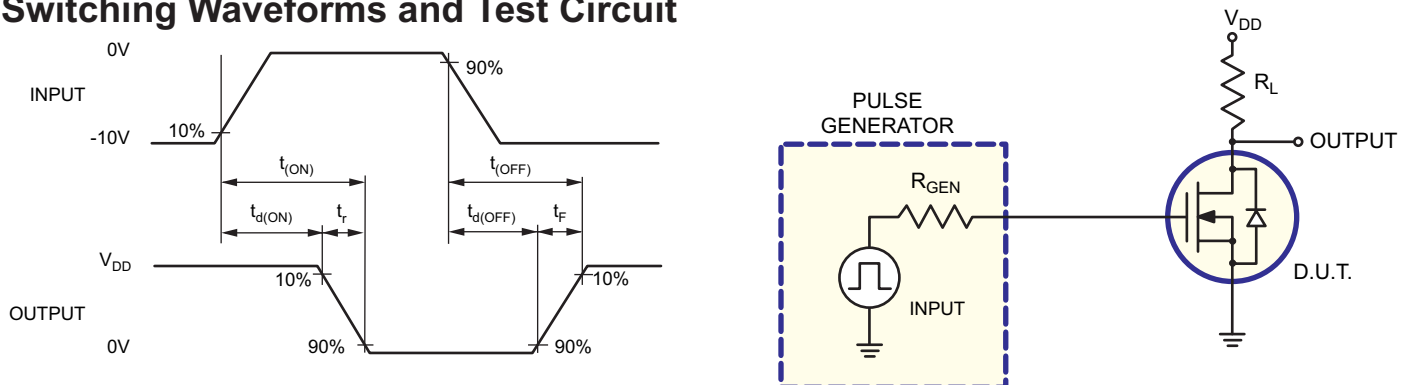
Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------------------|--|------|-----|------|----------------------|--|
| BV_{DSX} | Drain-to-source breakdown voltage | 700 | - | - | V | $V_{GS} = -5.0\text{V}, I_D = 100\mu\text{A}$ |
| $V_{GS(OFF)}$ | Gate-to-source OFF voltage | -1.5 | - | -3.5 | V | $V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$ |
| $\Delta V_{GS(OFF)}$ | Change in $V_{GS(OFF)}$ with temperature | - | - | 4.5 | mV/ $^\circ\text{C}$ | $V_{DS} = 25\text{V}, I_D = 10\mu\text{A}$ |
| I_{GSS} | Gate body leakage current | - | - | 100 | nA | $V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ |
| $I_{D(OFF)}$ | Drain-to-source leakage current | - | - | 1.0 | μA | $V_{DS} = \text{Max rating}, V_{GS} = -10\text{V}$ |
| | | - | - | 1.0 | mA | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = -10\text{V}, T_A = 125^\circ\text{C}$ |
| I_{DSS} | Saturated drain-to-source current | - | 500 | - | mA | $V_{GS} = 0\text{V}, V_{DS} = 25\text{V}$ |
| $R_{DS(ON)}$ | Static drain-to-source ON-state resistance | - | - | 42 | Ω | $V_{GS} = 0\text{V}, I_D = 100\text{mA}$ |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.1 | %/ $^\circ\text{C}$ | $V_{GS} = 0\text{V}, I_D = 100\text{mA}$ |
| G_{FS} | Forward transconductance | 100 | - | - | mmho | $V_{DS} = 10\text{V}, I_D = 100\text{mA}$ |
| C_{ISS} | Input capacitance | - | - | 540 | pF | $V_{GS} = -10\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$ |
| C_{OSS} | Common source output capacitance | - | - | 60 | | |
| C_{RSS} | Reverse transfer capacitance | - | - | 25 | | |
| $t_{d(ON)}$ | Turn-ON delay time | - | - | 30 | ns | $V_{DD} = 25\text{V}, I_D = 100\text{mA}, R_{GEN} = 25\Omega$ |
| t_r | Rise time | - | - | 45 | | |
| $t_{d(OFF)}$ | Turn-OFF delay time | - | - | 45 | | |
| t_f | Fall time | - | - | 60 | | |
| V_{SD} | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS} = -5.0\text{V}, I_{SD} = 200\text{mA}$ |
| t_{rr} | Reverse recovery time | - | 800 | - | ns | $V_{GS} = -5.0\text{V}, I_{SD} = 200\text{mA}$ |

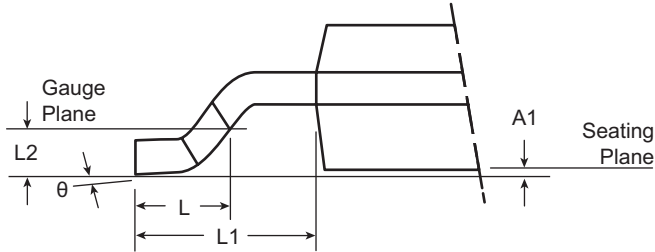
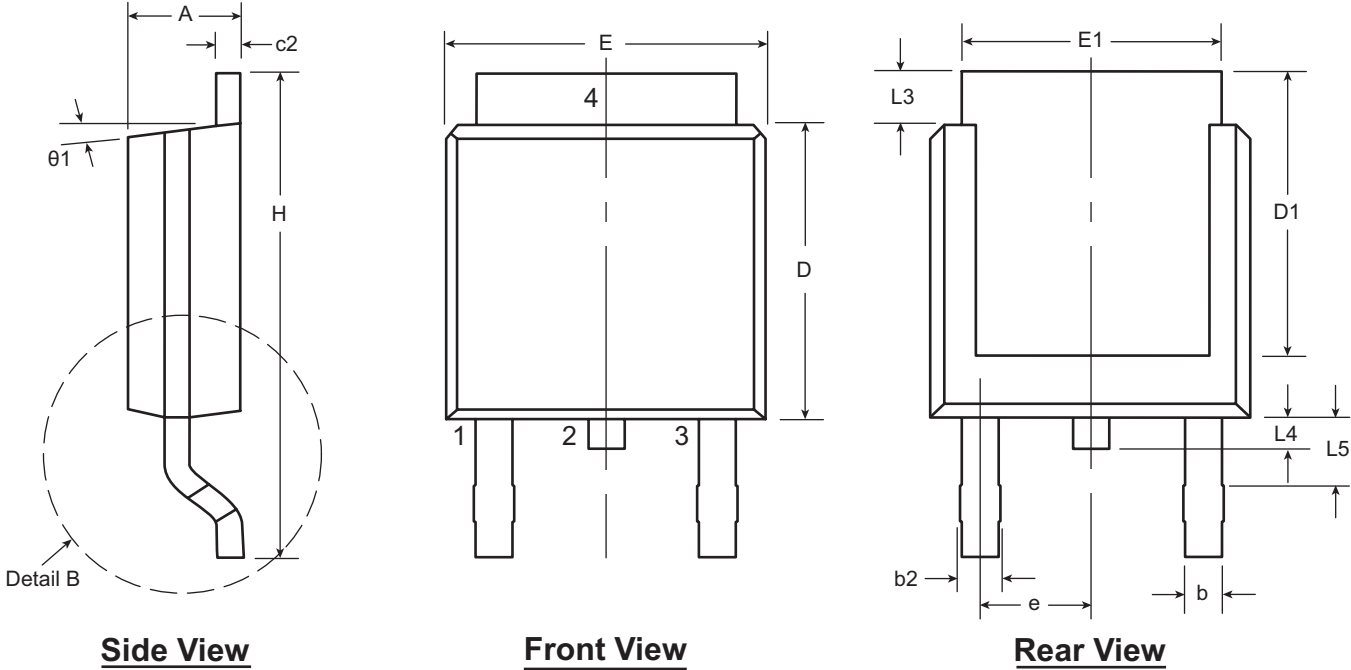
Notes:

- All D.C. parameters 100% tested at 25 $^\circ\text{C}$ unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



3-Lead TO-252 D-PAK Package Outline (K4)



Notes:

1. 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

| Symbol | A | A1 | b | b2 | c2 | D | D1 | E | E1 | e | H | L | L1 | L2 | L3 | L4 | L5 | θ | $\theta 1$ | | | |
|--------------------|-----|------|------|------|------|------|------|------|------|------|-------------|------|------|-------------|-------------|------|----|----------|------------|------|-----|-----|
| Dimension (inches) | MIN | .086 | - | .025 | .030 | .018 | .235 | .205 | .250 | .170 | .090 BSC | .370 | .055 | .108 REF | .020 BSC | .035 | - | .045 | 0° | 0° | | |
| | NOM | - | - | - | - | - | .240 | - | - | - | | - | .060 | | | - | - | - | - | - | - | - |
| | MAX | .094 | .005 | .035 | .045 | .035 | .245 | - | .265 | - | | .410 | .070 | | | - | - | .050 | .040 | .060 | 10° | 15° |

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
 Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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