

SPICE Device Model SUD50N02-09P Vishay Siliconix

N-Channel 20-V (D-S), 175°C MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- · Macro Model (Subcircuit Model)
- Level 3 MOS

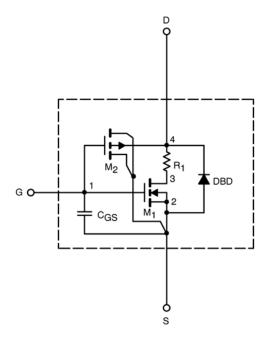
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Document Number: 72195 S-60543—Rev. B, 10-Apr-06

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			-		-
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.7		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	438		А
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.0078	0.008	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125°C	0.010		
		V _{GS} = 4.5 V, I _D = 20 A	0.0136	0.0135	
Forward Voltage ^a	V _{SD}	$I_F = 50 \text{ A}, V_{GS} = 0 \text{ V}$	0.91	1.1	V
Dynamic ^b			-		
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz	1212	1300	pF
Output Capacitance	C _{oss}		470	470	
Reverse Transfer Capacitance	C _{rss}		237	275	
Total Gate Charge ^c	Qg	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 50 A	10.6	10.5	nC
Gate-Source Charge ^c	Q_{gs}		4.2	4.2	
Gate-Drain Charge ^c	Q_{gd}		4	4	
Turn-On Delay Time ^c	t _{d(on)}	V_{DD} = 10 V, R_L = 0.20 Ω $I_D \cong 50$ A, V_{GEN} = 10 V, R_G = 2.5 Ω I_F = 50 A, di/dt = 100 A/ μ s	9	8	ns
Rise Time ^c	t _r		9	10	
Turn-Off Delay Time ^c	$t_{d(off)}$		32	25	
Fall Time ^c	t _f		10	12	
Source-Drain Reverse Recovery Time	t _{rr}		31	35	

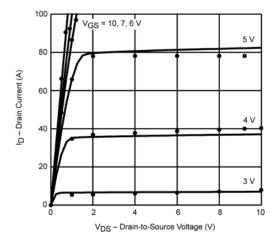
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing. c. Independent of operating temperature.

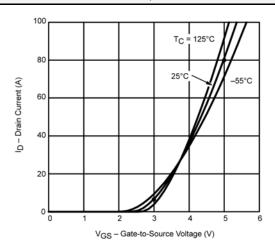


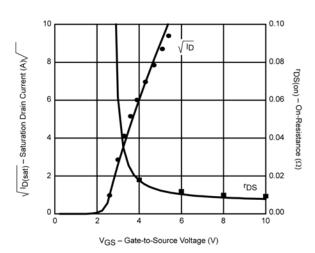
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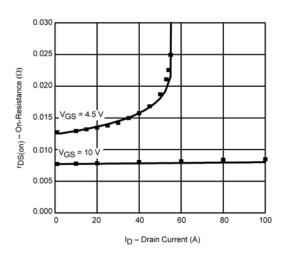
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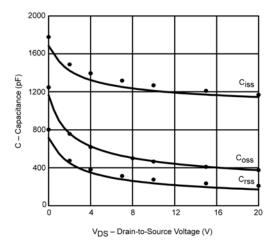
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

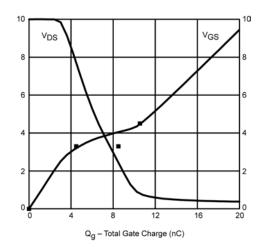












Note: Dots and squares represent measured data





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Revision: 18-Jul-08

Document Number: 91000 www.vishay.com