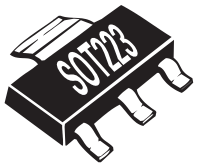
ZXM64N035G

35V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS}$ = 35V: $R_{DS(on)}$ = 0.050Ω: I_D = 6.7A

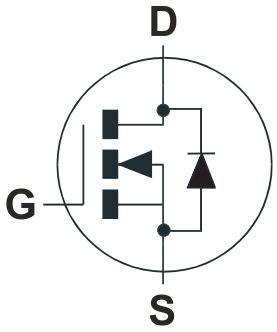


DESCRIPTION

This new generation of high cell density planar MOSFETs from Zetex utilises a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- SOT223 package

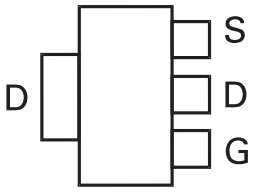


APPLICATIONS

- 50W Class D Audio Output Stage
- Motor Control

ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
ZXM64N035GTA	7”	12mm	1000 units
ZXM64N035GTC	13”	12mm	4000 units



Top View

DEVICE MARKING

- ZXM6
  4N035

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ZETEX SEMICONDUCTORS

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DSS}	35	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (V_{GS}=10V; T_A=25°C)[b] (V_{GS}=10V; T_A=70°C)[b] (V_{GS}=10V; T_A=25°C)[a]	I_D	6.7 5.4 4.8	A
Pulsed Drain Current [c]	I_{DM}	30	A
Continuous Source Current (Body Diode) [b]	I_S	2.4	A
Pulsed Source Current (Body Diode)[c]	I_{SM}	30	A
Power Dissipation at T_A=25°C [a] Linear Derating Factor	P_D	2.0 16	W mW/°C
Power Dissipation at T_A=25°C [b] Linear Derating Factor	P_D	3.9 31	W mW/°C
Operating and Storage Temperature Range	T_j:T_{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient [a]	$R_{\theta JA}$	62.5	°C/W
Junction to Ambient [b]	$R_{\theta JA}$	32	°C/W

NOTES

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions

(b) For a device surface mounted on FR4 PCB measured at t≤10 secs.

(c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.05 pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (at T_A = 25°C unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	35			V	I_D=250μA, V_{GS}=0V
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS}=35V, V_{GS}=0V
Gate-Body Leakage	I_{GSS}			100	nA	V_{GS}=±20V, V_{DS}=0V
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0			V	I_D=250μA, V_{DS}= V_{GS}
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.050 0.062	Ω Ω	V_{GS}=10V, I_D=3.7A V_{GS}=4.5V, I_D=1.9A
Forward Transconductance (1)(3)	g_{fs}	4.3			S	V_{DS}=10V,I_D=1.9A
DYNAMIC (3)						
Input Capacitance	C_{iss}		950		pF	V_{DS}=25V, V_{GS}=0V, f=1MHz
Output Capacitance	C_{oss}		200		pF	
Reverse Transfer Capacitance	C_{rss}		50		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		4.2		ns	V_{DD} =15V, I_D=3.7A R_G=6.0Ω, V_{GS}=10V
Rise Time	t_r		4.6		ns	
Turn-Off Delay Time	$t_{d(off)}$		20.5		ns	
Fall Time	t_f		8		ns	
Total Gate Charge	Q_g			27	nC	V_{DS}=24V,V_{GS}=10V, I_D=3.7A
Gate-Source Charge	Q_{gs}			5	nC	
Gate-Drain Charge	Q_{gd}			4.5	nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}			0.95	V	T_J=25°C, I_S=3.7A, V_{GS}=0V
Reverse Recovery Time (3)	t_{rr}		24.5		ns	T_J=25°C, I_F=3.7A, di/dt= 100A/μs
Reverse Recovery Charge (3)	Q_{rr}		19.1		nC	

NOTES
(1) Measured under pulsed conditions. Width=300μs. Duty cycle ≤ 2% .
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

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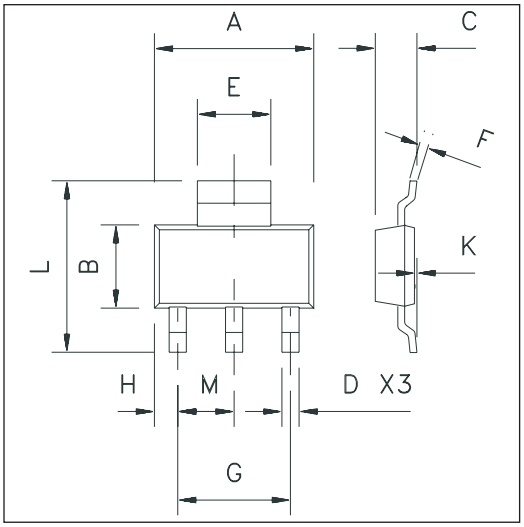
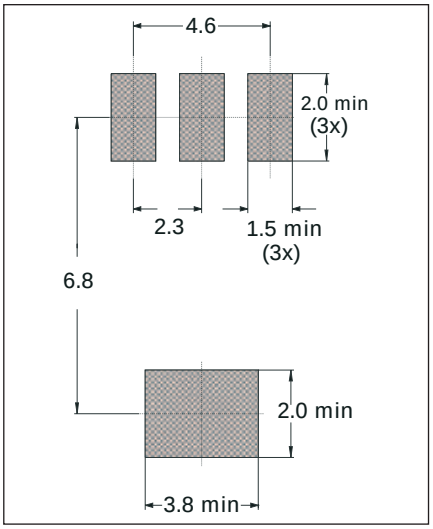
PACKAGE DIMENSIONS



PAD LAYOUT DETAILS



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	6.3	6.7	0.248	0.264
B	3.3	3.7	0.130	0.146
C	-	1.7	-	0.067
D	0.6	0.8	0.024	0.031
E	2.9	3.1	0.114	0.122
F	0.24	0.32	0.009	0.13
G	NOM 4.6		NOM 0.181	
H	0.85	1.05	0.033	0.041
K	0.02	0.10	0.0008	0.004
L	6.7	7.3	0.264	0.287
M	NOM 2.3		NOM 0.0905	

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