

30V SO8 Asymmetrical dual N-channel enhancement mode MOSFET

Summary

Device	V _{(BR)DSS}	Q _G (nC)	$R_{DS(on)}$ (Ω)	I _D (A)
Q1	30	12.9	0.024 @ V _{GS} = 10V	7.3
			0.039 @ V _{GS} = 4.5V	5.7
Q2	30	9	0.035 @ V _{GS} = 10V	6
			0.055 @ V _{GS} = 4.5V	4.8



Description

This new generation dual Trench MOSFET from Zetex features low on-resistance achievable with low (4.5V) gate drive.

Features

- · Low on-resistance
- 4.5V gate drive capability
- Low profile SOIC package

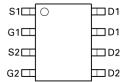
Applications

- DC-DC Converters
- SMPS
- · Load switching
- Motor control
- Backlighting

G2 G1 D1 D1 S2 S1 Q1 Q1

Ordering information

Device	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN3F318DN8TA	7	12	500



Device marking

ZXMN

Pinout – top view

3F318

ABSOLUTE MAXIMUM RATINGS

ABSOLUTE WAXIIVIOW RATINGS		-		
PARAMETER	SYMBOL	LIMIT	LIMIT	UNIT
		Q1	Q2	
Drain-Source Voltage	V_{DSS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current V _{GS} =10V; T _A =25°C (b)	I_D	7.3	6	Α
$V_{GS}=10V; T_{A}=70^{\circ}C$ (b)		5.9	4.8	
V_{GS} =10V; T_{A} =25°C (a)		5.7	4.6	
Pulsed Drain Current (c)	I _{DM}	33	25	Α
Continuous Source Current (Body Diode) (b)	I _S	3.5	3.3	Α
Pulsed Source Current (Body Diode) (c)	I _{SM}	33	25	Α
Power Dissipation at T _A =25°C (a) (d)	P_D	1.25		W
Linear Derating Factor		1	0	mW/°C
Power Dissipation at T _A =25°C (a) (e)	P_D	1.	.8	W
Linear Derating Factor		1	4	mW/°C
Power Dissipation at T _A =25°C (b) (d)	P _D	2	.1	W
Linear Derating Factor		1	7	mW/°C
Operating and Storage Temperature Range	T _j , T _{stg}	-55 to	+150	°C

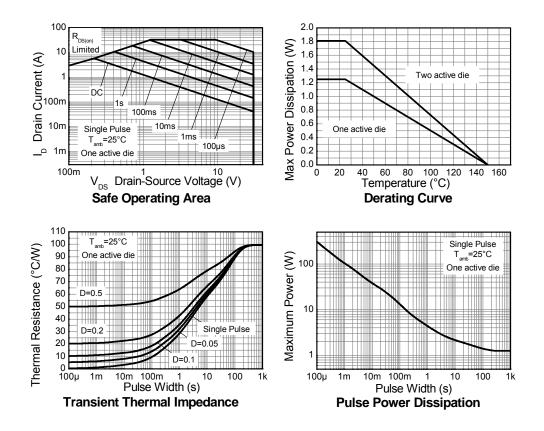
THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a) (d)	$R_{\theta JA}$	100	°C/W
Junction to Ambient (a) (e)	$R_{\theta JA}$	70	°C/W
Junction to Ambient (b) (d)	$R_{\theta JA}$	60	°C/W
Junction to Lead (f)	$R_{\theta JL}$	53	°C/W

NOTES

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at $t \le 10$ sec.
- (c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.02, pulse width 300us pulse width limited by maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at the end of the drain lead).

Q1 Thermal Characteristics



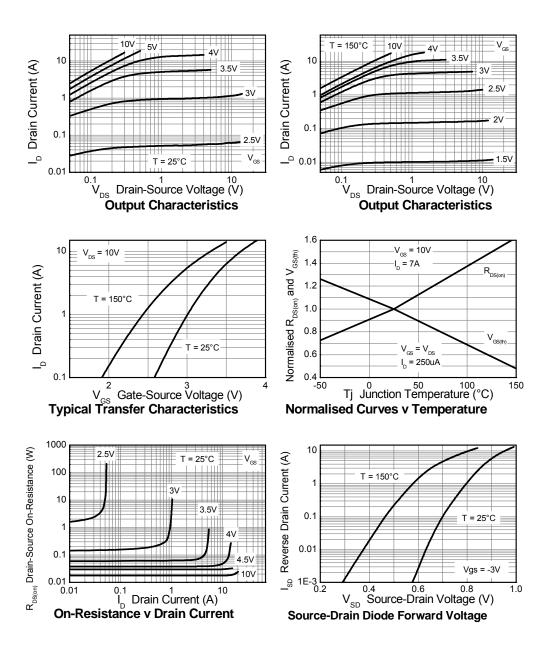
Q1 ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
STATIC							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	30			V	I _D = 250μA, V _G S=0V	
Zero Gate Voltage Drain Current	I _{DSS}			0.5	μА	V _{DS} = 30V, V _{GS} =0V	
Gate-Body Leakage	I _{GSS}			100	nA	VGS=±20V, VDS=0V	
Gate-Source Threshold Voltage	V _{GS(th)}	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.024	Ω	V _G S= 10V, I _D = 7.0A	
				0.039	Ω	VGS= 4.5V, ID = 6.0A	
Forward Transconductance (1) (3)	g _{fs}		16.5		S	V _{DS} = 15V, I _D = 7A	
DYNAMIC (3)							
Input Capacitance	C _{iss}		608		pF	V _{DS} = 15V, V _{GS} =0V	
Output Capacitance	Coss		132		pF	f=1MHz	
Reverse Transfer Capacitance	C _{rss}		71		pF		
SWITCHING (2) (3)							
Turn-On-Delay Time	$t_{d(on)}$		2.9		ns	V _{DD} = 15V, I _D = 1A	
Rise Time	t _r		3.3		ns	RG≅6.0Ω, VGS= 10V	
Turn-Off Delay Time	$t_{d(off)}$		16		ns		
Fall Time	t _f		8		ns		
Total Gate Charge	Q_{g}		12.9		nC	V _{DS} = 15V, V _{GS} = 10V	
Gate-Source Charge	Q_{gs}		2.5		nC	I _D = 7A	
Gate Drain Charge	Q_{gd}		2.52		nC		
SOURCE-DRAIN DIODE							
Diode Forward Voltage (1)	V _{SD}		0.82	1.2	٧	T _j =25°C, I _S = 1.7A, V _{GS} =0V	
Reverse Recovery Time (3)	t _{rr}		12		ns	T _j =25°C, I _S = 2.2A,	
Reverse Recovery Charge (3)	Q _{rr}		4.8		nC	di/dt=100A/μs	

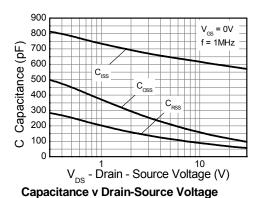
⁽¹⁾ Measured under pulsed conditions. Pulse width = $300\mu s$. Duty cycle $\leq 2\%$.

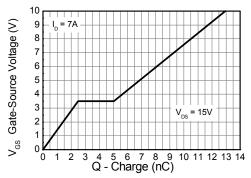
 ⁽²⁾ Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

Q1 Typical Characteristics



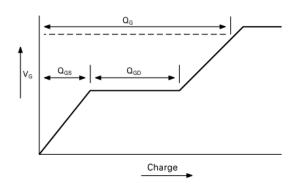
Q1 Typical Characteristics

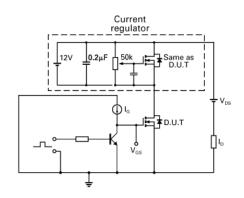




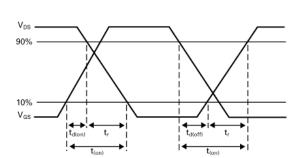
Gate-Source Voltage v Gate Charge

Test Circuits

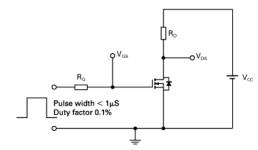




Basic gate charge waveform



Gate charge test circuit



Switching time waveforms

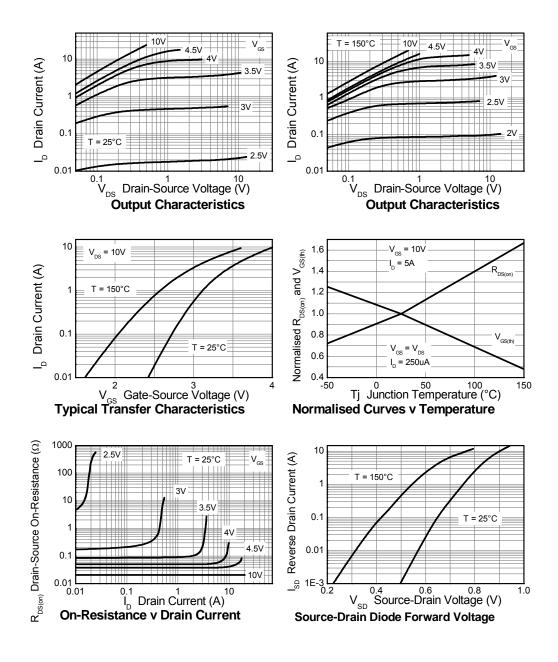
Switching time test circuit

Q2 ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise stated).

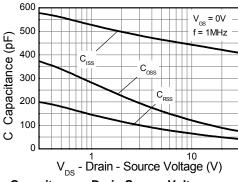
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Zero Gate Voltage Drain Current	I _{DSS}			0.5	μА	V _{DS} = 30V, V _{GS} =0V	
Gate-Body Leakage	I _{GSS}			100	nA	VGS=±20V, VDS=0V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0		3.0	V	I _D = 250μA, V _{DS} =V _{GS}	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.035	Ω	VGS= 10V, ID= 5.0A	
				0.055	Ω	VGS= 4.5V, ID = 4A	
Forward Transconductance (1) (3)	g _{fs}		11.8		S	V _{DS} = 15V, I _D = 5A	
DYNAMIC (3)							
Input Capacitance	C _{iss}		430		pF	V _{DS} = 15V, V _{GS} =0V f=1MHz	
Output Capacitance	Coss		101		pF		
Reverse Transfer Capacitance	C _{rss}		56		pF		
SWITCHING (2) (3)							
Turn-On-Delay Time	$t_{d(on)}$		2.5		ns	V _{DD} = 15V, I _D = 1A	
Rise Time	t _r		3.3		ns	RG≅6.0Ω, VGS= 10V	
Turn-Off Delay Time	$t_{d(off)}$		11.5		ns		
Fall Time	t _f		6.3		ns		
Total Gate Charge	Q_{g}		9		nC	V _{DS} = 15V, V _{GS} = 10V	
Gate-Source Charge	Q_{gs}		1.7		nC	I _D = 5A	
Gate Drain Charge	Q_{gd}		2		nC		
SOURCE-DRAIN DIODE							
Diode Forward Voltage (1)	V_{SD}		0.82	1.2	V	T _j =25°C, I _S = 1.7A, V _{GS} =0V	
Reverse Recovery Time (3)	t _{rr}		12		ns	Tj=25°C, IS= 2.1A,	
Reverse Recovery Charge (3)	Q_{rr}		4.9		nC	di/dt=100A/µs	

¹ Measured under pulsed conditions. Pulse width = $300\mu s$. Duty cycle $\leq 2\%$. 2 Switching characteristics are independent of operating junction temperature. 3 For design aid only, not subject to production testing.

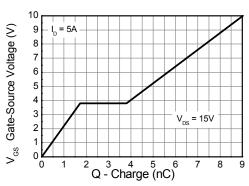
Q2 Typical Characteristics



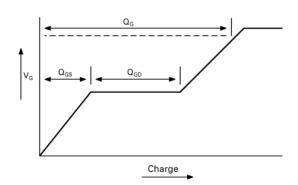
Q2 Typical Characteristics



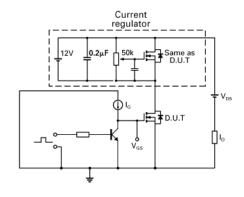
Capacitance v Drain-Source Voltage



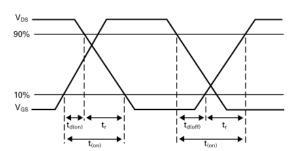
Gate-Source Voltage v Gate Charge



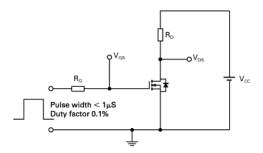
Basic gate charge waveform



Gate charge test circuit



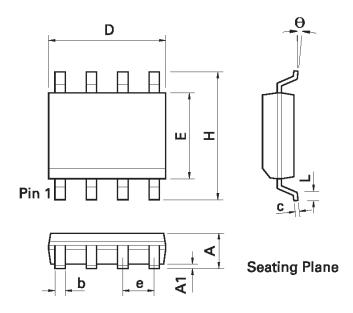
Switching time waveforms



Switching time test circuit

Packaging details - SO8

Package outline



DIM	Inc	hes	Millin	neters	DIM	Inc	hes	Millin	neters
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
Α	0.053	0.069	1.35	1.75	е	0.050	BSC	1.27	BSC
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	С	0.008	0.010	0.19	0.25
Н	0.228	0.244	5.80	6.20	θ	0°	8°	0°	8°
Е	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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