FAIRCHILD

SEMICONDUCTOR®

January 2007

FDMC2523P
P-Channel QFET®

-150V, -3A, 1.5Ω

Features

- Max $r_{DS(on)}$ = 1.5Ω at V_{GS} = -10V, I_D = -1.5A
- Low Crss (typical 10pF)
- Fast Switching
- Low gate charge (typical 6.2 nC)
- Improved dv / dt capability
- RoHS Compliant

General Description

These P-Channel MOSFET enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

Application

- Active Clamp Switch

Bottom   **Top**
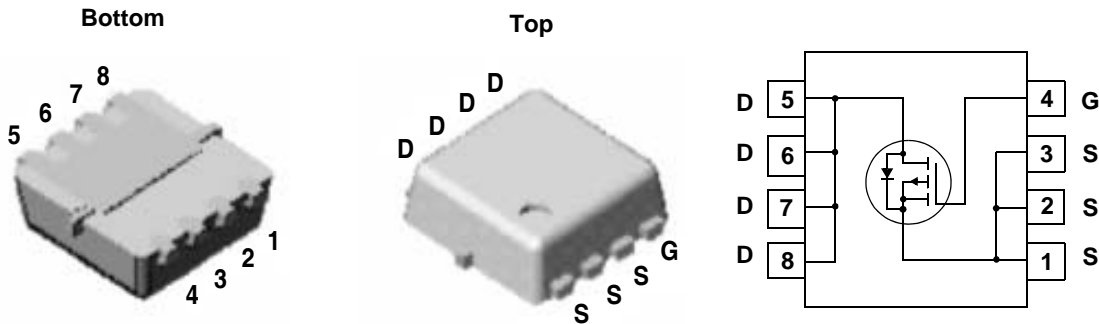
Power 33

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-150	V
V_{GS}	Gate to Source Voltage			±30	V
I_D	Drain Current -Continuous	T_C = 25°C		-3	A
	-Continuous	T_C = 100°C		-1.8	
	-Pulsed			-12	
P_D	Power Dissipation (Steady State)	T_C = 25°C		42	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds			300	°C
dv/dt	Peak Diode Recovery dv/dt		(Note 2)	-5	V/ns

Thermal Characteristics

$R_{θJC}$	Thermal Resistance, Junction to Case	(Note 1)	3.0	°C/W
$R_{θJA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	60	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC2523P	FDMC2523P	Power 33	7"	8mm	3000 units

1

www.fairchildsemi.com

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250µA, V_{GS} = 0V	-150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		-138		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -150V, V_{GS} = 0V			-1	µA
		T_J = 125°C			-10	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±30V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250µA	-3	-3.8	-5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250µA, referenced to 25°C		6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10V, I_D = -1.5A		1.1	1.5	Ω
		V_{GS} = -10V, I_D = -1.5A , T_J = 125°C		2.0	3.6	
g_{FS}	Forward Transconductance	V_{DS} = -40V, I_D = -1.5A (Note 4)		1.4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		200	270	pF
C_{oss}	Output Capacitance			60	80	pF
C_{rss}	Reverse Transfer Capacitance			10	15	pF
R_g	Gate Resistance	f = 1MHz		7.5		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -75V, I_D = -3A V_{GS} = -10V, R_{GEN} = 25Ω (Note 3,4)		15	27	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
t_f	Fall Time			13	24	ns
Q_g	Total Gate Charge	V_{GS} = -10V V_{DD} = -75V I_D = -3A (Note 3,4)		6.2	9	nC
Q_{gs}	Gate to Source Gate Charge			1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			3.3		nC
Drain-Source Diode Characteristics						
I_S	Maximum continuous Drain - Source Diode Forward Current				-3	A
I_{SM}	Maximum Pulse Drain - Source Doide Forward Current				-12	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = -3.0A		-1.8	-5	V
t_{rr}	Reverse Recovery Time	I_F = -3.0A, di/dt = 100A/µs		93		ns
Q_{rr}	Reverse Recovery Charge	(Note 3)		0.27		nC

Notes:
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to- ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
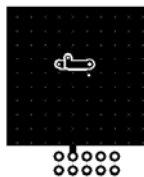
a. 60°C/W when mounted on a 1 in^2 pad of 2 oz copper

b.135°C/W when mounted on a minimum pad of 2 oz copper

2: $I_{SD} \leq$ -3A, dI/dt $\leq$ 300A/us, $V_{DD} \leq B_{VDSS}$, Starting T_J = 25°C
3: Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.
4: Essentially independent of operating temperature.

Typical Characteristics T_J = 25°C unless otherwise noted
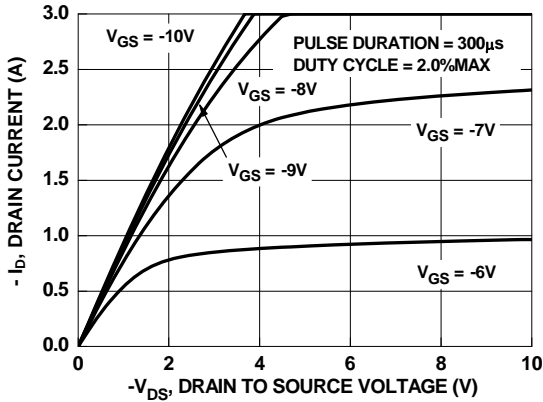

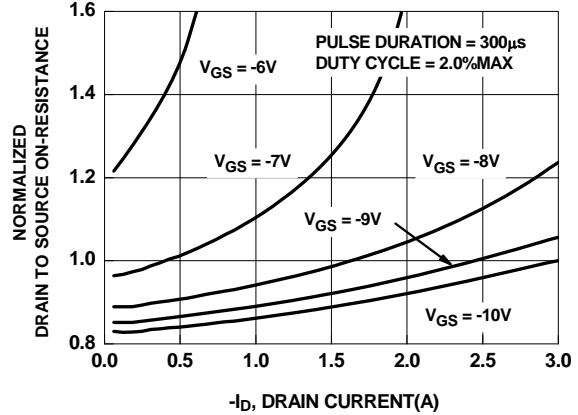**Figure 1. On-Region Characteristics**

Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage
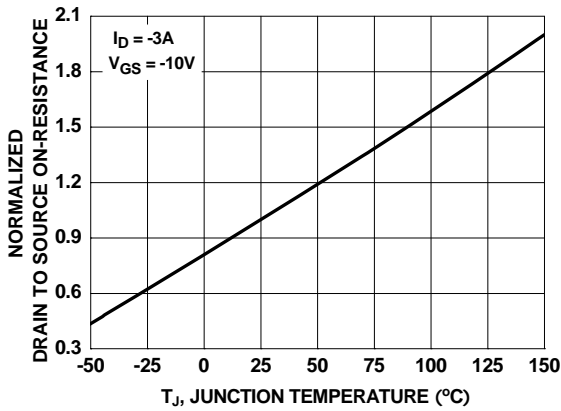

Figure 3. Normalized On-Resistance vs Junction Temperature
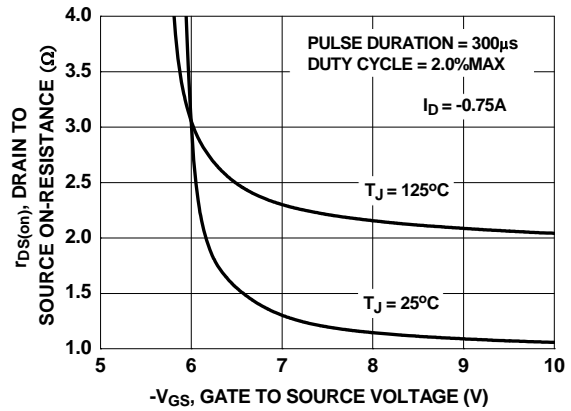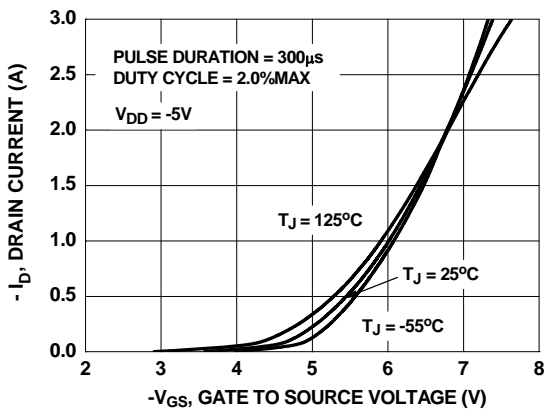

Figure 4. On-Resistance vs Gate to Source Voltage

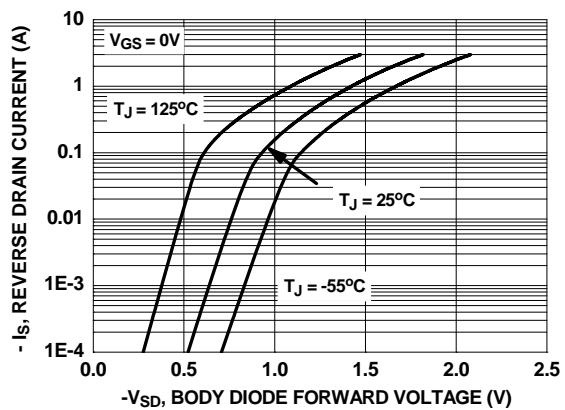
Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

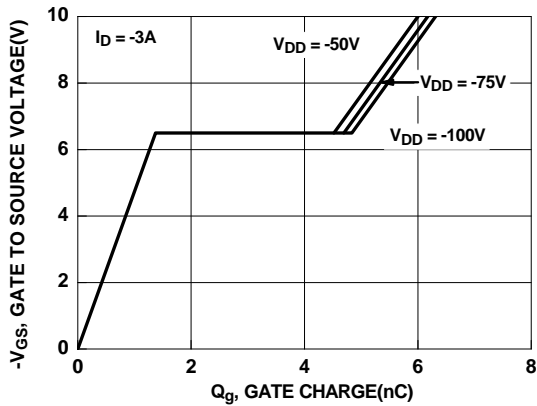## Typical Characteristics T_J = 25°C unless otherwise noted

Figure 7. Gate Charge Characteristics

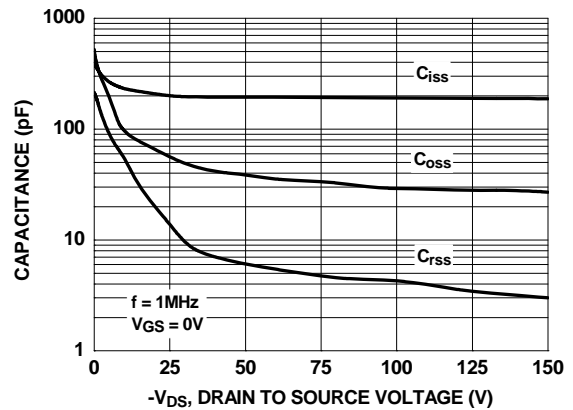I_D = -3A, V_{DD} = -50V, V_{DD} = -75V, V_{DD} = -100V

-V_{GS}, GATE TO SOURCE VOLTAGE(V) vs Q_g, GATE CHARGE(nC)

Figure 8. Capacitance vs Drain to Source Voltage

C_{iss}, C_{oss}, C_{rss}

f = 1MHz, V_{GS} = 0V

CAPACITANCE (pF) vs -V_{DS}, DRAIN TO SOURCE VOLTAGE (V)
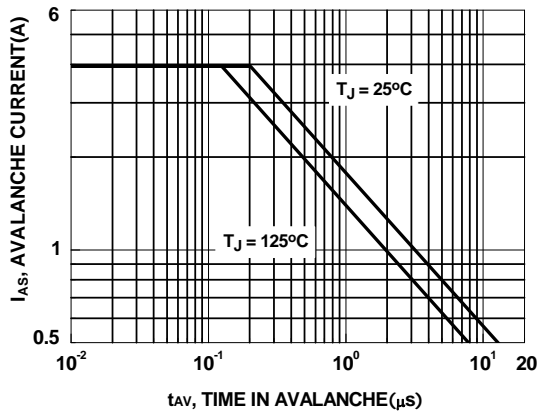
Figure 9. Unclamped Inductive Switching Capability

T_J = 25°C, T_J = 125°C

I_{AS}, AVALANCHE CURRENT(A) vs t_{AV}, TIME IN AVALANCHE(µs)
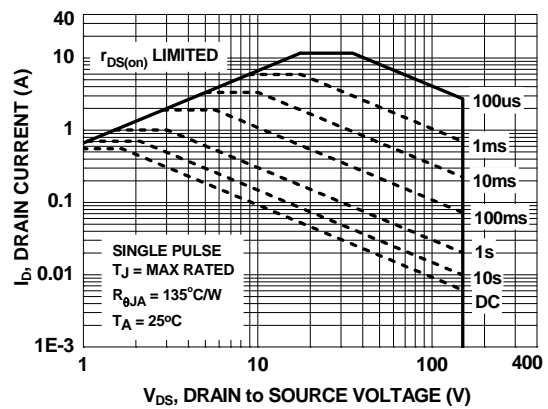
Figure 10. Forward Bias Safe Operating Area

$r_{DS(on)}$ LIMITED

100us, 1ms, 10ms, 100ms, 1s, 10s, DC

SINGLE PULSE
T_J = MAX RATED
$R_{\theta JA}$ = 135°C/W
T_A = 25°C

I_D, DRAIN CURRENT (A) vs V_{DS}, DRAIN to SOURCE VOLTAGE (V)
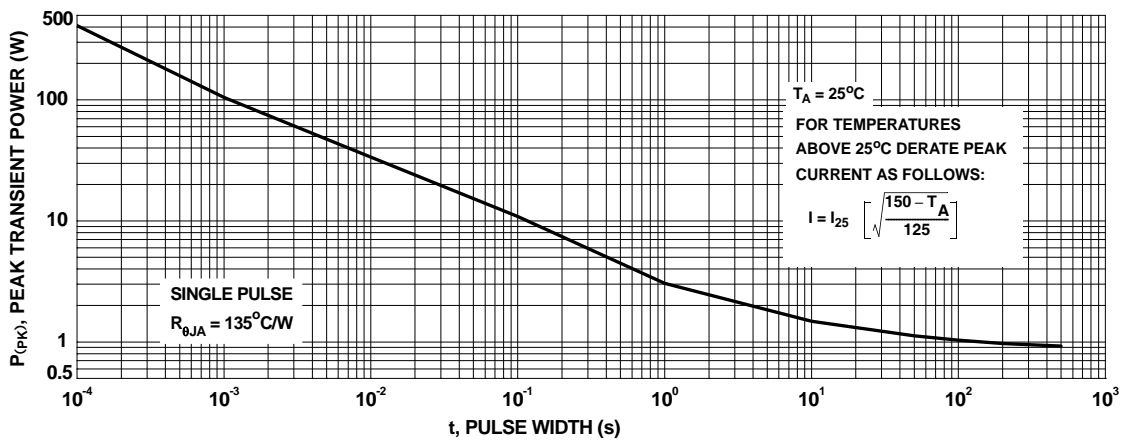
Figure 11. Single Pulse Maximum Power Dissipation

T_A = 25°C

FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$$I = I_{25} \left[\sqrt{\frac{150 - T_A}{125}} \right]$$

SINGLE PULSE
$R_{\theta JA}$ = 135°C/W

$P_{(PK)}$, PEAK TRANSIENT POWER (W) vs t, PULSE WIDTH (s)

Typical Characteristics $T_J = 25°C$ unless otherwise noted
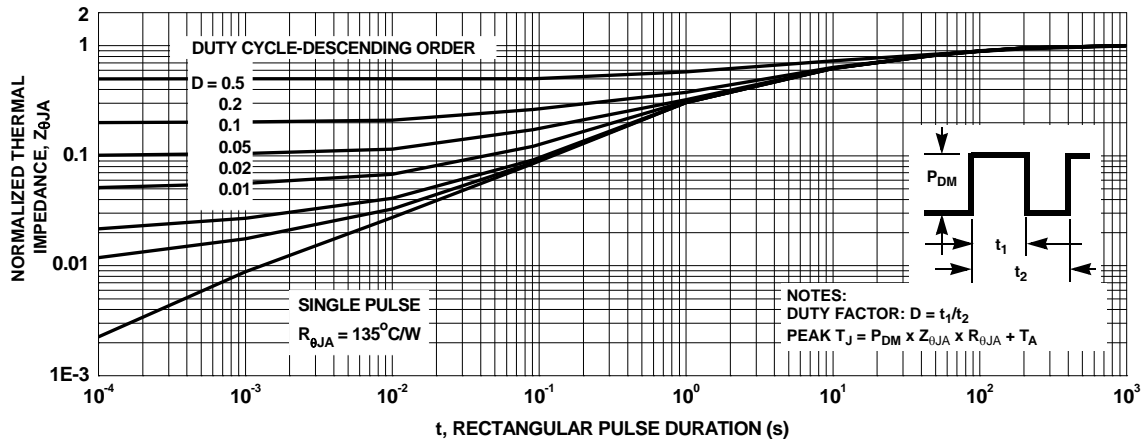
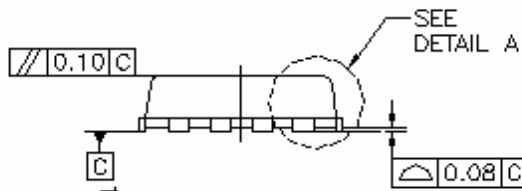**Figure 12. Transient Thermal Response Curve**

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

t, RECTANGULAR PULSE DURATION (s)

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

SINGLE PULSE

$R_{\theta JA} = 135°C/W$

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$

3.00±0.10 A

PKG ℄

8   5   B

PKG ℄

3.00±0.10

(0.37) 1   4

0.32±0.05

0.65

1.95

⊕ 0.10 A B

// 0.10 C

SEE
DETAIL A

C

1.50±0.10

△ 0.08 C

(2.27)

(0.30)
(0.10)

1   4

(0.20)

PKG ℄

3.20±0.15

8   5

3.20±0.15

(0.35)

2.37 MIN

SYM ℄

(0.45)

8   5

(0.40)

2.15 MIN

3.50

(0.85)

1

4

0.65

0.42 MIN

1.95

LAND PATTERN
RECOMMENDATION

NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE
AS OF 29 JUNE 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS
OR MOLD FLASH.
D) DIMENSIONING AND TOLERANCING PER
ASME Y14.5M-1994.

1.00
0.85

0.80
0.65

SEATING
PLANE

0.20±0.025

0.05
0.00

DETAIL A
SCALE: 48:1

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	VCX™
Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I^{2}C™	PACMAN™	SuperFET™	
CROSSVOLT™	i-Lo™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^{2}CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I22