

Voltage Detectors, Delay Circuit Built-In

■ GENERAL DESCRIPTION

The XC61F series are highly accurate, low power consumption voltage detectors, manufactured using CMOS and laser trimming technologies. A delay circuit is built-in to each detector.

Detect voltage is extremely accurate with minimal temperature drift.

Both CMOS and N-channel open drain output configurations are available.

Since the delay circuit is built-in, peripherals are unnecessary and high density mounting is possible.

■ APPLICATIONS

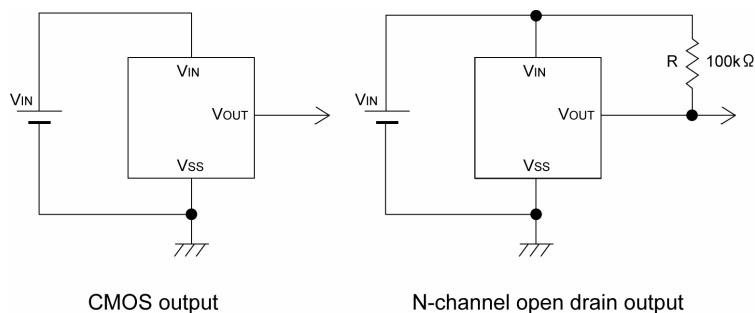
- Microprocessor reset circuitry
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure detection
- System battery life and charge voltage monitors
- Delay circuitry

■ FEATURES

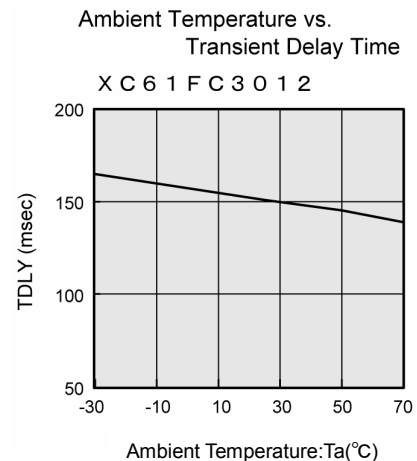
- Highly Accurate** : $\pm 2\%$
- Low Power Consumption** : $1.0 \mu\text{A}$ (TYP.) [$V_{\text{IN}}=2.0\text{V}$]
- Detect Voltage Range** : 1.6V ~ 6.0V in 100mV increments
- Operating Voltage Range** : 0.7V ~ 10.0V
- Detect Voltage Temperature Characteristics** : $\pm 100\text{ppm}/^\circ\text{C}$ (TYP.)
- Built-In Delay Circuit** : ① 1ms ~ 50ms
② 50ms ~ 200ms
③ 80ms ~ 400ms
- Output Configuration** : N-channel open drain or CMOS
- CMOS**
- Mini Mold Package**
- Ultra Small Packages** : SOT-23 (150mW) mini-mold
: SOT-89 (500mW) mini-power mold
: TO-92 (300mW)

* No parts are available with an accuracy of $\pm 1\%$

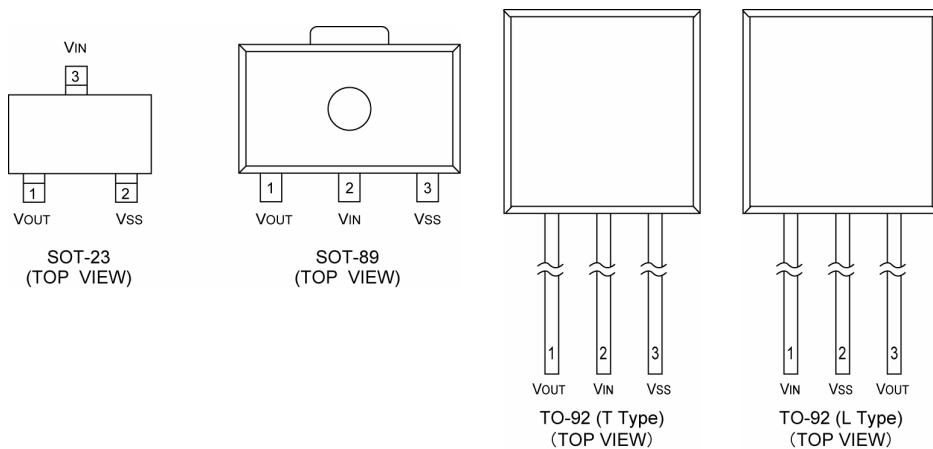
■ TYPICAL APPLICATION CIRCUITS



■ TYPICAL PERFORMANCE CHARACTERISTICS



PIN CONFIGURATION



PIN ASSIGNMENT

PIN NUMBER				PIN NAME	FUNCTION
SOT-23	SOT-89	TO-92 (T)	TO-92 (L)		
3	2	2	1	V _{IN}	Supply Voltage Input
2	3	3	2	V _{SS}	Ground
1	1	1	3	V _{OUT}	Output

PRODUCT CLASSIFICATION

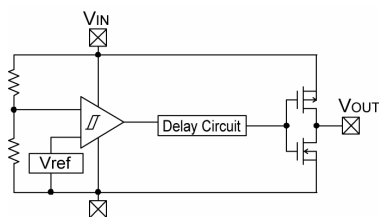
Ordering Information

XC61F ①②③④⑤⑥⑦

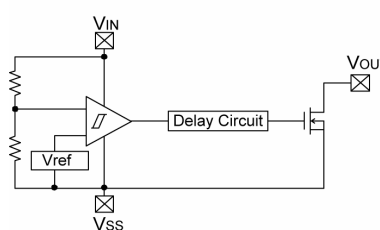
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	C	: CMOS output
		N	: N-ch open drain output
② ③	Detect Voltage	16 ~ 60	: e.g. 2.5V → ②2, ③5
			: e.g. 3.8V → ②3, ③8
④	Output Delay	1	: 50ms ~ 200ms
		4	: 80ms ~ 400ms
		5	: 1ms ~ 50ms
⑤	Detect Accuracy	2	: Within ± 2.0%
⑥	Package	M	: SOT-23
		P	: SOT-89
		T	: TO-92 (Standard)
		L	: TO-92 (Custom pin configuration)
⑦	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed
		H	: Paper type (TO-92)
		B	: Bag (TO-92)

■ BLOCK DIAGRAMS

(1) CMOS output



(2) N-channel open drain output



■ ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

PARAMETER	SYMBOL	RATINGS	UNITS
Input Voltage	V _{IN}	12.0	V
Output Current	I _{OUT}	50	mA
Output Voltage	CMOS	V _{SS} -0.3 ~ V _{IN} + 0.3	V
	N-ch open drain	V _{SS} -0.3 ~ 9	
Power Dissipation	SOT-23	150	mW
	SOT-89	500	
	TO-92	300	
Operating Temperature Range	Topr	-30 ~ +85	°C
Storage Temperature Range	Tstg	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	
Detect Voltage	V _{DF}		V _{DF(T)} x 0.98	V _{DF(T)}	V _{DF(T)} x 1.02	V	
Hysteresis Range	V _{HYS}		V _{DF} x 0.02	V _{DF} x 0.05	V _{DF} x 0.08	V	
Supply Current	I _{SS}	V _{IN} = 1.5V	-	0.9	2.6	μA	
		V _{IN} = 2.0V	-	1.0	3.0		
		V _{IN} = 3.0V	-	1.3	3.4		
		V _{IN} = 4.0V	-	1.6	3.8		
		V _{IN} = 5.0V	-	2.0	4.2		
Operating Voltage	V _{IN}	V _{DF} = 1.6V to 6.0V	0.7	-	10.0	V	
Output Current	I _{OUT}	N-ch V _{DF} = 0.5V	V _{IN} = 1.0V	-	2.2	-	mA
			V _{IN} = 2.0V	-	7.7	-	
			V _{IN} = 3.0V	-	10.1	-	
			V _{IN} = 4.0V	-	11.5	-	
			V _{IN} = 5.0V	-	13.0	-	
		CMOS, P-ch V _{DF} = 2.1V	V _{IN} = 8.0V	-	-10.0	-	
Detect Voltage Temperature Characteristics	$\frac{\Delta V_{DF}}{\Delta T_{opr} \cdot V_{DF}}$		-	±100	-	ppm/°C	
Transient Delay Time (V _{DR} → V _{OUT} inversion)	T _{DLY} *	V _{IN} changes from 0.6V to 10V	50	-	200	ms	

V_{DF} (T): Setting detect voltage value

Release Voltage: V_{DR} = V_{DF} + V_{HYS}

* Transient Delay Time: 1ms to 50ms & 80ms to 400ms versions are also available.

Note: The power consumption during power-start to output being stable (release operation) is 2 μA greater than it is after that period (completion of release operation) because of delay circuit through current.

OPERATIONAL EXPLANATION

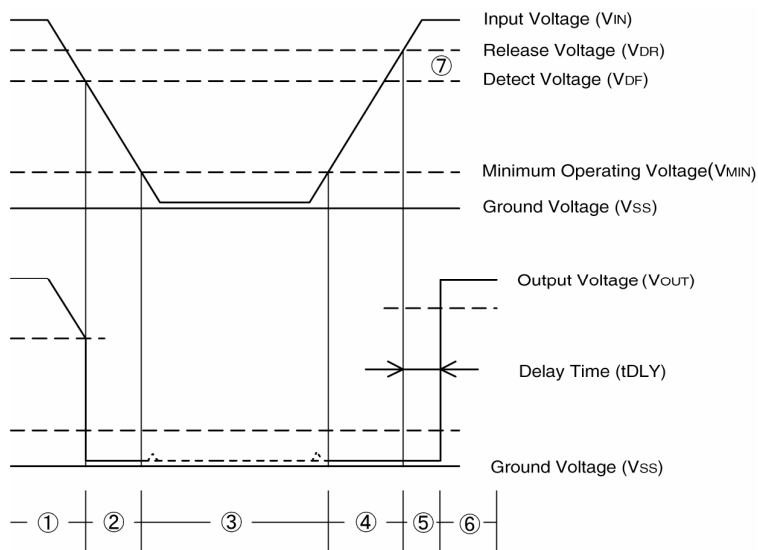
CMOS output

- ① When a voltage higher than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN}), the voltage will gradually fall. When a voltage higher than the detect voltage (V_{DF}) is applied to V_{IN} , output (V_{OUT}) will be equal to the input at V_{IN} .
Note that high impedance exists at V_{OUT} with the N-channel open drain configuration. If the pin is pulled up, V_{OUT} will be equal to the pull up voltage.
- ② When V_{IN} falls below V_{DF} , V_{OUT} will be equal to the ground voltage (V_{SS}) level (detect state). Note that this also applies to N-channel open drain configurations.
- ③ When V_{IN} falls to a level below that of the minimum operating voltage (V_{MIN}) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.
- ④ When V_{IN} rises above the V_{SS} level (excepting levels lower than minimum operating voltage), V_{OUT} will be equal to V_{SS} until V_{IN} reaches the V_{DR} level.
- ⑤ Although V_{IN} will rise to a level higher than V_{DR} , V_{OUT} maintains ground voltage level via the delay circuit.
- ⑥ Following transient delay time, V_{IN} will be output at V_{OUT} . Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:

1. The difference between V_{DR} and V_{DF} represents the hysteresis range.
2. Propagation delay time (tDLY) represents the time it takes for V_{IN} to appear at V_{OUT} once the said voltage has exceeded the V_{DR} level.

Timing Chart



■ DIRECTIONS FOR USE

● Notes on Use

1. Please use this IC within the stated maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current (I_{OUT}) exists. It is therefore recommend that no resistor be added. (refer to Oscillation Description (1) below)
3. When a resistor is connected between the V_{IN} pin and the input with CMOS output configurations, irrespective of N-ch output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current (I_{OUT}) does not exist. (refer to Oscillation Description (2) below)
4. With a resistor connected between the V_{IN} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN} pin.
5. If a resistor (R_{IN}) must be used, then please use with as small a level of input impedance as possible in order to control the occurrences of oscillation as described above.

Further, please ensure that R_{IN} is less than $10k\Omega$ and that C_{IN} is more than $0.1\mu F$ (Figure 1). In such cases, detect and release voltages will rise due to voltage drops at R_{IN} brought about by the IC's supply current.

● Oscillation Description

- (1) Oscillation as a result of output current with the CMOS output configuration:

When the voltage applied at IN rises, release operations commence and the detector's output voltage increases. Load current (I_{OUT}) will flow through R_L . Because a voltage drop ($R_{IN} \times I_{OUT}$) is produced at the R_{IN} resistor, located between the input (IN) and the V_{IN} pin, the load current will flow via the IC's V_{IN} pin. The voltage drop will also lead to a fall in the voltage level at the V_{IN} pin. When the V_{IN} pin voltage level falls below the detect voltage level, detect operations will commence. Following detect operations, load current flow will cease and since voltage drop at R_{IN} will disappear, the voltage level at the V_{IN} pin will rise and release operations will begin over again.

Oscillation may occur with this "release - detect - release" repetition.

Further, this condition will also appear via means of a similar mechanism during detect operations.

- (2) Oscillation as a result of through current:

Since the XC61F series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur during release voltage operations as a result of output current which is influenced by this through current (Figure 3).

Since hysteresis exists during detect operations, oscillation is unlikely to occur.

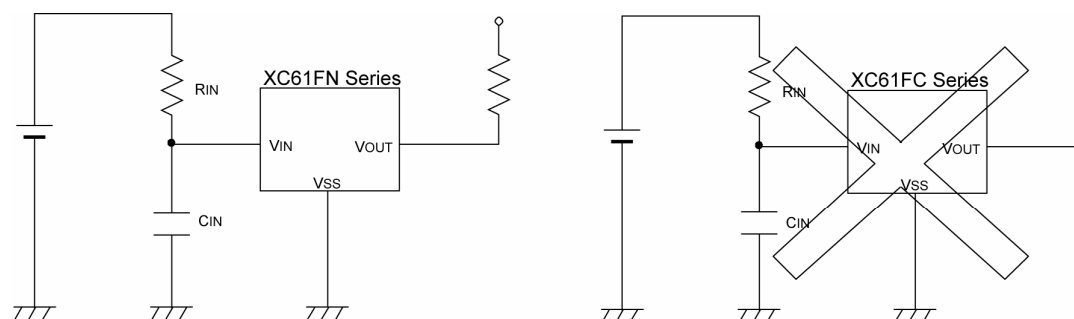


Figure 1. When using an input resistor

■ DIRECTIONS FOR USE (Continued)

● Oscillation Description (Continued)

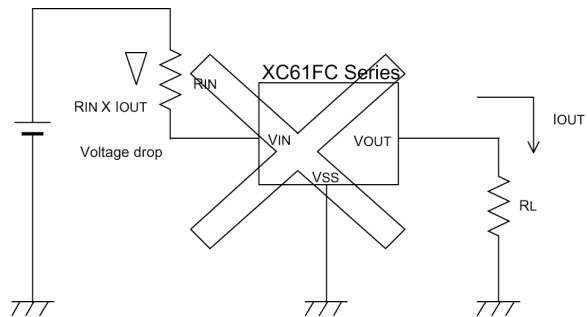


Figure 2. Oscillation in relation to output current

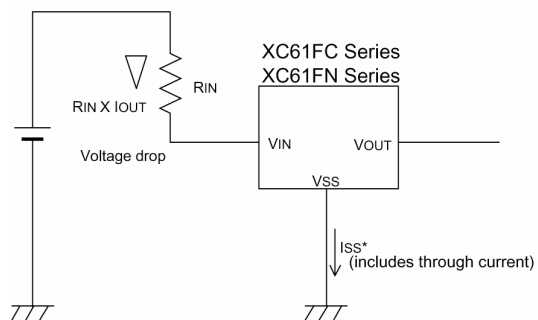
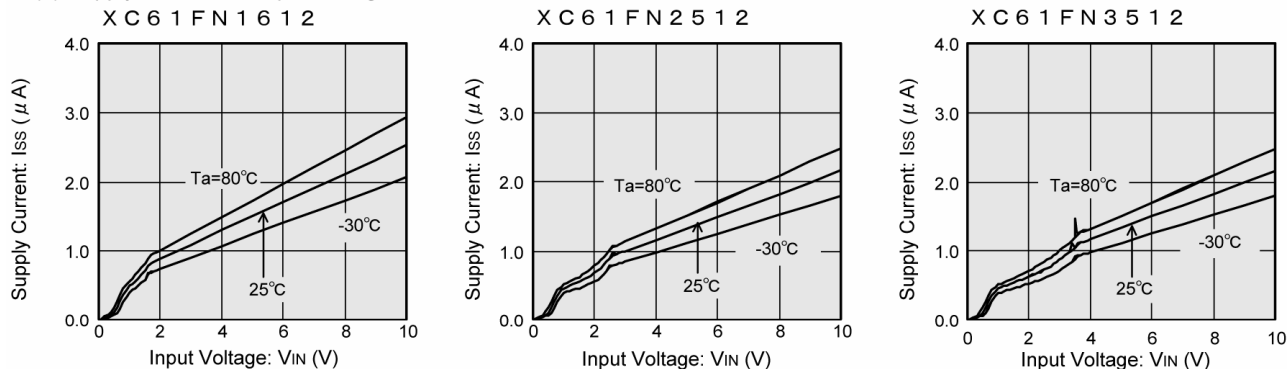


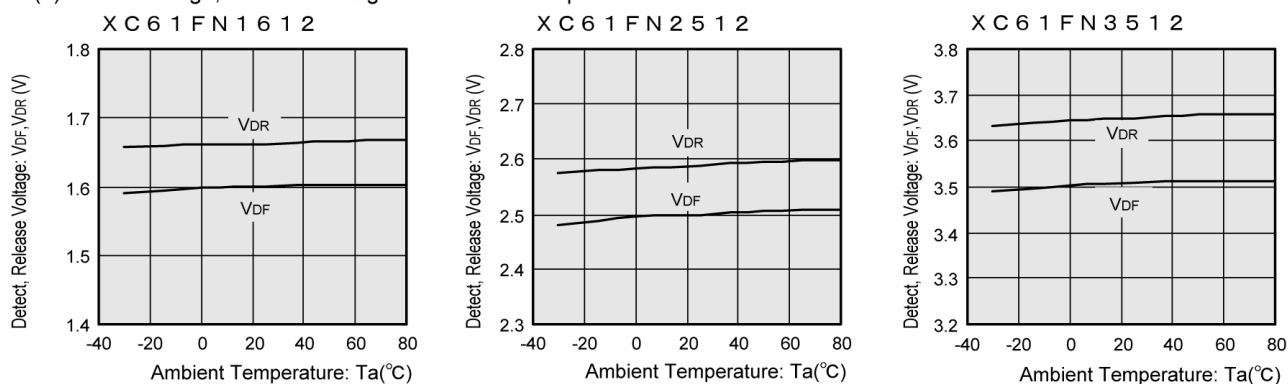
Figure 3. Oscillation in relation to through current

TYPICAL PERFORMANCE CHARACTERISTICS

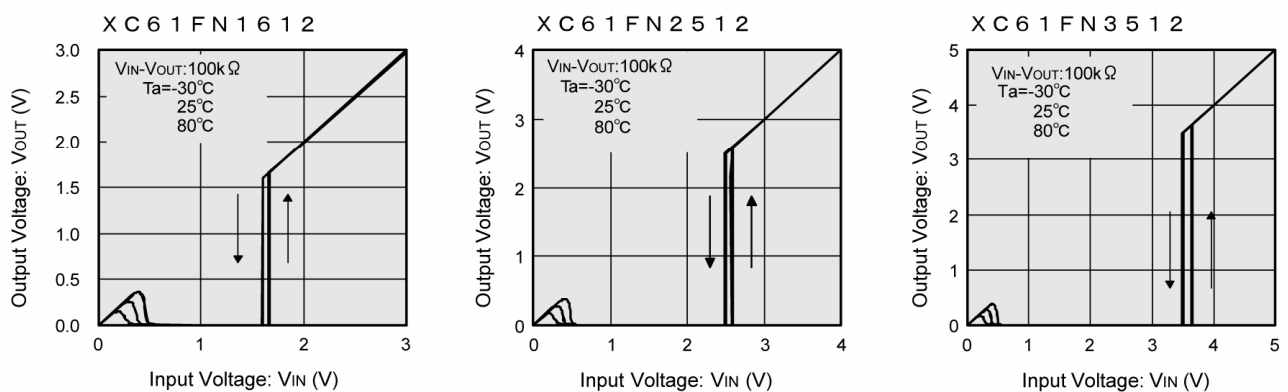
(1) Supply Current vs. Input Voltage



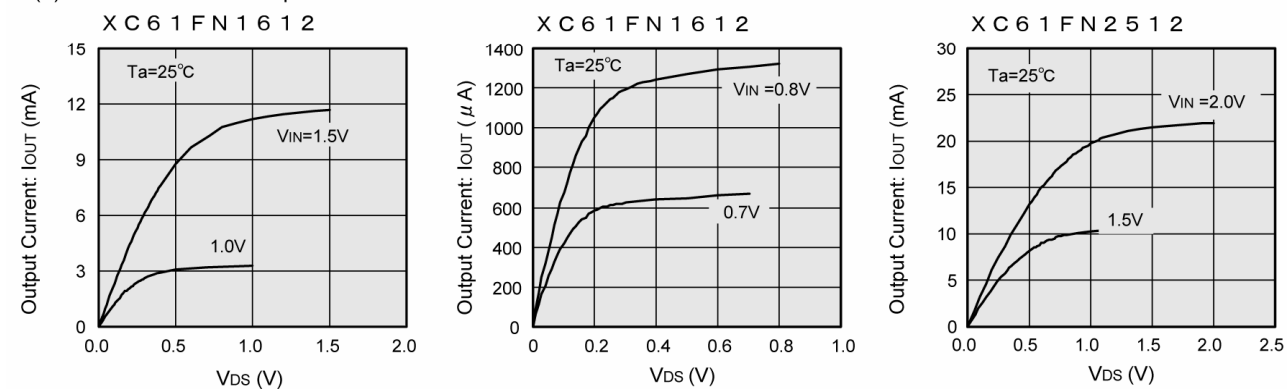
(2) Detect Voltage, Release Voltage vs. Ambient Temperature



(3) Output Voltage vs. Input Voltage

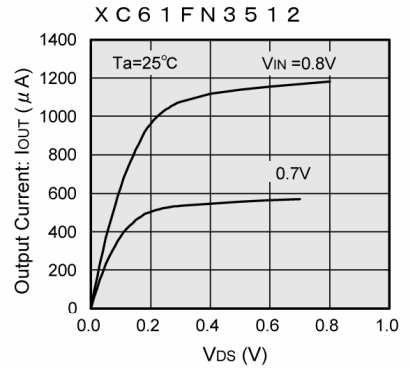
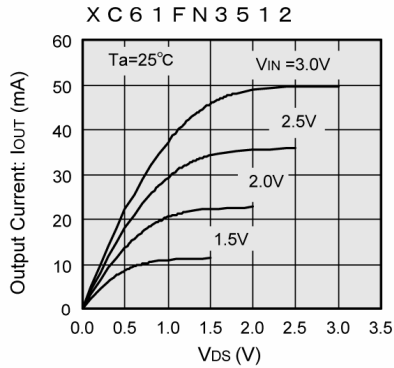
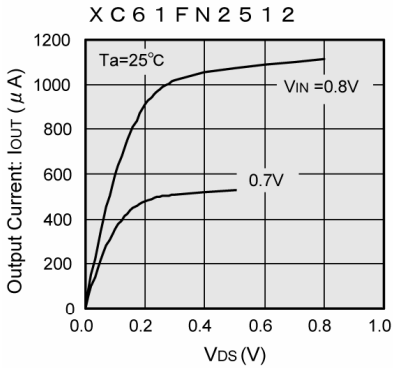


(4) N-Channel Driver Output Current vs. VDS

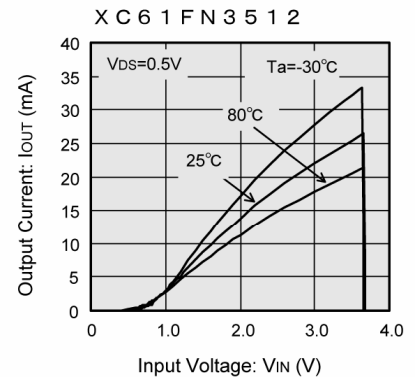
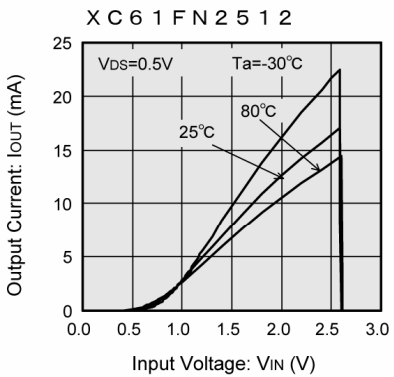
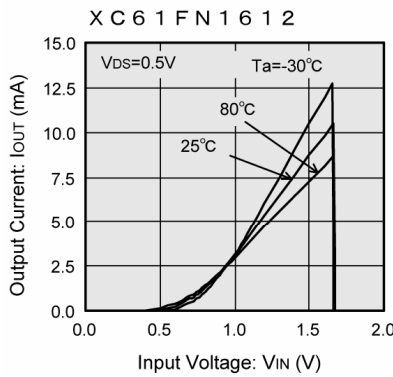


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

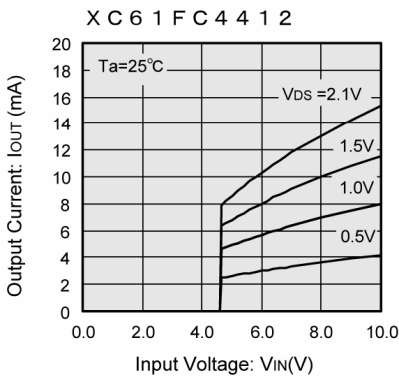
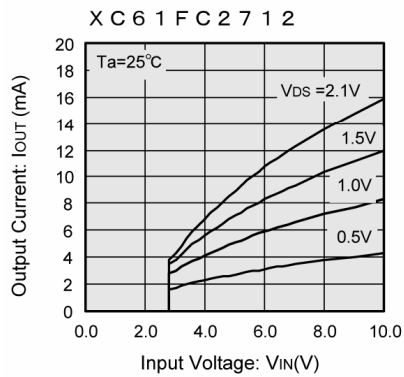
(4) N-Channel Driver Output Current vs. V_{DS} (Continued)



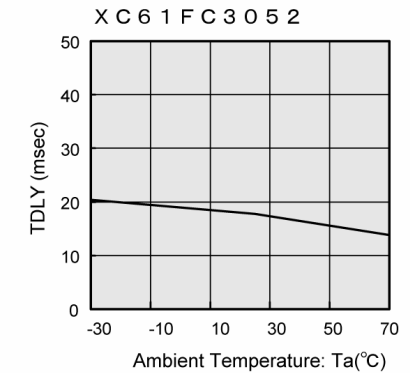
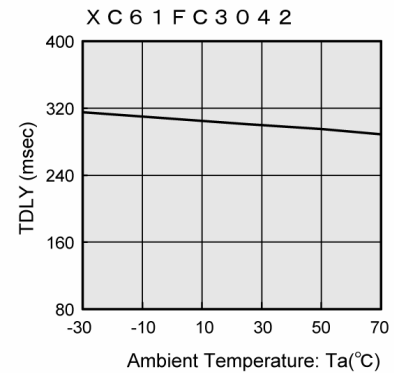
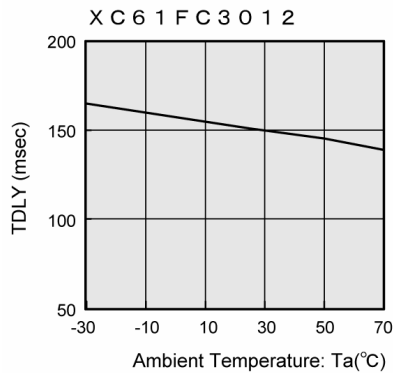
(5) N-Channel Driver Output Current vs. Input Voltage



(6) P-Channel Driver Output Current vs. Input Voltage

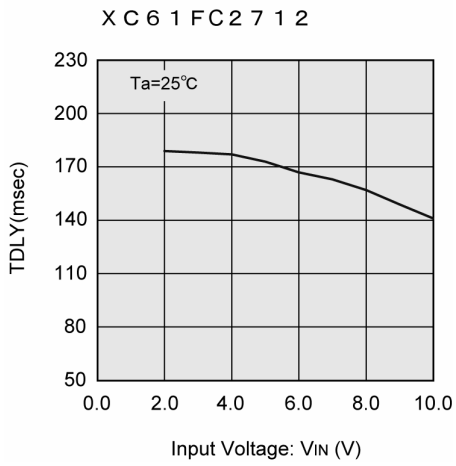


(7) Ambient Temperature vs. Transient Delay Time



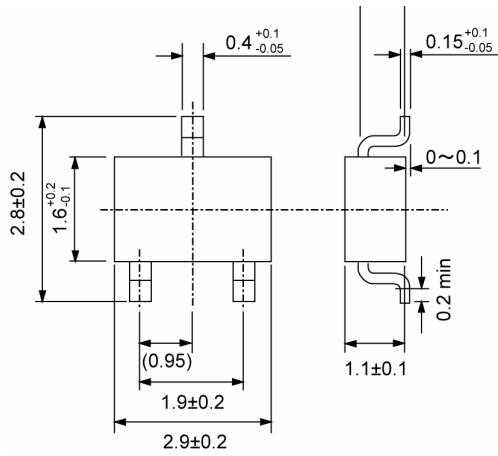
■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(8) Input Voltage vs. Transient Delay Time

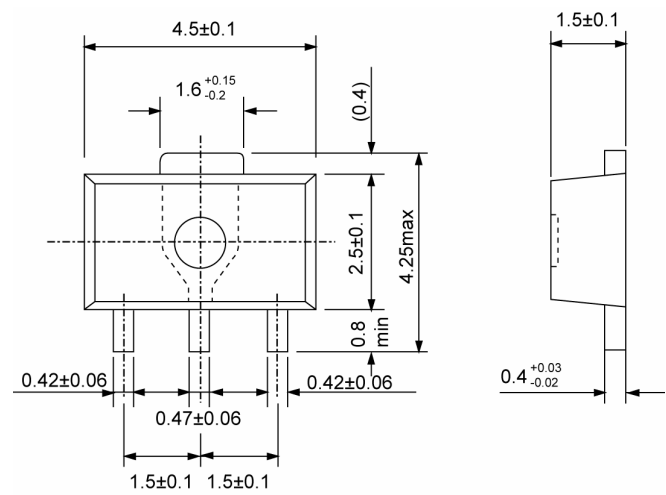


PACKAGING INFORMATION

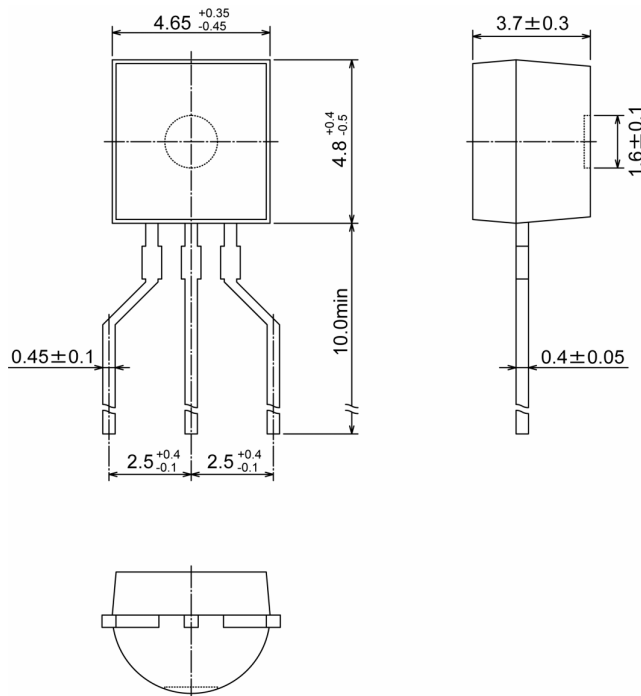
● SOT-23



● SOT-89

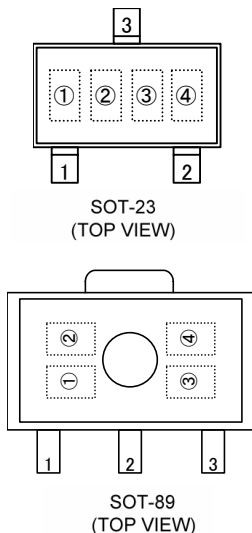


● TO-92



MARKING RULE

● SOT-23, SOT-89



① Represents integer of detect voltage and output configuration
CMOS output (XC61FC series)

MARK	CONFIGURATION	VOLTAGE (V)
A	CMOS	0.x
B	CMOS	1.x
C	CMOS	2.x
D	CMOS	3.x
E	CMOS	4.x
F	CMOS	5.x
H	CMOS	6.x

N-channel open drain (XC61FN series)

MARK	CONFIGURATION	VOLTAGE (V)
K	N-ch	0.x
L	N-ch	1.x
M	N-ch	2.x
N	N-ch	3.x
P	N-ch	4.x
R	N-ch	5.x
S	N-ch	6.x

② Represents decimal number of detect voltage

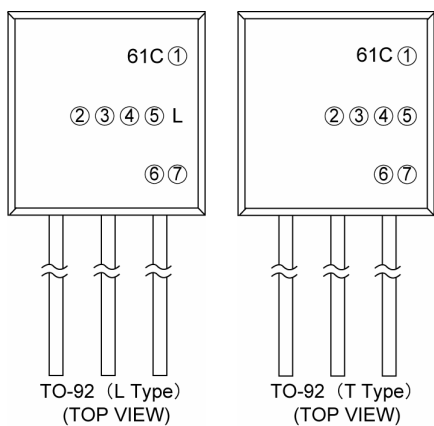
MARK	VOLTAGE (V)	MARK	VOLTAGE (V)
0	x.0	5	x.5
1	x.1	6	x.6
2	x.2	7	x.7
3	x.3	8	x.8
4	x.4	9	x.9

③ Represents delay time

VOLTAGE (V)	DELAY TIME
5	50 ~ 200ms
6	80 ~ 400ms
7	1 ~ 50ms

④ Represents assembly lot number (Based on internal standards)

● TO-92



① Represents output configuration

MARK	OUTPUT CONFIGURATION
C	CMOS
N	N-ch

②, ③ Represents detect voltage

MARK		VOLTAGE (V)
②	③	
3	3	3.3
5	0	5.0

④ Represents delay time

MARK	DELAY TIME
1	50ms ~ 200ms
4	80ms ~ 400ms
5	1ms ~ 50ms

⑤ Represents detect voltage accuracy

MARK	DETECT VOLTAGE ACCURACY
2	Within +2%

⑥ Represents a least significant digit of the production year (ex.)

MARK	PRODUCTION YEAR
3	2003
4	2004

⑦ Represents production lot number

0 to 9, A to Z repeated (G, I, J, O, Q, W expected)

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