TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSII)

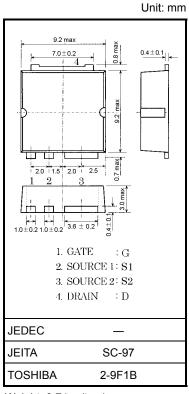
2SK3440

Switching Regulator, DC-DC Converter Applications Motor Drive Applications

- Low drain-source ON resistance: RDS (ON) = $6.5 \text{ m}\Omega$ (typ.)
- High forward transfer admittance: $|Y_{fs}| = 30 \text{ S (typ.)}$
- Low leakage current: IDSS = 100 μA (VDS = 60 V)
- Enhancement mode: $V_{th} = 2.0 \text{ to } 4.0 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	60	V	
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	60	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	I _D	50	Α	
	Pulse (Note 1)	I _{DP}	200		
Drain power dissipation (Tc = 25°C)		P _D	125	W	
Single pulse avalanche energy (Note 2)		E _{AS}	644	mJ	
Avalanche current		I _{AR}	50	А	
Repetitive avalanche energy (Note 3)		E _{AR}	12.5	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	



Weight: 0.74 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit	
Thermal resistance, channel to case	R _{th (ch-c)}	1.00	°C/W	

Notice:

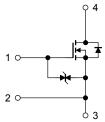
Please use the S1 pin for gate input signal return. Make sure that the main current flows into the S2 pin.

Note 1: Ensure that the channel temperature does not exceed 150°C.

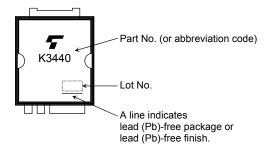
Note 2: V_{DD} = 50 V, T_{ch} = 25°C (initial), L = 350 μ H, R_G = 25 Ω , I_{AR} = 50 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic-sensitive device. Please handle with caution.



Marking



Electrical Characteristics (Note 4) (Ta = 25°C)

Ch	aracteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cui	rrent	I _{GSS}	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μΑ
Drain cut-off curr	ent	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		_	100	μА
Drain-source bre	akdown voltage	V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	60	_	_	V
Gate threshold v	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.0	_	4.0	V
Drain-source ON	resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 25 A	_	6.5	8	mΩ
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 25 A	15	30	_	S
Input capacitance		C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	_	3700	_	pF
Reverse transfer capacitance		C _{rss}			280	_	pF
Output capacitance		Coss		_	1320	_	pF
Switching time	Rise time	t _r	V _{DD} ~ 30 V	_	12	_	
	Turn-on time	t _{on}		_	30	_	
	Fall time	t _f		_	12	_	ns
	Turn-off time	t _{off}	V _{IN} : Duty ≦ 1%, t _W = 10 μs	_	50	_	
Total gate charge (gate-source plus gate-drain)		Qg	40.77		55		nC
Gate-source charge		Qgs	$V_{DD} \simeq 48 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		35		nC
Gate-drain ("miller") charge		Q _{gd}			20	_	nC

Note 4: Connect the S1 and S2 pins together, and ground them except during switchin time measurement.

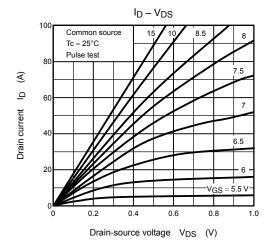
Source-Drain Ratings and Characteristics (Note 5) (Ta = 25°C)

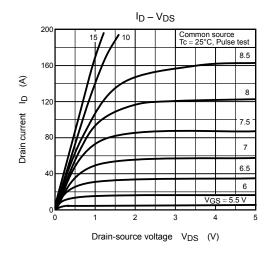
Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1, Note 5)	I _{DR} 1	_	_	_	50	Α
Pulse drain reverse current (Note 1, Note 5)	I _{DRP} 1	_	ı	_	200	Α
Continuous drain reverse current (Note 1, Note 5)	I _{DR} 2	_		_	1	Α
Pulse drain reverse current (Note 1, Note 5)	I _{DRP} 2	_		_	4	Α
Forward voltage (diode)	V _{DS2F}	$I_{DR} = 50 \text{ A}, V_{GS} = 0 \text{ V}$	_	_	-1.5	V
Reverse recovery time	t _{rr}	$I_{DR} = 50 \text{ A}, V_{GS} = 0 \text{ V},$	_	70	_	ns
Reverse recovery charge	Q _{rr}	$dI_{DR}/dt = 100 \text{ A/}\mu\text{s}$		123	_	nC

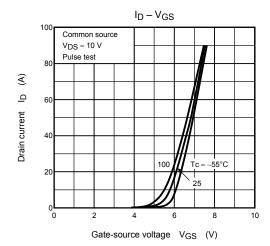
Note 5: I_{DR}1, I_{DRP}1: Current flowing between the drain and the S2 pin. Ensure that the S1 pin is left open. I_{DR}2, I_{DRP}2: Current flowing between the drain and the S1 pin. Ensure that the S2 pin is left open.

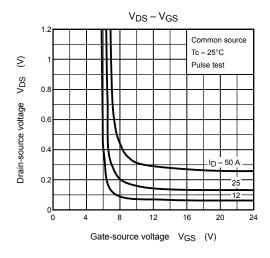
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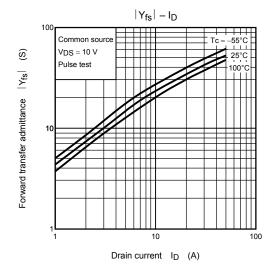
Unless otherwise specified, connect the S1 and S2 pins together, and ground them.

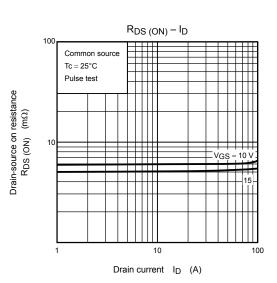




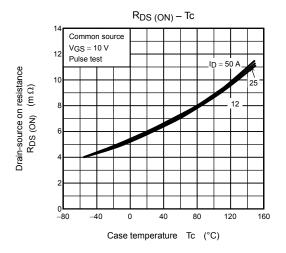


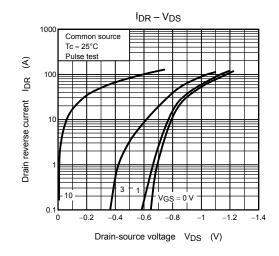


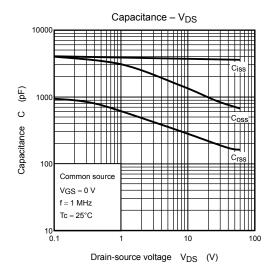


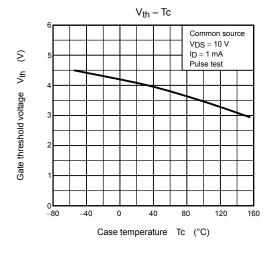


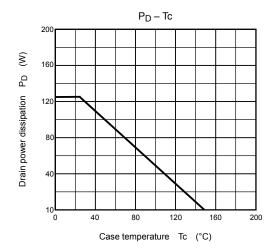
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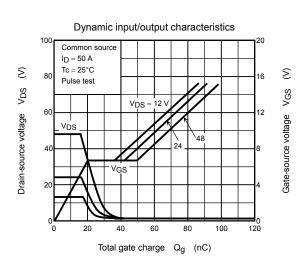




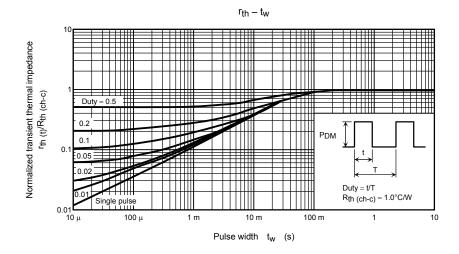


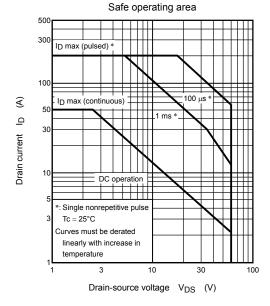


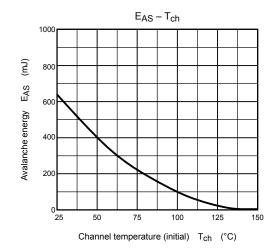


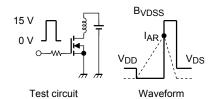


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$$R_G = 25~\Omega$$

$$V_{DD} = 50~V,~L = 350~\mu H$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{BVDSS}{BVDSS - VDD} \right)$$

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