XC612 Series

2-Channel Voltage Detectors

■GENERAL DESCRIPTION

The XC612 series consist of 2 voltage detectors, in 1 mini-molded, SOT-25 package.

The series provides accuracy and low power consumption through CMOS processing and laser trimming and consists of a highly accurate voltage reference source, 2 comparators, hysteresis and output driver circuits.

The input (V_{IN1}) for voltage detector 1 (V_{D1}) dually functions as the power supply pin for both detector 1 (V_{D1}) and detector 2 (V_{D2}).

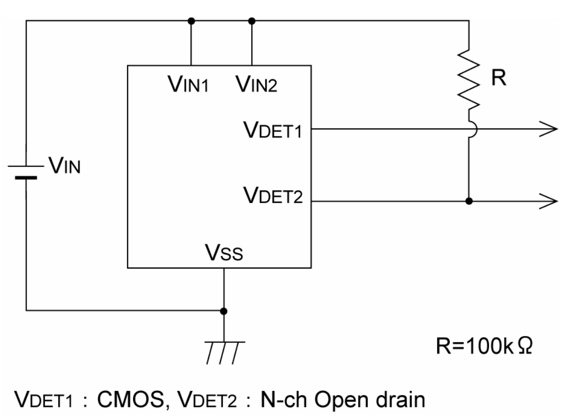
■APPLICATIONS

●Microprocessor reset circuitry
●Memory battery back-up circuits
●Power-on reset circuits
●Power failure detection
●System battery life and charge voltage monitors
●Delay circuitry

■FEATURES

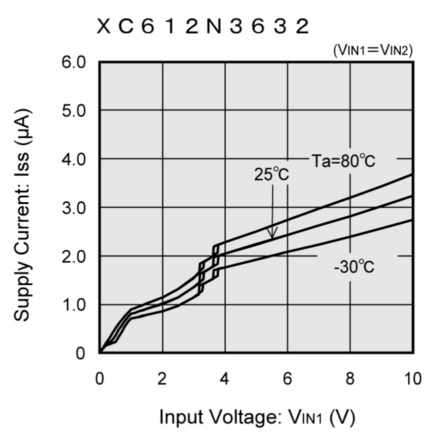
Highly Accurate : Setting voltage accuracy ±2%
Low Power Consumption : 2.0 μA(TYP.) (V_{IN1}=V_{IN2}=2.0V, Static state)
Detect Voltage : 1.5V ~ 5.0V programmable in 100mV steps. Detector's voltages can be set-up independently
Conditionaly;
XC612N : V_{DET1}>V_{DET2}
XC612D, XC612E : V_{DET1}≧V_{DET2}, V_{DET1}<V_{DET2}
Operating Voltage Range : 1.5V ~ 10.0V
Temperature Characteristics : ±100ppm/℃ (TYP.)
Output Configuration : N-channel open drain
CMOS Low Power Consumption
2 Voltage Detectors Built-in
Small Package : SOT-25 (150mW) mini-mold
*** CMOS Output is under development**

■TYPICAL APPLICATION CRICUIT

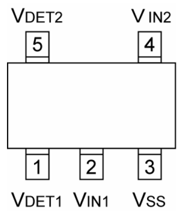


■TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Input Voltae



■PIN CONFIGURATION



SOT-25
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTION
1	V_{DET1}	Voltage Detector 1 Output
2	V_{IN1}	Detector 1 Input, Power Supply
3	V_{SS}	Ground
4	V_{IN2}	Voltage Detector 2 Input
5	V_{DET2}	Voltage Detector 2 Output

■PRODUCT CLASSIFICATION

●Selection Guide

TYPE	V_{DET1}	V_{DET2}
XC612N	N-ch Open Drain	N-ch Open Drain
XC612D	N-ch Open Drain	CMOS
XC612E	CMOS	N-ch Open Drain

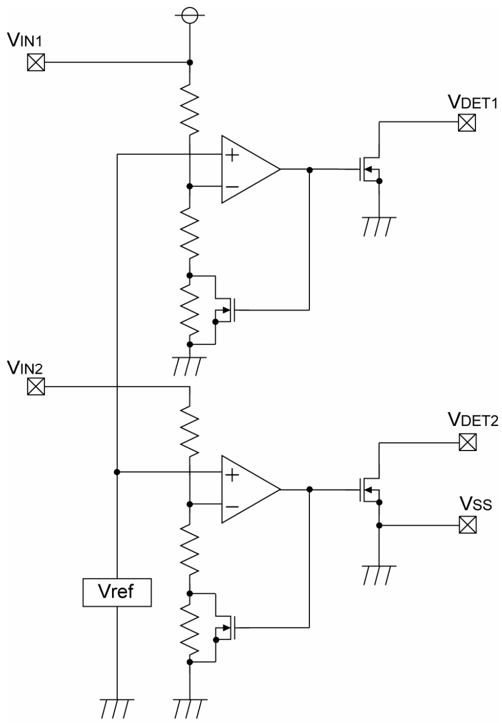
●Ordering Information

XC612①②③④⑤⑥⑦

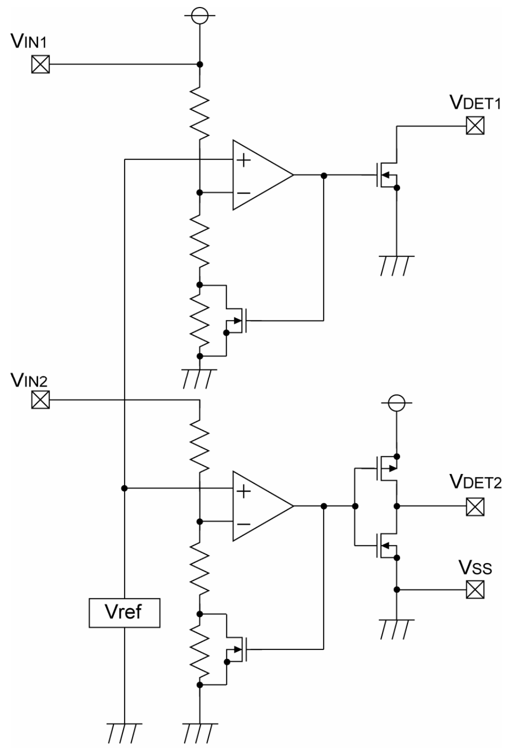
DESIGNATOR	DESCRIPTION	SYMBOL	DESCRIPTION
①	Output Configuration	N	: V_{DET1}/V_{DET2}: N-ch open drain
		D	: V_{DET1}: N-ch open drain, V_{DET2}: CMOS
		E	: V_{DET1}: CMOS, V_{DET2}: N-ch open drain
②③	Detect Voltage 1 (V_{DET1})	15～50	: V_{DET1}: 2.5V→②25
④⑤	Detect Voltage 2 (V_{DET2})	15～50	: V_{DET2}: 3.3V→③33
⑥	Package	M	: SOT-25 (SOT-23-5)
⑦	Device Orientation	R	: Embossed tape, standard feed
		L	: Embossed tape, reverse feed

■BLOCK DIAGRAMS

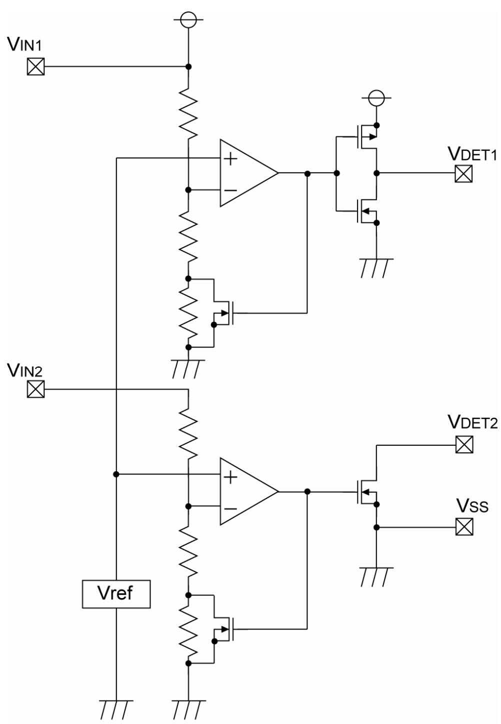
XC612N Series



XC612D Series



XC612E Series



■ABSOLUTE MAXIMUM RATINGS

Ta = 25℃

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage	VD 1	VIN1	12.0	V
	VD 2	VIN2	12.0	V
Output Voltage	VD 1 (N-ch open drain)	VVDET1	VSS – 0.3 ~ 12.0	V
	VD 1 (CMOS)		VSS – 0.3 ~ VIN1 + 0.3	V
	VD 2 (N-ch open drain)	VVDET2	VSS – 0.3 ~ 12.0	V
	VD 2 (CMOS)		VSS – 0.3 ~ VIN1 + 0.3	V
Output Current	VD 1	IVDET1	50	mA
	VD 2	IVDET2	50	mA
Power Dissipation		Pd	150	mW
Operating Temperature Range		Topr	- 30 ~ + 80	℃
Storage Temperature Range		Tstg	- 40 ~ + 125	℃

■ELECTRICAL CHARACTERISTICS

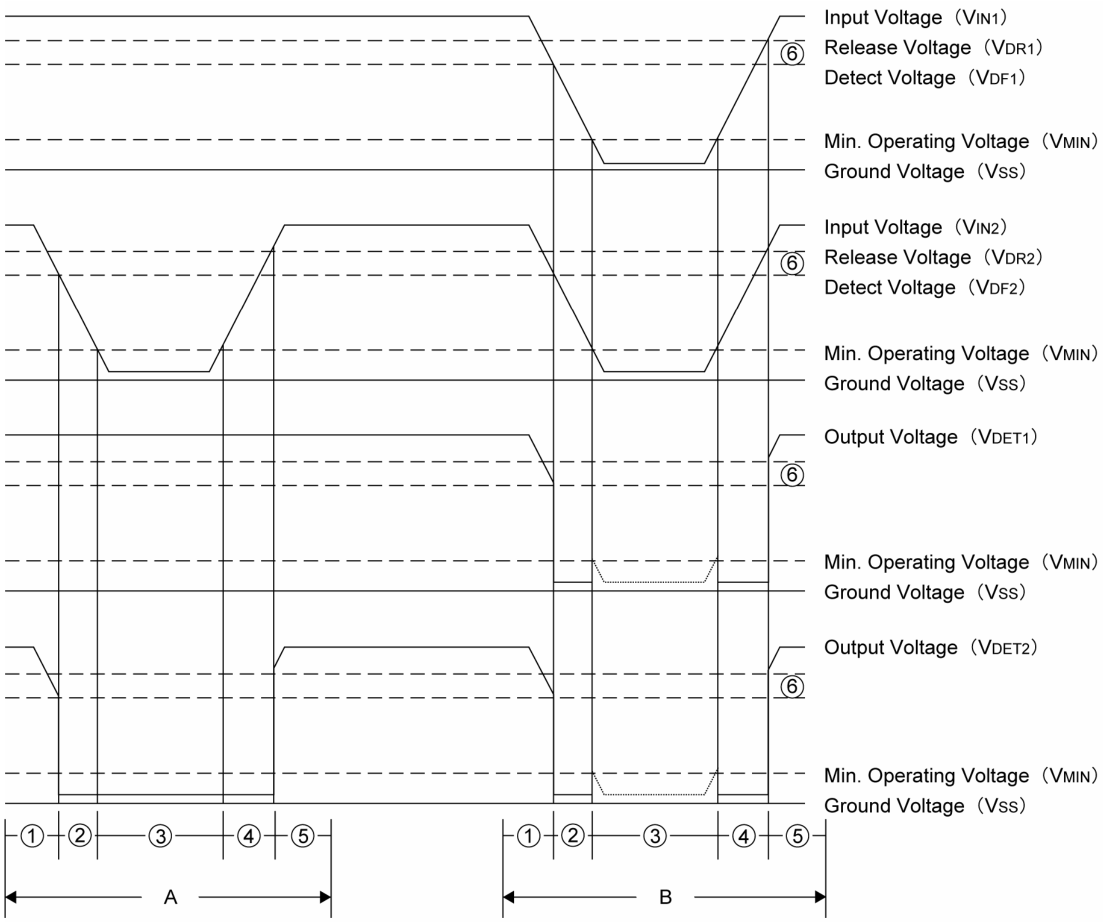
Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUITS
Detect Voltage (V_{DET1}) (*1)	V_{DF1}	Voltage when V_{DET1} changes from H to L following a reduction of V_{IN1}	V_{DF1} x 0.98	V_{DF1}	V_{DF1} x 1.02	V	1
Detect Voltage (V_{DET2}) (*1)	V_{DF2}	Voltage when V_{DET2} changes from H to L following a reduction of V_{IN2}	V_{DF2} x 0.98	V_{DF2}	V_{DF2} x 1.02	V	1
Hysteresis Range 1	V_{HYS1}	Voltage (V_{DR1}) - V_{DF1} when V_{DET1} changes from L to H following an increase of V_{IN1}	$V_{DF1(T)}$ x 0.02	$V_{DF1(T)}$ x 0.05	$V_{DF1(T)}$ x 0.08	V	1
Hysteresis Range 2	V_{HYS2}	Voltage (V_{DR2}) - V_{DF2} when V_{DET2} changes from L to H following an increase of V_{IN2}	$V_{DF2(T)}$ x 0.02	$V_{DF2(T)}$ x 0.05	$V_{DF2(T)}$ x 0.08	V	1
Supply Current (V_{IN1} Input Current)	I_{SS}	V_{IN1} = 1.5V	-	1.35	3.90	μA	2
		V_{IN1} = 2.0V	-	1.50	4.50		
		V_{IN1} = 3.0V	-	1.95	5.10		
		V_{IN1} = 4.0V	-	2.40	5.70		
		V_{IN1} = 5.0V	-	3.00	6.30		
V_{IN2} Input Current	I_{IN2}	V_{IN2} = 1.5V	-	0.45	1.30	μA	2
		V_{IN2} = 2.0V	-	0.50	1.50		
		V_{IN2} = 3.0V	-	0.65	1.70		
		V_{IN2} = 4.0V	-	0.80	1.90		
		V_{IN2} = 5.0V	-	1.00	2.10		
Operating Voltage	V_{IN1}	$V_{DF(T)}$ = 1.5V to 6.0V	1.0	-	10	V	—
Output Current (*3)	I_{VDET}	N-ch, V_{DS}=0.5V, V_{IN1} = 1.0V	0.3	2.2	-	mA	3
		V_{IN1} = 2.0V	3.0	7.7	-		
		V_{IN1} = 3.0V	5.0	10.1	-		
		V_{IN1} = 4.0V	6.0	11.5	-		
		V_{IN1} = 5.0V	7.0	13.0	-		
		P-ch (CMOS) V_{DS}=-2.1V, V_{IN1} = 8.0V	-	-10.0	-2.0		
Temperature Characteristics (*3)	$\frac{\Delta V_{DF}}{\Delta Topr \cdot V_{DF}}$	-30℃ ≦ Topr ≦ 80℃	-	±100	—	ppm/℃	—
Delay Time (*3) (Release Voltage→Output inversion)	tDLY	(V_{DR}→V_{OUT} inversion)	-	-	0.2	ms	5

NOTE:
*1 : V_{DF1}(T), V_{DF2}(T) : User specified detect voltage.
*2 : Release voltage (V_{DR}) = V_{DF} +V_{HYS}
*3 : Those parameters marked with an asterisk apply to both V_{DET1} and V_{DET2}.
*4 : Input Voltage : please ensure that V_{IN1} > V_{IN2}
(Input voltage of XC612D and XC612E series : please ensure that V_{IN1} ≧ V_{IN2}, V_{IN1} < V_{IN2}.)
*5 : V_{IN1} pin serve both I_{SS} and power supply pin so that V_{IN2} operates V_{IN1} as a power supply source. For normal operation of V_{IN2}, operating voltage higher than the minimum is needed to be applied to power supply pin V_{IN1}.
*6 : For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of V_{IN}.

■OPERATONAL EXPLANATION

●Timing Chart (Pull up voltage =Input voltage V_{IN1})



●Operational Notes (N-ch Open drain)

Timing Chart A (V_{IN1}=voltages above release voltage, V_{IN2}=sweep voltage)

Because a voltage higher than the minimum operating voltage is applied to the voltage input pin (V_{IN}), ground voltage will be output at the output pin (V_{DET}) during stage 3. (Stages 1, 2, 4, 5 are the same as in B below).

Timing Chart B (V_{IN1}=V_{IN2})

① When a voltage greater than the release voltage (V_{DR}) is applied to the voltage input pin (V_{IN1}, V_{IN2}), input voltage (V_{IN1}, V_{IN2}) will gradually fall.
When a voltage greater than the detect voltage (V_{DF}) is applied to the voltage input pin (V_{IN1}, V_{IN2}), a state of high impedance will exist at the output pin (V_{DET1}, V_{DET2}), so should the pin be pulled up, voltage will be equal to pull up voltage.

② When input voltage (V_{IN1}, V_{IN2}) falls below detect voltage (V_{DF}), output voltage (V_{DET1}, V_{DET2}) will be equal to ground level (V_{SS}).

③ Should input voltage (V_{IN1}, V_{IN2}) fall below the minimum operational voltage (V_{MIN}), output will become unstable. Should V_{IN2} fall below V_{MIN}, voltage at the output pin (V_{DET2}) will be equal to ground level (V_{SS}) if the power supply (V_{IN1}) is within the operating voltage range.
*In general the output pin is pulled up so output will be equal to pull up voltage.

④ Should input voltage (V_{IN1}, V_{IN2}) rise above ground voltage (V_{SS}), output voltage (V_{DET1}, V_{DET2}) will equal ground level until the release voltage level (V_{DR}) is reached.

⑤ When input voltage (V_{IN1}, V_{IN2}) rises above release voltage, the output pin's (V_{DET1}, V_{DET2}) voltage will be equal to the voltage dependent on pull up.

Note : The difference between release voltage (V_{DR}) and detect voltage (V_{DF}) is the Hysteresis Range ⑥.

■NOTES ON USE

1. Please use this IC within the specified maximum absolute ratings.
2. Please ensure that input voltage V_{IN2} is less than V_{IN1} + 0.3V. (refer to N.B. 1 below)
3. With a resistor connected between the V_{IN1} pin and the input, oscillation is liable to occur as a result of through current at the time of release. (refer to N.B. 2 below)
4. With a resistor connected between the V_{IN1} pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{IN1} pin.
5. In order to stabilize the IC's operations, please ensure that the V_{IN1} pin's input frequency's rise and fall times are more than 5 msec/V.
6. Should the power supply voltage V_{IN1} exceed 6V, voltage detector 2's detect voltage (V_{DF2}) and the release voltage (V_{DR2}) will shift somewhat.
7. For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of V_{IN}.

●N.B.

1. Voltage detector 2's input voltage (V_{IN2})
   An input protect diode is connected from input detector 2's input (V_{IN2}) to input detector 1's input. Therefore, should the voltage applied to V_{IN2} exceed V_{IN1}, current will flow through V_{IN1} via the diode. (refer to diagram1)
2. Oscillation as a result of through current
   Since the XC612 series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor (R_{IN}) during release voltage operations. (refer to diagram 2)
   Since hysteresis exists during detect operations, oscillation is unlikely to occur.

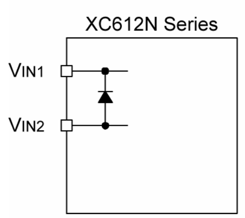


Diagram 1. Voltage detector 2's input voltage V_{IN2}

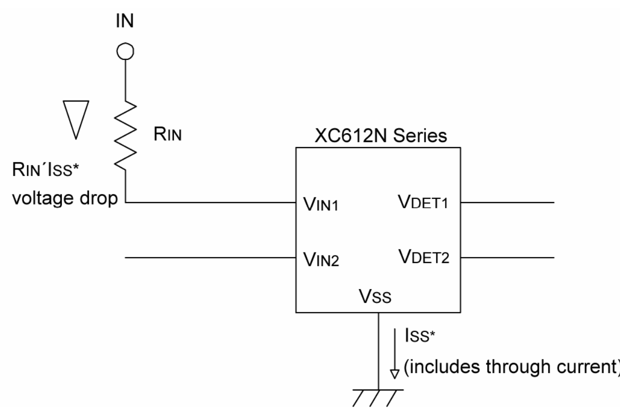
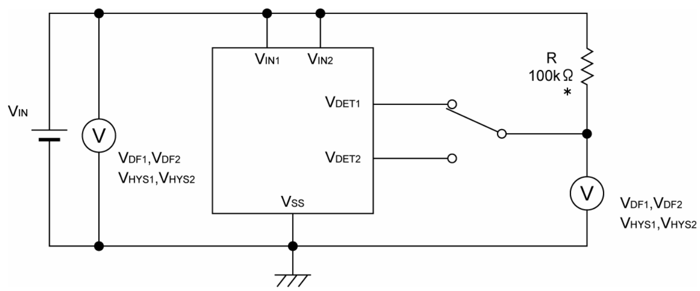


Diagram 2. Through current oscillation

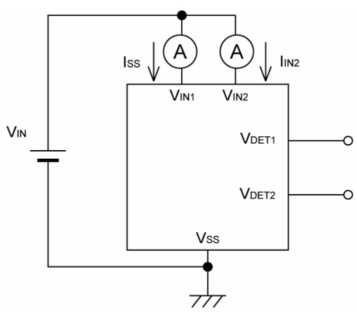
■TEST CIRCUITS

Circuit 1



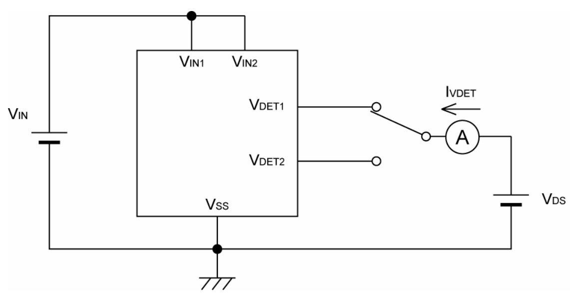
* A resistor is not needed for CMOS output type.

Circuit 2

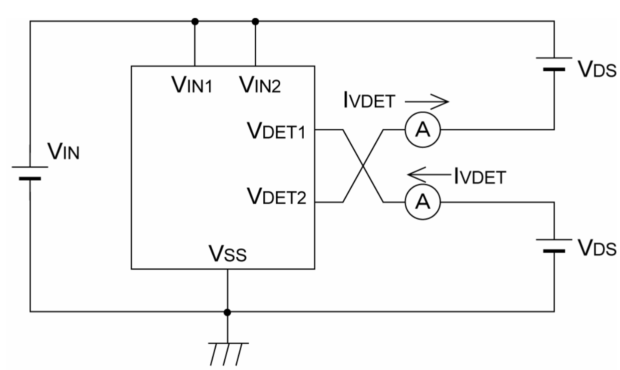


Circuit 3

XC612N Series



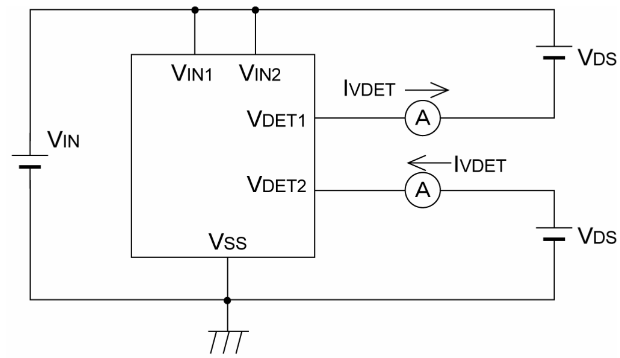
XC612D Series



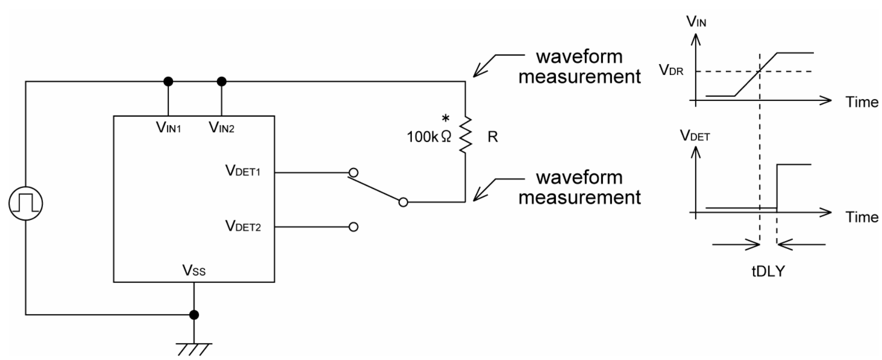
■TEST CIRCUITS (Continued)

Circuit 3 (Continued)

XC612E Series

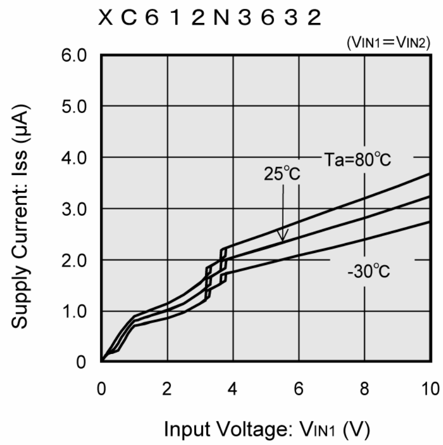


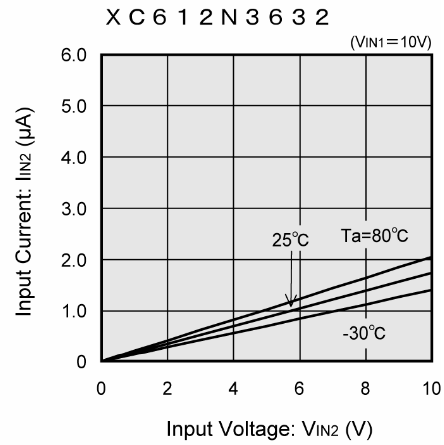
Circuit 4



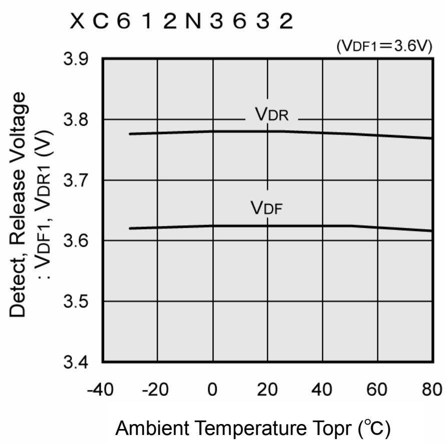
■TYPICAL PERFORMANCE CHARACTERISTICS

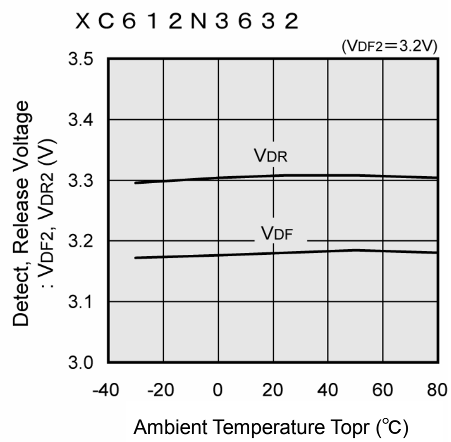
(1) Supply Current vs. Input Voltage





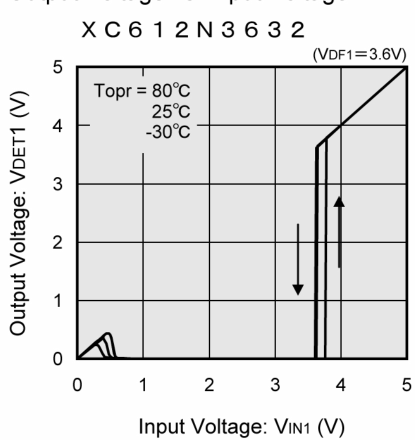
(2) Detect & Release Voltage vs. Ambient Temperature

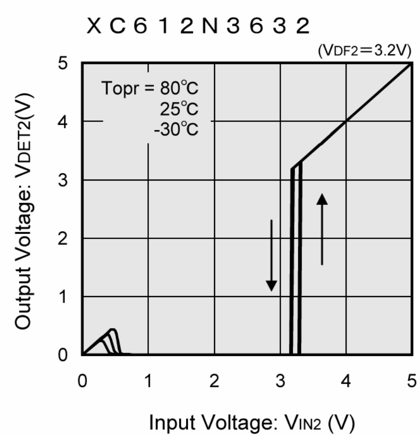




Note: Unless otherwise stated, pull up resistance = 100kΩ with N-ch open drain output type.

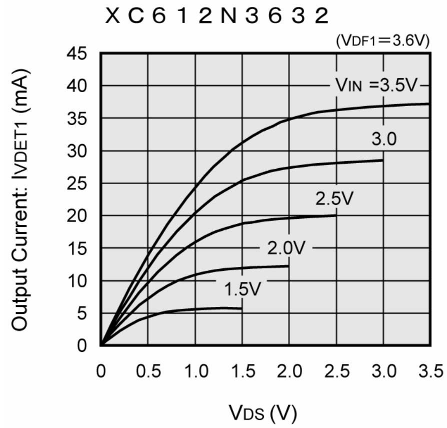
(3) Output Voltage vs. Input Voltage

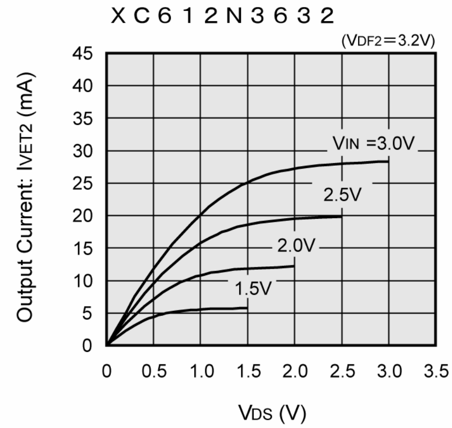


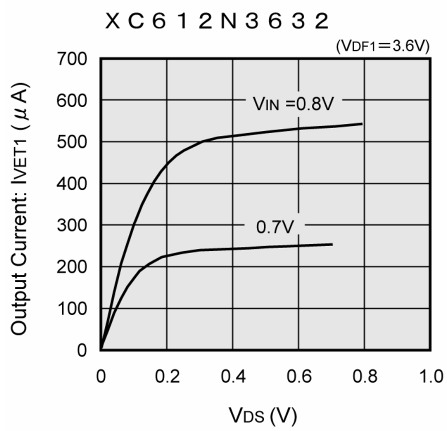


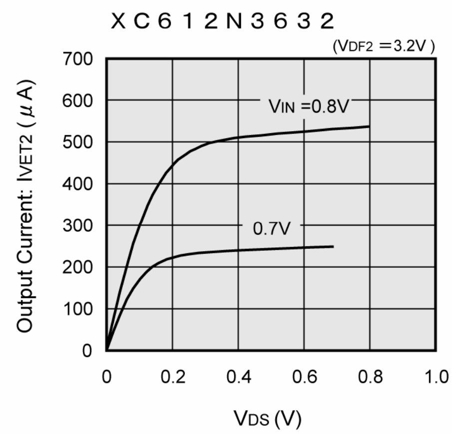
■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(4) N-ch Driver Output Current vs. VDS

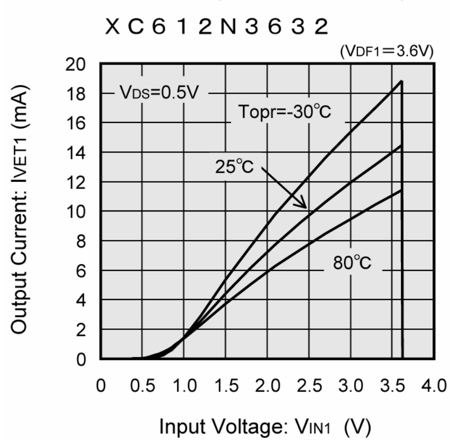


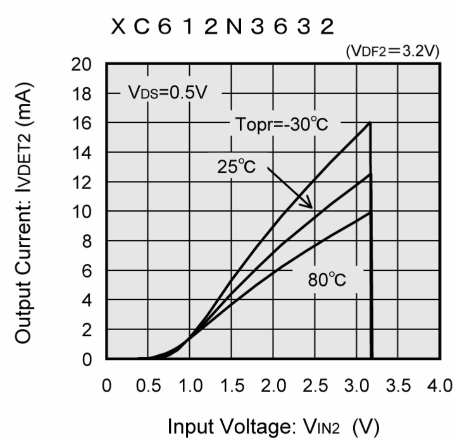






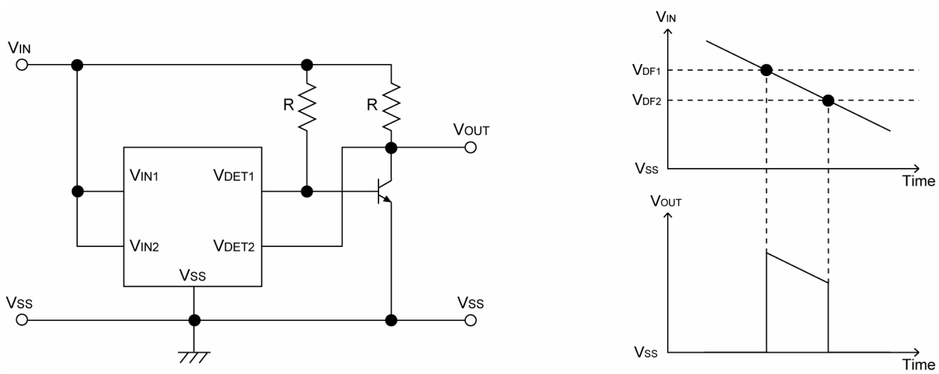
(5) N-ch Driver Output Current vs. Input Voltage



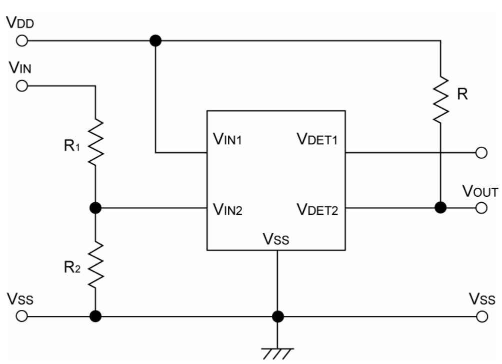


■APPLICATION CIRCUITS EXAMPLE *Example covers N-channel open drain product's circuits

●Window comparator circuit



●Detect voltages above respective established voltages circuit



On resistors R1 and R2 equation (1) and (2)

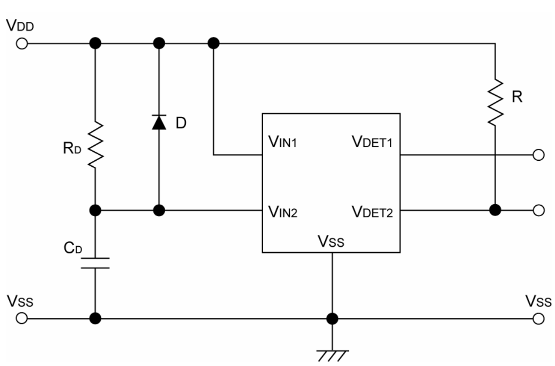
Detect voltage $= \{ (R1 + R2) \div R2\} \times V_{DF2}$ (1)

N.B. V_{DF2} = detect voltage VD2

Hysteresis $(V_{HYS2}) = \{ (R1 + R2) \div R2 \} \times V_{HYS2}$ (2)

Note: Please ensure that input voltage 2 (V_{IN2}) is less than V_{IN1} + 0.3V

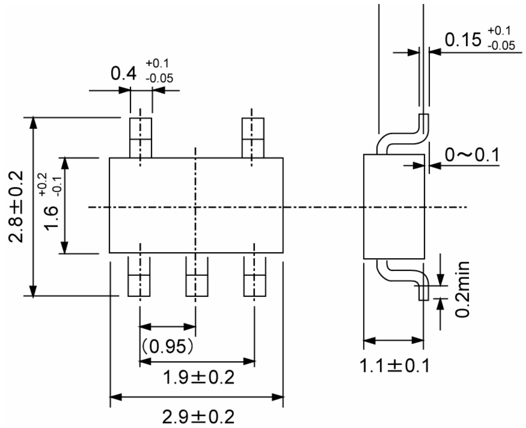
●Detect voltage circuit with delay built-in



Note: Delay operates at both times of release and detect operations.

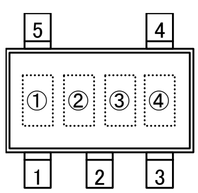
■PACKAGING INFORMATION

●SOT-25



■MARKING RULE

●SOT-25



SOT-25
(TOP VIEW)

①Represents output configuration

MARK	CONFIGURATION		PRODUCT SERIES
	VDET1	VDET2	
N	N-ch Open Drain	N-ch Open Drain	XC612NxxxxMx
D	N-ch Open Drain	CMOS	XC612DxxxxMx
E	CMOS	N-ch Open Drain	XC612ExxxxMx

②, ③Represents sequence number

④Represents production lot number
0 to 9, A to Z repeated. (G, I, J, O, Q, W excepted.)

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