TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

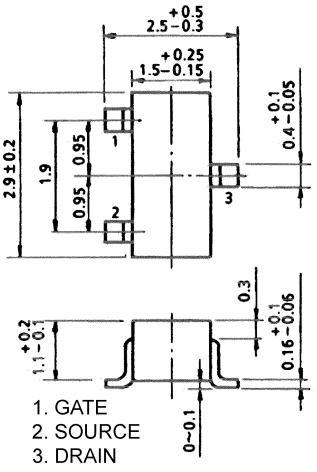
2SJ305

High Speed Switching Applications

Analog Applications

- High input impedance
- Low gate threshold voltage.: V_{th} = −0.5~−1.5 V
- Excellent switching times.: t_{on} = 0.06 μs (typ.)
  t_{off} = 0.15 μs (typ.)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 2.4 Ω (typ.)
- Small package.
- Complementary to 2SK2009

Unit: mm



S-MINI

JEDEC	TO-236MOD
JEITA	SC-59
TOSHIBA	2-3F1F

Weight: 0.012 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

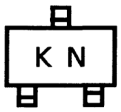
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DS}	−30	V
Gate-source voltage	V_{GSS}	±20	V
DC drain current	I_D	−200	mA
Drain power dissipation	P_D	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

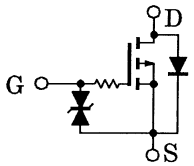
Note: This transistor is electrostatic sensitive device.

Please handle with caution.

Marking



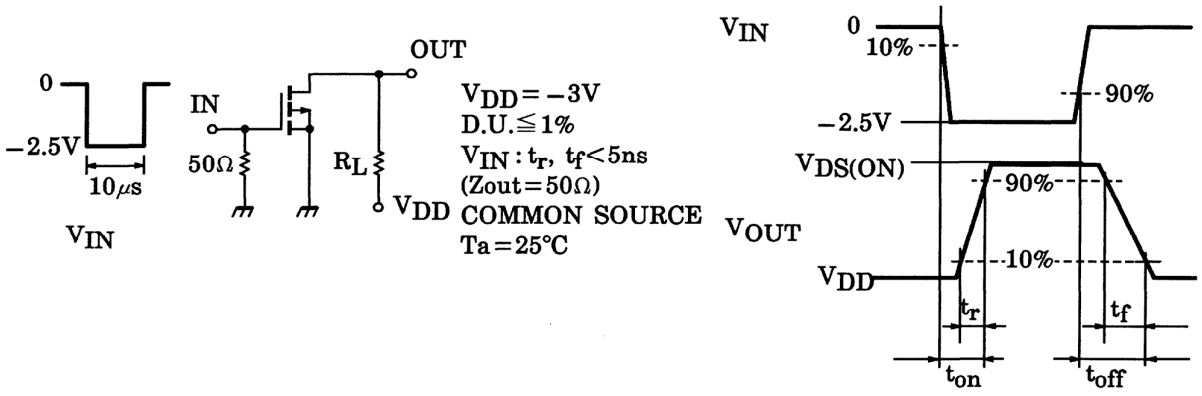
Equivalent Circuit



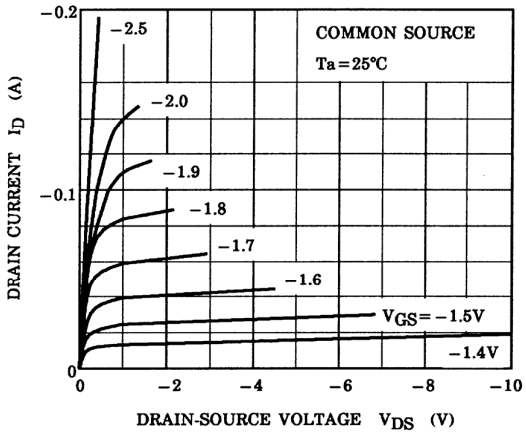
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0	—	—	±0.1	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −1 mA, V_{GS} = 0	−30	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0	—	—	−10	μA
Gate threshould voltage		V_{th}	V_{DS} = −3 V, I_D = −0.1 mA	−0.5	—	−1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3 V, I_D = −50 mA	100	—	—	mS
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = −50 mA, V_{GS} = −2.5 V	—	2.4	4	Ω
Input capacitance		C_{iss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	92	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	36	—	pF
Output capacitance		C_{oss}	V_{DS} = −3 V, V_{GS} = 0, f = 1 MHz	—	80	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −3 V, I_D = −10 mA V_{GS} = 0~−2.5 V	—	0.06	—	μs
	Turn-off time	t_{off}	V_{DD} = −3 V, I_D = −10 mA V_{GS} = 0~−2.5 V	—	0.15	—	

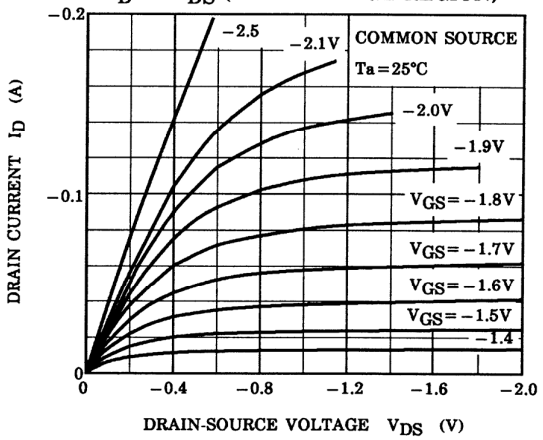
Switching Time Test Circuit



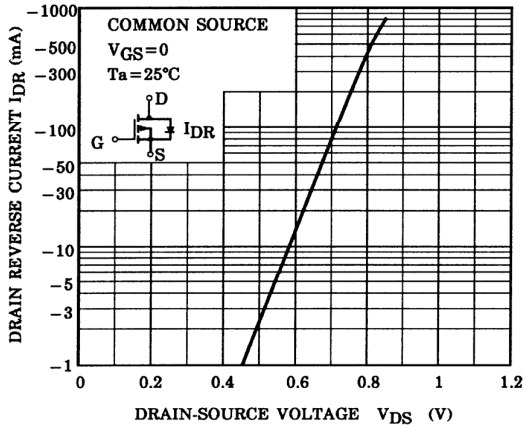
$I_D - V_{DS}$



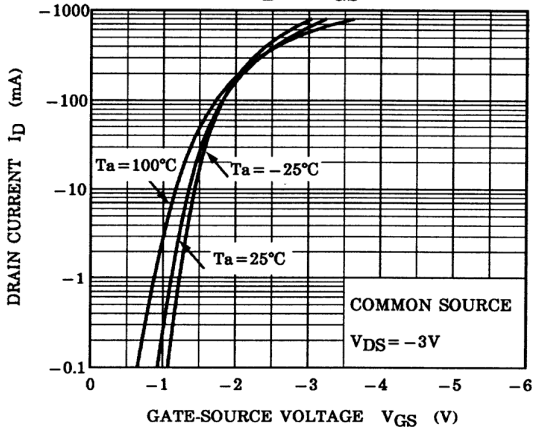
$I_D - V_{DS}$ (LOW VOLTAGE REGION)



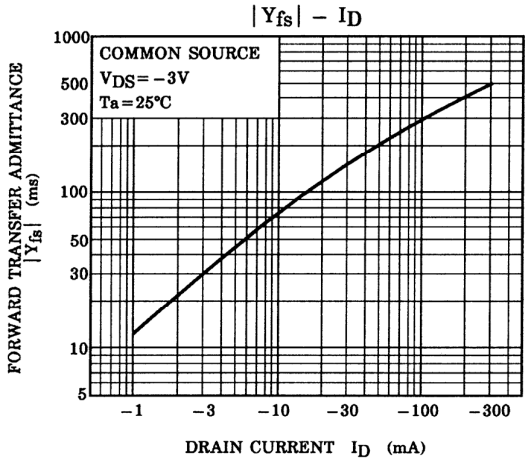
$I_{DR} - V_{DS}$



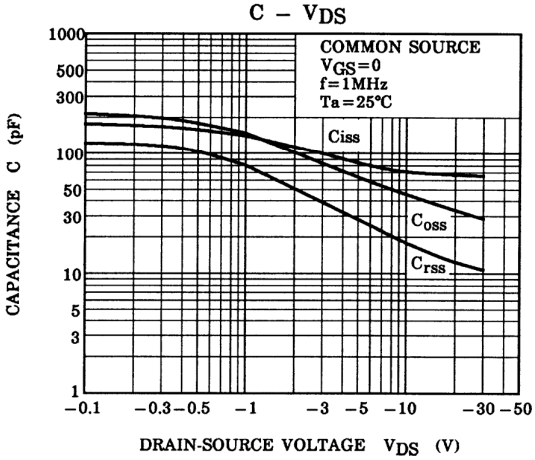
$I_D - V_{GS}$



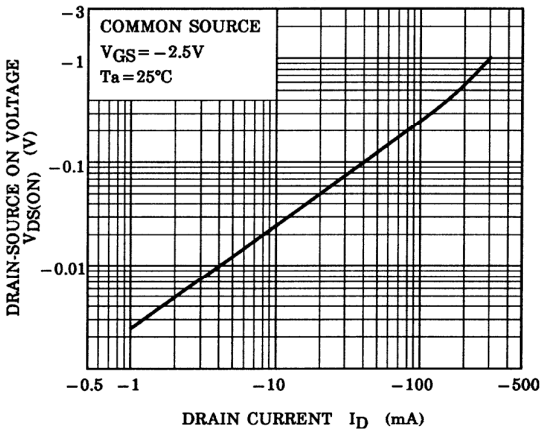
$|Y_{fs}| - I_D$



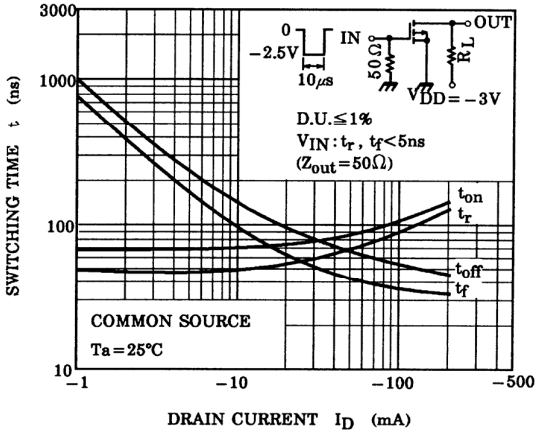
C − VDS



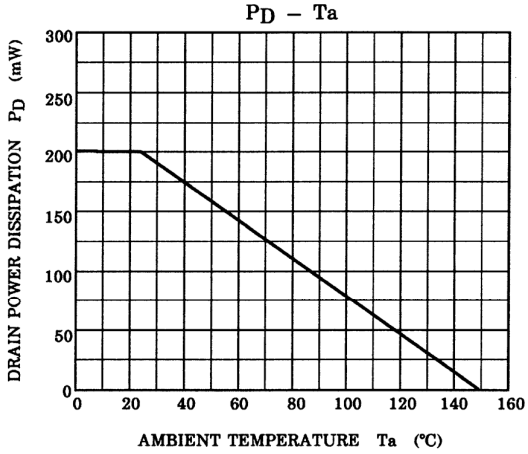
$V_{DS\,(ON)}$ – I_D



t – I_D



P_D – Ta



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20070701-EN GENERAL

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