100 MHz, 80-Channel Serial To Parallel Converter With Push-Pull Outputs

Ordering Information

Device	Package Options	
	100 Lead Quad Plastic Gullwing	Die
HV574	HV574PG	HV574X

Features

- ❏ Processed with HVCMOS® technology
- ❏ 5V CMOS logic
- ❏ Output voltages up to 80V
- ❏ Low power level shifting
- ❏ 100MHz equivalent data rate using four dynamic shift registers
- ❏ Static latched data outputs
- ❏ Forward and reverse shifting options (DIR pin)
- ❏ Diode to V_{PP} allows efficient power recovery
- ❏ Outputs may be hot switched
- ❏ Hi-Rel processing available

General Description

The HV574 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for printer applications. It can also be used in any application requiring multiple output high-voltage current sourcing and sinking capability such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays.

The device has 4 parallel 20-bit dynamic shift registers, permitting data rates 4X the speed of one (they are clocked together).

There are 80 static latches and control logic to perform the polarity select and blanking of the outputs. $HV_{OUT}1$ is connected to the first stage of the first shift register through the polarity and blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to GND, and CW shifting when connected to V_{DD}. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}80$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), BL (blanking), or the POL (polarity) inputs. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latches is stored when $\overline{LE}$ is low.

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]	-0.5V to +7.5V
Output voltage, V_{PP}[1]	-0.5V to +90V
Logic input levels[1]	-0.3V to V_{DD} +0.3V
Ground current[2]	1.5A
Continuous total power dissipation[3]	1200mW
Operating temperature range	-40 to 85°C
Storage temperature range	-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C

Notes:
1. All voltages are referenced to GND.
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 20mW/°C.

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Electrical Characteristics (over recommended commercial operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			30	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 25MHz
I_{PP}	Quiescent V_{PP} supply current			100	µA	Outputs high
				100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			100	µA	All $V_{IN} = V_{DD}$
V_{OH}	High-level output	HV_{OUT}	V_{PP} - 9V		V	I_O= -30mA, V_{PP} = 80V
		Data out	V_{DD} - 0.5		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		3.75	V	I_O = 15mA, V_{DD} = 5V
		Data out		0.5	V	I_O= 100µA
I_{IH}	High-level logic input current			1.0	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1.0	µA	V_{IL} = 0V

AC Characteristics (T_A = 85°C max. Logic signal inputs and Data inputs have t_r, $t_f \leq$ 5ns [10% and 90% points])

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency	0.001	25	MHz	V_{DD} = 4.5V, T_J = 25°C
		0.001	20		V_{DD} = 4.5V, T_J = 125°C
t_{WL},t_{WH}	Clock width high or low	20		ns	
t_{SU}	Data set-up time before clock rises	0		ns	
t_H	Data hold time after clock rises	15		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low		38	ns	C_L = 15pF, V_{DD} = 5.0V
t_{DLH}	Delay time clock to data low to high		38	ns	C_L = 15pF, V_{DD} = 5.0V
t_{DLE}*	Delay time clock to $\overline{LE}$ low to high	25		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	25		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	0		ns	
tr, tf	Output rise/fall time		1.0	µs	C_L = 600pF, HV_{OUT} from 0 to 60V

* t_{DLE} is not required but is recommended to produce stable HV outputs and thus minimize power dissipation and current spikes (allows internal SR output to stabilize).

Recommended Operating Conditions

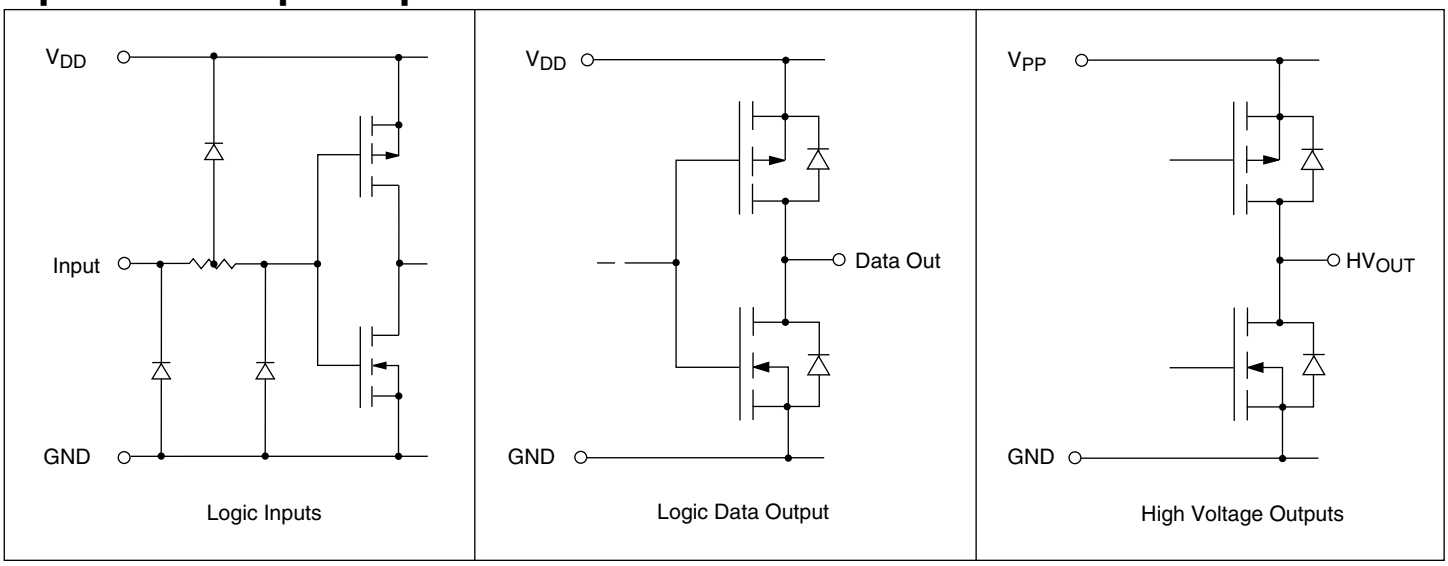
Symbol	Parameter	Min	Max	Units
V_{DD}	Logic supply voltage	4.5	5.5	V
V_{PP}	Output voltage	12	80	V
V_{IH}	High-level input voltage	V_{DD} -0.5V		V
V_{IL}	Low-level input voltage	0	0.5	V
f_{CLK}	Clock frequency per register	0.001	25	MHz
T_A	Operating free-air temperature	-40	+85	°C

Notes: Power-up sequence should be the following:

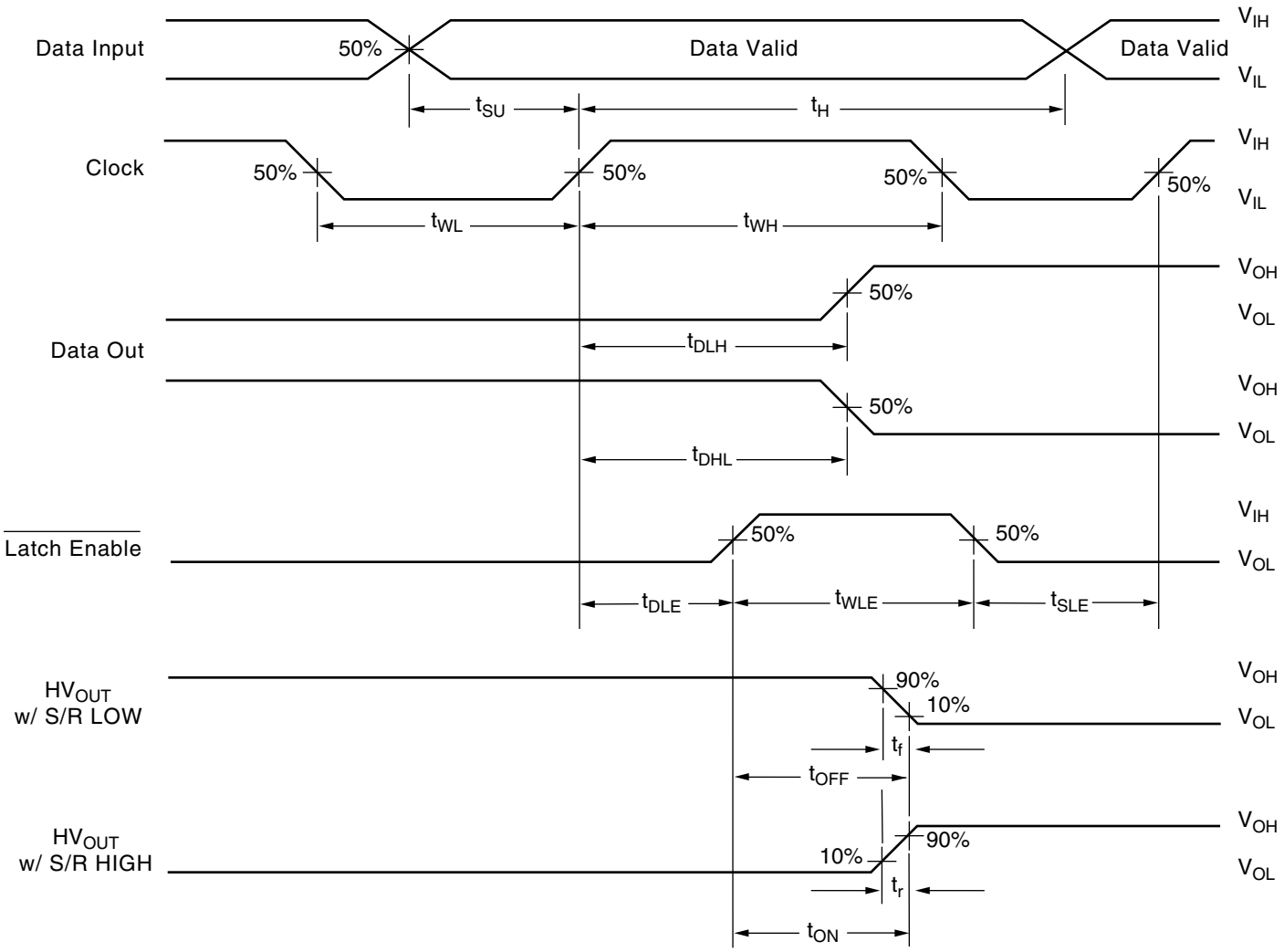
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.
5. The V_{PP} should not drop below V_{DD} or float during operation.

Power-down sequence should be the reverse of the above.
The V_{PP} should not drop below V_{DD} during operation.

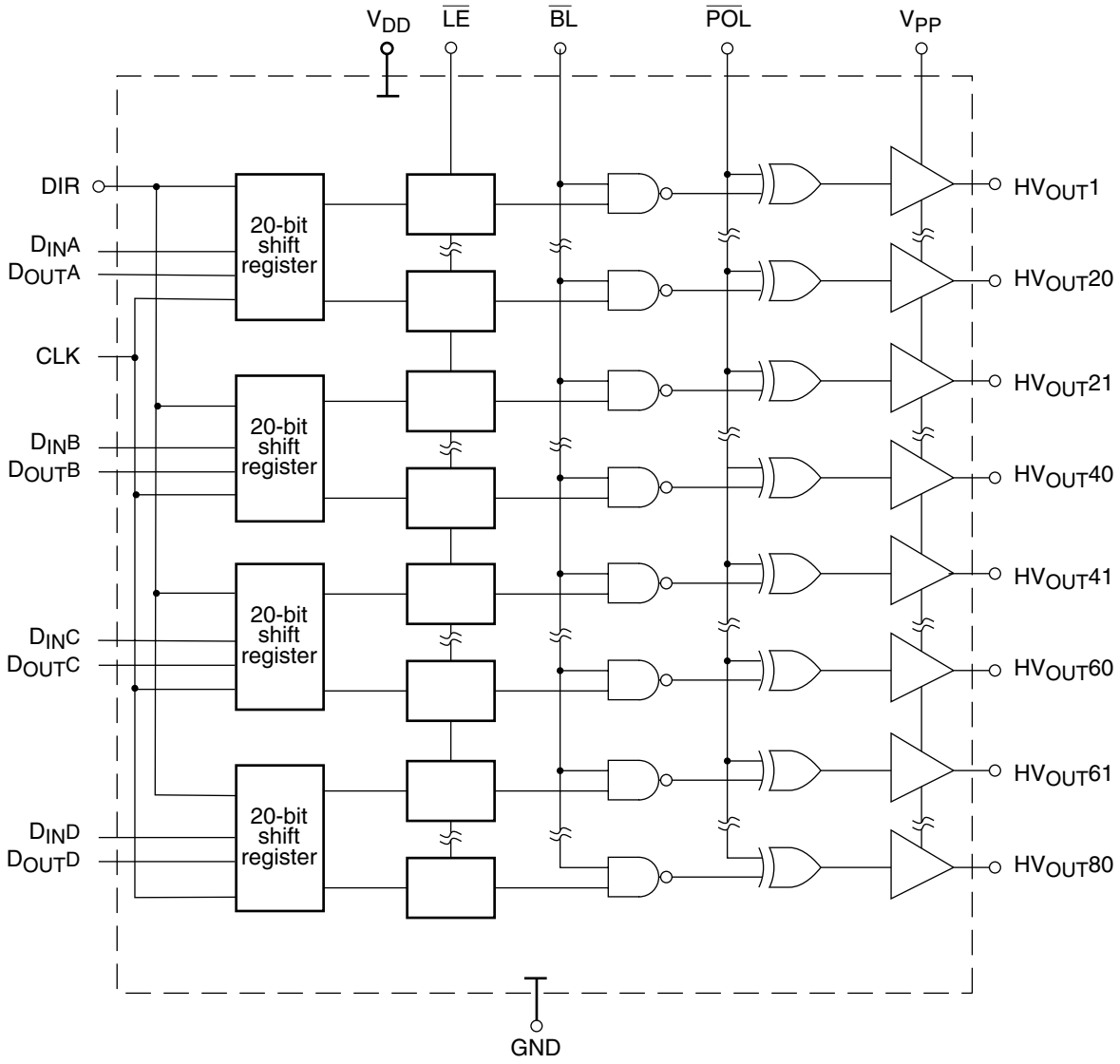
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs						Outputs		
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P High	X	X	X	L	L	X		H	
All O/P Low	X	X	X	L	H	X		L	
O/P Normal	X	X	X	H	H	X		No inversion	
O/P Inverted	X	X	X	H	L	X		Inversion	
Data Falls Through (Latches Transparent)	L	↑	H	H	H	X	L	L	
	H	↑	H	H	H	X	H	H	
	L	↑	H	H	L	X	L	H	
	H	↑	H	H	L	X	H	L	
Data Stored/ Latches Loaded	X	X	L	H	H	X	*	Stored Data	
	X	X	L	H	L	X	*	Inversion of Stored Data	
I/O Relation	$D_{IN}X$	↑	H	H	H	H	$Q_n \rightarrow Q_{n+1}$	New H or L	$D_{OUT}X$
	$D_{IN}X$	↑	L	H	H	H	$Q_n \rightarrow Q_{n+1}$	Previous H or L	$D_{OUT}X$
	$D_{OUT}X$	↑	L	H	H	L	$Q_n \rightarrow Q_{n-1}$	Previous H or L	$D_{IN}X$
	$D_{OUT}X$	↑	H	H	H	L	$Q_n \rightarrow Q_{n-1}$	New H or L	$D_{IN}X$

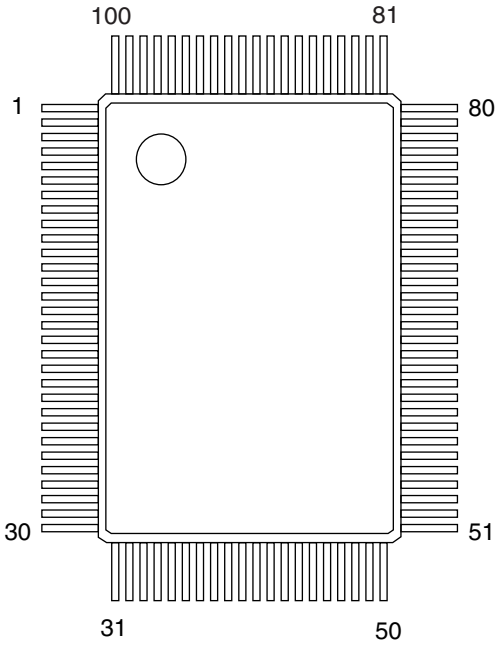
Notes: * = dependent on previous stage's state. See Pin configuration for D_{IN} and D_{OUT} pin designation for CW and CCW shift.

Pin Configuration

100-Pin PG Package

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	$HV_{OUT}30$	26	$HV_{OUT}5$	51	$HV_{OUT}80$	76	$HV_{OUT}55$
2	$HV_{OUT}29$	27	$HV_{OUT}4$	52	$HV_{OUT}79$	77	$HV_{OUT}54$
3	$HV_{OUT}28$	28	$HV_{OUT}3$	53	$HV_{OUT}78$	78	$HV_{OUT}53$
4	$HV_{OUT}27$	29	$HV_{OUT}2$	54	$HV_{OUT}77$	79	HVout52
5	$HV_{OUT}26$	30	$HV_{OUT}1$	55	$HV_{OUT}76$	80	$HV_{OUT}51$
6	$HV_{OUT}25$	31	N/C	56	$HV_{OUT}75$	81	$HV_{OUT}50$
7	$HV_{OUT}24$	32	V_{PP}	57	$HV_{OUT}74$	82	$HV_{OUT}49$
8	$HV_{OUT}23$	33	HVGND	58	$HV_{OUT}73$	83	$HV_{OUT}48$
9	$HV_{OUT}22$	34	$D_{IN}A$	59	$HV_{OUT}72$	84	$HV_{OUT}47$
10	$HV_{OUT}21$	35	$D_{IN}B$	60	$HV_{OUT}71$	85	$HV_{OUT}46$
11	$HV_{OUT}20$	36	$D_{IN}C$	61	$HV_{OUT}70$	86	$HV_{OUT}45$
12	$HV_{OUT}19$	37	$D_{IN}D$	62	$HV_{OUT}69$	87	$HV_{OUT}44$
13	$HV_{OUT}18$	38	V_{DD}	63	$HV_{OUT}68$	88	$HV_{OUT}43$
14	$HV_{OUT}17$	39	$\overline{POL}$	64	$HV_{OUT}67$	89	$HV_{OUT}42$
15	$HV_{OUT}16$	40	$\overline{LE}$	65	$HV_{OUT}66$	90	$HV_{OUT}41$
16	$HV_{OUT}15$	41	CLK	66	$HV_{OUT}65$	91	$HV_{OUT}40$
17	$HV_{OUT}14$	42	DIR	67	$HV_{OUT}64$	92	$HV_{OUT}39$
18	$HV_{OUT}13$	43	$\overline{BL}$	68	$HV_{OUT}63$	93	$HV_{OUT}38$
19	$HV_{OUT}12$	44	GND	69	$HV_{OUT}62$	94	$HV_{OUT}37$
20	$HV_{OUT}11$	45	$D_{OUT}D$	70	$HV_{OUT}61$	95	$HV_{OUT}36$
21	$HV_{OUT}10$	46	$D_{OUT}C$	71	$HV_{OUT}60$	96	$HV_{OUT}35$
22	$HV_{OUT}9$	47	$D_{OUT}B$	72	$HV_{OUT}59$	97	$HV_{OUT}34$
23	$HV_{OUT}8$	48	$D_{OUT}A$	73	$HV_{OUT}58$	98	$HV_{OUT}33$
24	$HV_{OUT}7$	49	HVGND	74	$HV_{OUT}57$	99	$HV_{OUT}32$
25	$HV_{OUT}6$	50	V_{PP}	75	$HV_{OUT}56$	100	$HV_{OUT}31$

Package Outlines



top view

100-Lead Plastic Quad Flat Package
("Gullwing" Package)

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