

# 64-Channel Serial To Parallel Converter With P-Channel Open Drain Controllable Output Current

## Ordering Information

Device	Package Options			
	80-Lead Quad Ceramic Gullwing	80 Lead Quad Plastic Gullwing	Die	80 Lead Quad Ceramic Gullwing (MIL-Std-833 Processed*)
HV57009	HV57009DG	HV57009PG	HV57009X	RBHV57009DG

\* For Hi-Rel process flows, refer to page 5-3 of the Databook.

## Features

- Processed with HVCMOS® technology
- 5V CMOS Logic
- Output voltage up to -85V
- Output current source control
- 16MHz equivalent data rate
- Latched data outputs
- Forward and reverse shifting options (DIR pin)
- Diode to  $V_{DD}$  allows efficient power recovery
- Hi-Rel processing available

## Absolute Maximum Ratings

Supply voltage, $V_{DD}^1$	-0.5V to +7.5V	
Output Voltage, $V_{NN}^1$	$V_{DD} + 0.5V$ to -95V	
Logic input levels <sup>1</sup>	-0.3V to $V_{DD} + 0.3V$	
Ground Current <sup>2</sup>	1.5A	
Continuous total power dissipation <sup>3</sup>	Plastic	1200mW
	Ceramic	1900mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to +125°C
Storage temperature range	-65°C to +150°C	
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	260°C	

### Notes:

1. All voltages are referenced to  $V_{SS}$ .
2. Limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

## General Description

The HV570 is a low-voltage serial to high-voltage parallel converter with P-channel open drain outputs. This device has been designed for use as a driver for plasma panels.

The device has two parallel 32-bit shift registers, permitting data rate twice the speed of one (they are clocked together). There are also 64 latches and control logic to perform the blanking of the outputs.  $HV_{OUT1}$  is connected to the first stage of the first shift register through the blanking logic. Data is shifted through the shift registers on the logic low to high transition of the clock. The DIR pin causes CCW shifting when connected to  $V_{SS}$ , and CW shifting when connected to  $V_{DD}$ . A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ( $HV_{OUT64}$ ). Operation of the shift register is not affected by the  $\overline{LE}$  (latch enable), or the  $\overline{BL}$  (blanking) inputs. Transfer of data from the shift registers to latches occurs when the LE input is high. The data in the latches is stored when LE is low.

The HV570 has 64 channels of output constant current sourcing capability. They are adjustable from 0.1 to 2.0mA through one external resistor or a current source.

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# Electrical Characteristics

## DC Characteristics (All voltages are referenced to $V_{SS}$ , $V_{SS} = 0$ , $T_A = 25^\circ\text{C}$ )

Symbol	Parameter	Min	Max	Units	Conditions
$I_{DD}$	$V_{DD}$ supply current		15	mA	$V_{DD} = V_{DD, \text{max}}$ $f_{CLK} = 8\text{MHz}$
$I_{NN}$	High voltage supply current		-10	$\mu\text{A}$	Outputs off, $HV_{OUT} = -85\text{V}$ (total of all outputs)
$I_{DDQ}$	Quiescent $V_{DD}$ supply current		100	$\mu\text{A}$	All inputs = $V_{DD}$ , except $+IN = V_{SS} = \text{GND}$
$V_{OH}$	High-level output	Data out	$V_{DD} - 0.5$	V	$I_O = -100\mu\text{A}$
		$HV_{OUT}$	+1	$V_{DD}$	$I_O = -2\text{mA}$
$V_{OL}$	Low-level output	Data out	+0.5	V	$I_O = 100\mu\text{A}$
$I_{IH}$	High-level logic input current		1	$\mu\text{A}$	$V_{IH} = V_{DD}$
$I_{IL}$	Low-level logic input current		-1	$\mu\text{A}$	$V_{IL} = 0\text{V}$
$I_{CS}$	HV output source current		-2	mA	$V_{REF} = 2\text{V}$ , $R_{EXT} = 1\text{K}$ , see Figures 8a and 8b
		-0.1		mA	$V_{REF} = 0.1\text{V}$ , $R_{EXT} = 1\text{K}$ , see Figure 8a and 8b
$\Delta I_{CS}$	HV output source current for $I_{REF} = 2.0\text{mA}$		10	%	$V_{REF} = 2\text{V}$ , $R_{EXT} = 1\text{K}$

**Notes** 1: Current going out of the chip is considered negative.

## AC Characteristics (Logic signal inputs and Data inputs have $t_r, t_f \leq 5\text{ns}$ [10% and 90% points] for measurements)

Symbol	Parameter	Min	Max	Units	Conditions
$f_{CLK}$	Clock frequency	DC	8	MHz	Per register
$t_{WL}, t_{WH}$	Clock width high or low	62		ns	
$t_{SU}$	Data set-up time before clock rises	10		ns	
$t_H$	Data hold time after clock rises	15		ns	
$t_{ON}, t_{OFF}$	Time for latch enable to $HV_{OUT}$		500	ns	$C_L = 15\text{pF}$
$t_{DHL}$	Delay time clock to data high to low		70	ns	$C_L = 15\text{pF}$
$t_{DLH}$	Delay time clock to data low to high		70	ns	$C_L = 15\text{pF}$
$t_{DLE}$	Delay time clock to $\overline{LE}$ low to high	25		ns	
$t_{WLE}$	Width of $\overline{LE}$ pulse	25		ns	
$t_{SLE}$	$\overline{LE}$ set-up time before clock rises	0		ns	
$t_r, t_f$	Maximum allowable clock rise and fall time (10% and 90% points)		100	ns	

# Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
$V_{DD}$	Logic supply voltage	4.5	5.5	V	
$HV_{OUT}$	HV output off voltage	-85	$V_{DD}$	V	
$V_{IH}$	High-level input voltage	$V_{DD} - 1.2V$	$V_{DD}$	V	
$V_{IL}$	Low-level input voltage	0	1.2	V	
$f_{CLK}$	Clock frequency per register	DC	8	MHz	
$T_A$	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C

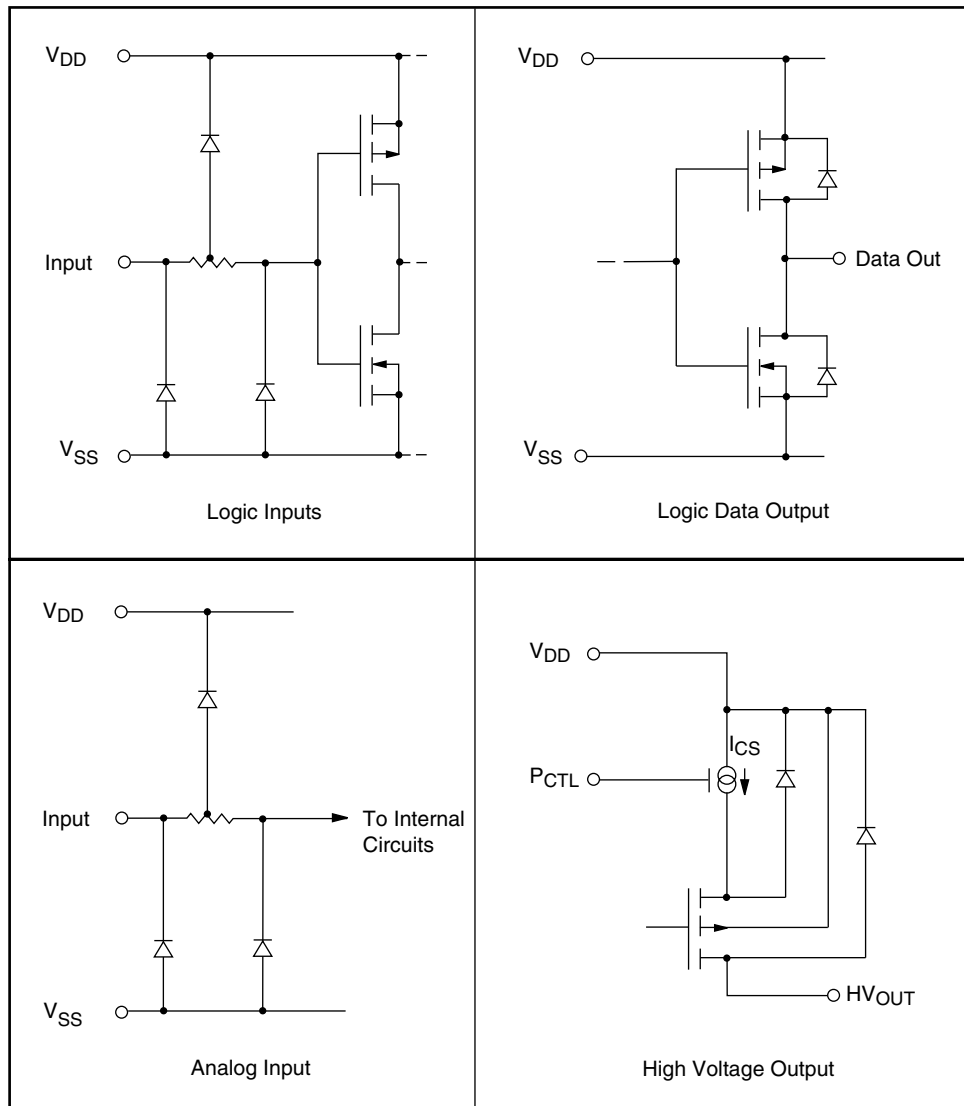
**Note:**

Power-up sequence should be the following:

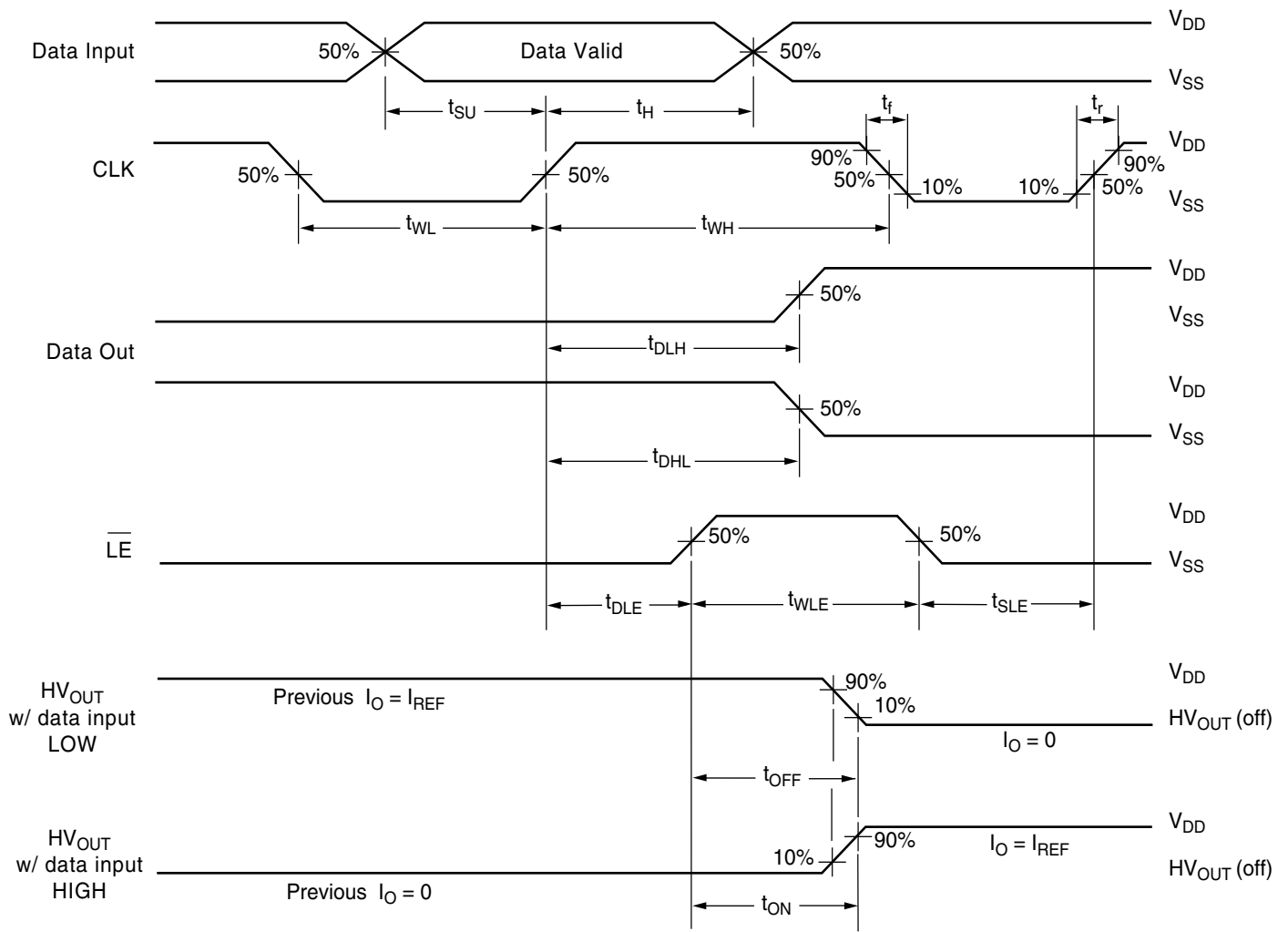
1. Connect ground.
2. Apply  $V_{DD}$ .
3. Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

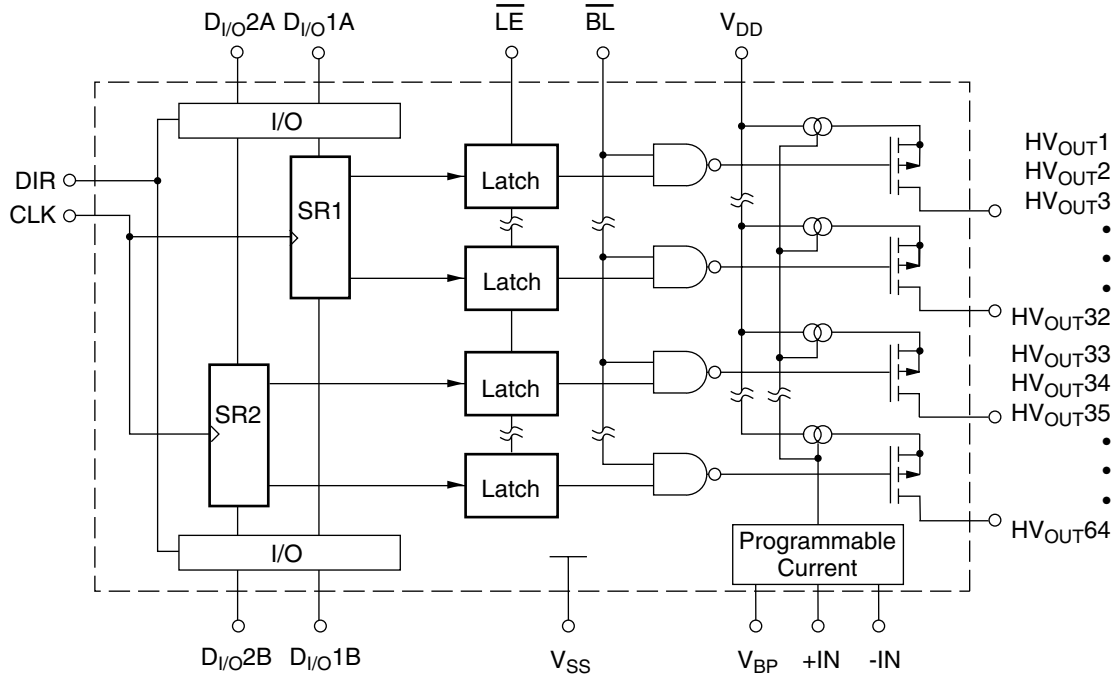
## Figure 1: Input and Output Equivalent Circuits



**Figure 2: Switching Waveforms**



**Figure 3: Functional Block Diagram**



**Note:** Each SR (shift register) provides 32 outputs. SR1 supplies outputs 1 to 32 and SR2 supplies outputs 33 to 64.

**Figure 4: Function Table**

Function	Inputs					Outputs		
	Data In	CLK	$\overline{LE}$	$\overline{BL}$	DIR	Shift Reg	HV Outputs	Data Out
All O/P High	X	X	X	L	X	*	ON	*
Data Falls Through (Latches Transparent)	L		H	H	X	L...L	ON	L
	H		H	H	X	H...H	OFF	H
Data Stored in Latches	X	X	L	H	X	*	Inversion of Stored Data	*
I/O Relation	$D_{I/O}1-2A$		H	H	H	$Q_n \rightarrow Q_{n+1}$	New ON or OFF	$D_{I/O}1-2B$
	$D_{I/O}1-2A$		L	H	H	$Q_n \rightarrow Q_{n+1}$	Previous ON or OFF	$D_{I/O}1-2B$
	$D_{I/O}1-2B$		L	H	L	$Q_n \rightarrow Q_{n-1}$	Previous ON or OFF	$D_{I/O}1-2A$
	$D_{I/O}1-2B$		H	H	L	$Q_n \rightarrow Q_{n-1}$	New ON or OFF	$D_{I/O}1-2A$

**Notes:**

\* = dependent on previous stage's state. See Figure 7 for  $D_{IN}$  and  $D_{OUT}$  pin designation for CW and CCW shift.

H =  $V_{DD}$  (Logic)/ $V_{NN}$  (HV Outputs)

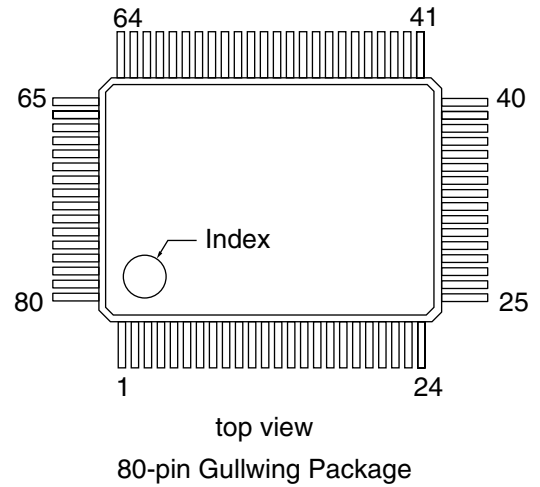
L =  $V_{SS}$

# Figure 5: Pin Configurations

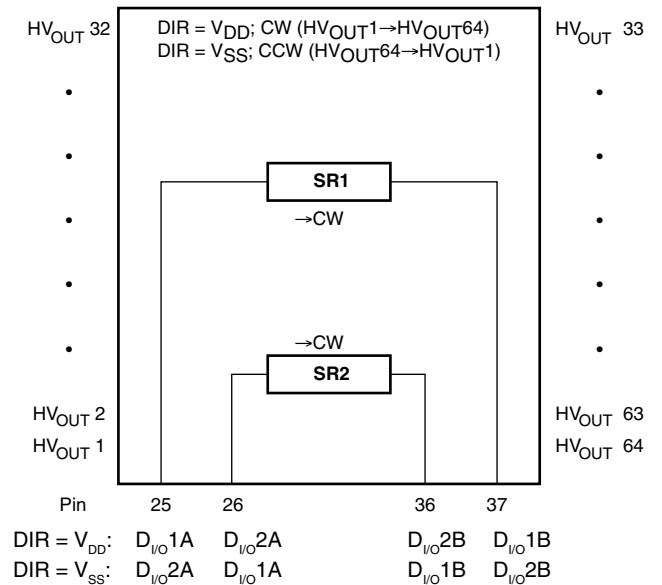
## 80-pin Gullwing Package

Pin	Function	Pin	Function
1	HV <sub>OUT</sub> 24	41	HV <sub>OUT</sub> 64
2	HV <sub>OUT</sub> 23	42	HV <sub>OUT</sub> 63
3	HV <sub>OUT</sub> 22	43	HV <sub>OUT</sub> 62
4	HV <sub>OUT</sub> 21	44	HV <sub>OUT</sub> 61
5	HV <sub>OUT</sub> 20	45	HV <sub>OUT</sub> 60
6	HV <sub>OUT</sub> 19	46	HV <sub>OUT</sub> 59
7	HV <sub>OUT</sub> 18	47	HV <sub>OUT</sub> 58
8	HV <sub>OUT</sub> 17	48	HV <sub>OUT</sub> 57
9	HV <sub>OUT</sub> 16	49	HV <sub>OUT</sub> 56
10	HV <sub>OUT</sub> 15	50	HV <sub>OUT</sub> 55
11	HV <sub>OUT</sub> 14	51	HV <sub>OUT</sub> 54
12	HV <sub>OUT</sub> 13	52	HV <sub>OUT</sub> 53
13	HV <sub>OUT</sub> 12	53	HV <sub>OUT</sub> 52
14	HV <sub>OUT</sub> 11	54	HV <sub>OUT</sub> 51
15	HV <sub>OUT</sub> 10	55	HV <sub>OUT</sub> 50
16	HV <sub>OUT</sub> 9	56	HV <sub>OUT</sub> 49
17	HV <sub>OUT</sub> 8	57	HV <sub>OUT</sub> 48
18	HV <sub>OUT</sub> 7	58	HV <sub>OUT</sub> 47
19	HV <sub>OUT</sub> 6	59	HV <sub>OUT</sub> 46
20	HV <sub>OUT</sub> 5	60	HV <sub>OUT</sub> 45
21	HV <sub>OUT</sub> 4	61	HV <sub>OUT</sub> 44
22	HV <sub>OUT</sub> 3	62	HV <sub>OUT</sub> 43
23	HV <sub>OUT</sub> 2	63	HV <sub>OUT</sub> 42
24	HV <sub>OUT</sub> 1	64	HV <sub>OUT</sub> 41
25	D <sub>I/O</sub> 1A	65	HV <sub>OUT</sub> 40
26	D <sub>I/O</sub> 2A	66	HV <sub>OUT</sub> 39
27	N/C	67	HV <sub>OUT</sub> 38
28	N/C	68	HV <sub>OUT</sub> 37
29	LE	69	HV <sub>OUT</sub> 36
30	CLK	70	HV <sub>OUT</sub> 35
31	BL	71	HV <sub>OUT</sub> 34
32	V <sub>SS</sub>	72	HV <sub>OUT</sub> 33
33	DIR	73	HV <sub>OUT</sub> 32
34	V <sub>DD</sub>	74	HV <sub>OUT</sub> 31
35	-IN	75	HV <sub>OUT</sub> 30
36	D <sub>I/O</sub> 2B	76	HV <sub>OUT</sub> 29
37	D <sub>I/O</sub> 1B	77	HV <sub>OUT</sub> 28
38	N/C	78	HV <sub>OUT</sub> 27
39	+IN	79	HV <sub>OUT</sub> 26
40	V <sub>BP</sub>	80	HV <sub>OUT</sub> 25

## Figure 6: Package Outline



## Figure 7: Shift Register Operation



### Notes:

1. Pin designation for DIR = V<sub>DD</sub>.
2. A 0.1μF capacitor is needed between V<sub>DD</sub> and V<sub>BP</sub> (pin 40) for better output current stability and to prevent transient cross-coupling between outputs. See Fig. 8a and 8b.

# Typical Current Programming Circuits

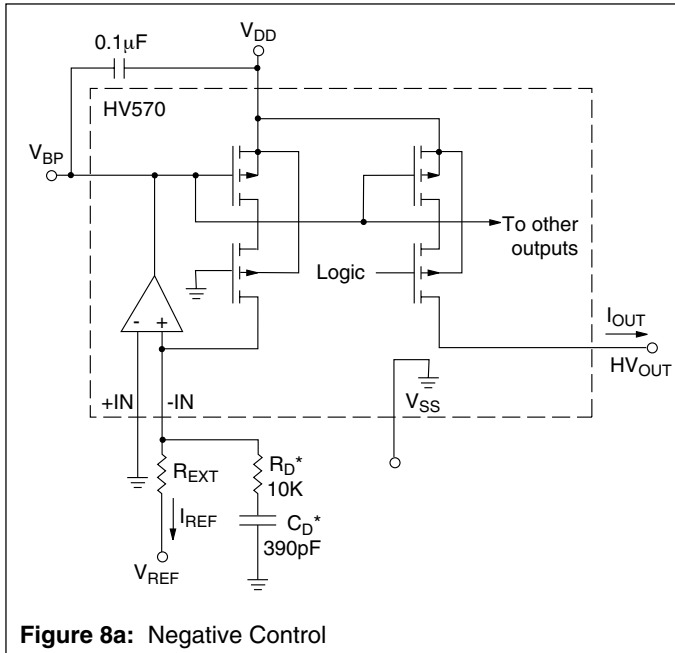


Figure 8a: Negative Control

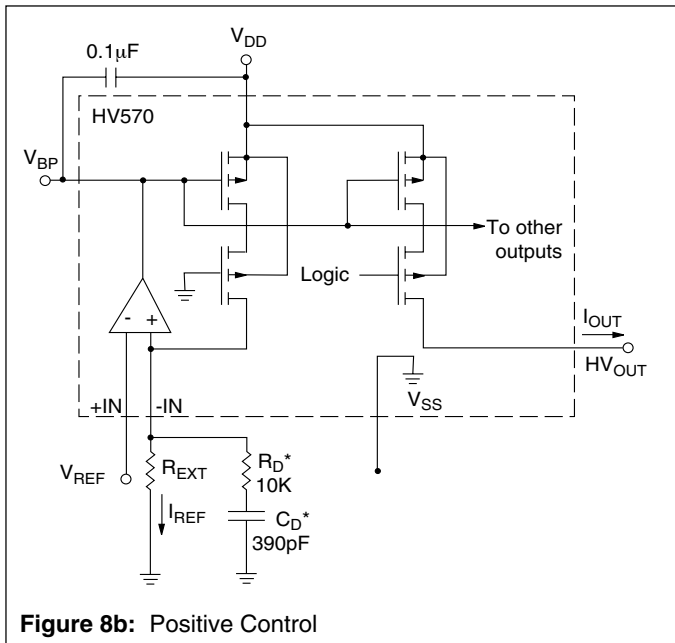


Figure 8b: Positive Control

\*Required if  $R_{EXT} > 10K$  or  $R_{EXT}$  is replaced by a constant current source.

$$\text{Since } I_{OUT} = I_{REF} = \frac{|V_{REF}|}{R_{EXT}}$$

Therefore, if  $I_{OUT} = 2\text{mA}$  and  $V_{REF} = -5\text{V} \rightarrow R_{EXT} = 2.5\text{K}\Omega$ .

If  $I_{OUT} = 1\text{mA}$  and  $R_{EXT} = 1\text{K}\Omega \rightarrow V_{REF} = -1\text{V}$ .

If  $R_{EXT} > 10\text{K}\Omega$ , add series network  $R_D$  and  $C_D$  to ground for stability as shown.

This control method behaves linearly as long as the operational amplifier is not saturated. However, it requires a negative power source and needs to provide a current  $I_{REF} = I_{OUT}$  for each HV570 chip being controlled.

If  $HV_{OUT} \geq +1\text{V}$ , the  $HV_{OUT}$  cascode may no longer operate as a perfect current source, and the output current will diminish. This effect depends on the magnitude of the output current.

Given  $I_{OUT}$  and  $V_{REF}$ , the  $R_{EXT}$  can be calculated by using:

$$R_{EXT} = \frac{V_{REF}}{I_{REF}} = \frac{V_{REF}}{I_{OUT}}$$

The intersection of a set of  $I_{OUT}$  and  $V_{REF}$  values can be located in the graph shown below. The value picked for  $R_{EXT}$  must always be in the shaded area for linear operation. This control method has the advantage that  $V_{REF}$  is positive, and draws only leakage current. If  $R_{EXT} > 10\text{K}$ , add series network  $R_D$  and  $C_D$  to ground for stability as shown.

Note: Lower reference current  $I_{REF}$ , results in higher distortion,  $\Delta I_{CS}$ , on the output.

