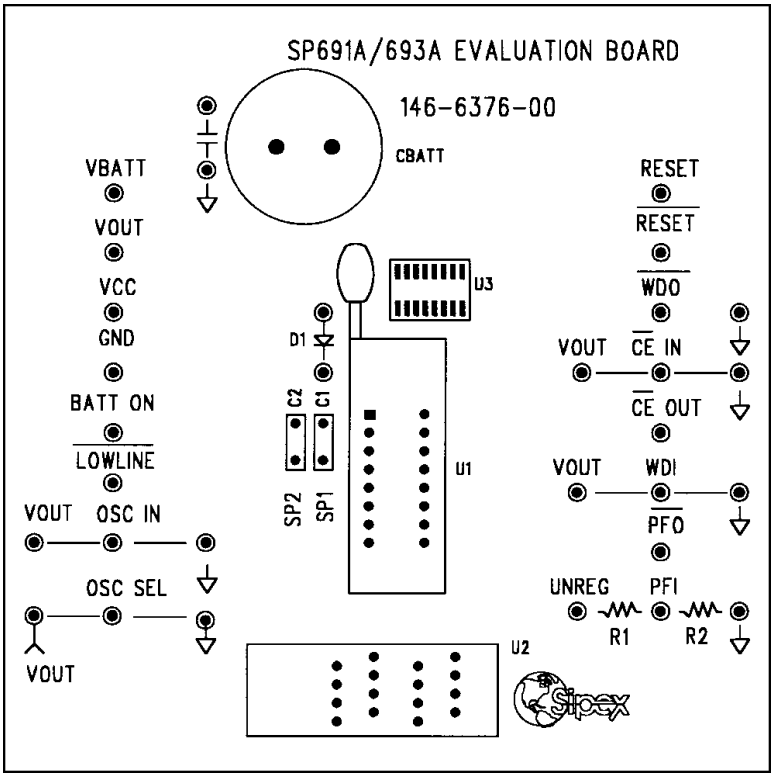
SP691A/693A
Evaluation Board Manual

- Easy Evaluation for the SP691A/693A Microprocessor Supervisory Circuit
- Probe Points Accessible for all SP691A/693A Pins & Input Options
- 16 Pin Narrow SOIC or DIP Sockets Available for the SP691A/693A Circuit
- Pin compatible upgrade to MAX691A, 693A, 800L, 800M



DESCRIPTION

The **SP691A/693A Evaluation Board** is designed to help analyze the many functions of the SP691A/693A µP Supervisory circuit. The evaluation board provides easy probe access points to all SP691A/693A pins so that the user can measure electrical characteristics and waveforms of each signal. The **SP691A/693A Evaluation Board** also provides solder pads for DIP or SOIC packages, as well as options for DIP or SOIC sockets for easy evaluation of multiple devices.

The next two sections describe the SP691A/693A Board Layout and Using the SP691A/693A Evaluation Boards. A table of SP691A/693A Pin Assignments is also included with a section on Power Supply Connections. A SP691A/693A Evaluation Board List of Materials is provided with some manufacturers part numbers to use as a reference. Finally, a schematic is included of the **SP691A/693A Evaluation Board**.

BOARD LAYOUT

The **SP691A/693A Evaluation Board** has been designed to easily and conveniently provide access to all pins of the SP691A/693A device under test. Position the board with the silkscreen lettering upright (also see drawing on the front page of this manual) and you will see two vertical rows of eight pins each, which represent the 16 pins of the SP691A/693A device starting in the top left with V_{BATT} as pin one. The pin receptacles are raised female pins which can accommodate easy-hook connection leads for power and meter connections, as well as scope probe hooks and grounds for waveform measurements.

The 16 pin SP691A/693A may be installed in one of 3 locations: U1 for DIP or DIP sockets, U3 for SOICs or U2 for SOIC sockets. The five input pins for the SP691A/693A are provided with extra Input Probe Points for connecting inputs to these pins. For example pin 11 WDI has nearby pins V_{OUT} and GND to connect to for evaluation of WDI timeout. These female receptacle pins can be jumpered together with easy-hook connectors or stripped back solid wire leads. In the case of inputs OSC IN, OSC SEL or PFI, a resistor or capacitor with leads may be pushed into the female receptacle pins to make easy connections. Also, mating male pins (see List of Materials) may be soldered to the components and inserted into the receptacle pins.

USING THE EVALUATION BOARD

Connect the **SP691A/693A Evaluation Board** to the power supplies for V_{CC} and V_{BATT} (see the section Power Supply Connections following the table SP691A/693A Pin Assignments). It is good practice to not switch power on until power connections are made to the evaluation board.

Evaluating Pin Functions

Pin 1 – V_{BATT} – Backup-Battery Input. Connect to external supply, battery or capacitor and charging circuit. If this pin is not used, connect to GND.

Pin 2 – V_{OUT} – Output Supply Voltage. This function is used to provide power supply switching of either V_{CC} or V_{BATT} to an external device like a CMOS RAM to ensure a constant supply for the memory. To evaluate this function, vary the V_{CC} voltage for a set V_{BATT} voltage until you simulate the following conditions: V_{OUT} connects to V_{CC} when V_{CC} is greater than V_{BATT} and V_{CC} is above the reset threshold. When V_{CC} falls below V_{BATT} and V_{CC} is below the reset threshold, V_{OUT} connects to V_{BATT}. Start with V_{BATT} voltage of about 2.8 to 4.0V and vary V_{CC} from 0V to 5V to 0V and observe V_{OUT}. (Note: a 0.1µF bypass capacitor (C1) is connected from V_{OUT} to GND). Connect V_{OUT} to V_{CC} if no backup battery is used.

Pin 3 – V_{CC} – Input Supply Voltage - +5V input. A 0.1(F bypass capacitor (C2) is connected from V_{CC} to GND.

Pin 4 – GND – Ground reference for all signals.

Pin 5 – BATT ON – Battery On Output. Goes high when V_{OUT} switches to V_{BATT}. Goes low when V_{OUT} switches to V_{CC}. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.

Pin 6 - $\overline{\text{LOWLINE}}$ - $\overline{\text{LOWLINE}}$ Output goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold. The output can be used to generate a NMI (non-maskable interrupt) if the unregulated supply is inaccessible.

Pin 7 – OSC IN – External Oscillator Input. When OSC SEL is unconnected or driven high, a 10µA pull-up connects from V_{OUT} to OSC IN, the internal oscillator sets the reset and watchdog timeout periods, and OSC IN selects between fast and slow watchdog timeout periods. When OSC SEL is driven low, the reset and watchdog timeout periods may be set either by a capacitor from OSC IN to ground or by an external clock at OSC IN.

Pin 8 – OSC SEL – Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset and watchdog timeout periods. When OSC SEL is low, the external oscillator input (OSC IN) is enabled. OSC SEL has a 10µA pull-up.

Pin 9 – PFI – Power-Fail Input. This is the non-inverting input to the power-fail comparator. When PFI is less than 1.25V, PFO_N goes low. Connect PFI to GND or VOUT when not used. Connect external divider R1 & R2 to Probe Pins and connect Unregulated Voltage to UNREG for Power Fail monitoring.

Pin 10 – $\overline{PFO}$ – Power-Fail Output. This is the output of the power-fail comparator. $\overline{PFO}$, goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.

Pin 11 – WDI – Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{WDO}$ goes low and reset is asserted for the reset timeout period. $\overline{WDO}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected. For a simple check of watchdog function, connect WDI to either Probe pins GND or V_{OUT} to cause $\overline{WDO}$ to go to a Logic Low.

Pin 12 – $\overline{CE}$ OUT – Chip-Enable Output. The Chip-Enable (CE) function $\overline{CE}$ OUT provides internal gating of chip enable signals to prevent erroneous data from corrupting the CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and all CE transitions are passed from $\overline{CE}$ IN to $\overline{CE}$ OUT. When Reset is asserted, this path is disabled. Note that $\overline{CE}$ OUT goes low (active) only when $\overline{CE}$ IN is low and V_{CC} is above the reset threshold. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will stay low for 12µs or until $\overline{CE}$ IN goes high, whichever occurs first.

Pin 13 – $\overline{CE}$ IN – Chip-Enable Input. The Input to chip-enable gating circuit. Connect to GND or V_{OUT} if not used.

Pin 14 –$\overline{WDO}$ – Watchdog Output. $\overline{WDO}$ goes low and reset is asserted if WDI remains either high or low longer than the watchdog timeout period. $\overline{WDO}$ returns high on the next transition at WDI. $\overline{WDO}$ remains high if WDI is unconnected. $\overline{WDO}$ is also high when RESET is asserted.

Pin 15 – $\overline{RESET}$ – $\overline{RESET}$ output goes low whenever V_{CC} falls below the reset threshold. $\overline{RESET}$ will remain low for 200ms (when internal oscillator is used) after V_{CC} crosses the reset threshold on power-up.

Pin 16 – RESET – RESET Output goes high whenever V_{CC} falls below the reset threshold. RESET is open drain and is the inverse of $\overline{RESET}$.

Note: To accurately measure the extremely small supply current in Battery Back-up mode, you need to cut split pads SP1 & SP2 (solder side of board) severing connections to C1 & C2 which would have leakage currents in the measurement range. Also, remove charging circuit components CBATT and D1 if they are installed.

SP691A/693A Pin Assignments

Pin #	Pin Name	Pin Function	Active Level	Input Pin Points
1	V_{BATT}	Backup-Battery Input	NA	
2	V_{OUT}	Output Supply Voltage	NA	
3	V_{CC}	Input Supply Voltage	NA	
4	GND	Ground for all Signals	NA	
5	BATT ON	Battery On Output	HIGH	
6	$\overline{\text{LOWLINE}}$	Lowline Output	LOW	
7	OSC IN	Oscillator Input	NA	V_{OUT} & GND
8	OSC SEL	Oscillator Select	NA	V_{OUT} & GND
9	PFI	Power-Fail Input	HIGH	R1 & R2
10	$\overline{\text{PFO}}$	Power-Fail Output	LOW	
11	WDI	Watchdog Input	Transitions	V_{OUT} & GND
12	$\overline{\text{CE}}$ OUT	Chip-Enable Output	LOW	
13	$\overline{\text{CE}}$ IN	Chip-Enable Input	LOW	V_{OUT} & GND
14	$\overline{\text{WDO}}$	Watchdog Output	LOW	
15	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output	LOW	
16	RESET	RESET Output	HIGH	

Power Supply Connections

Pin 3 – V_{CC} – connect to external +5 VDC supply.

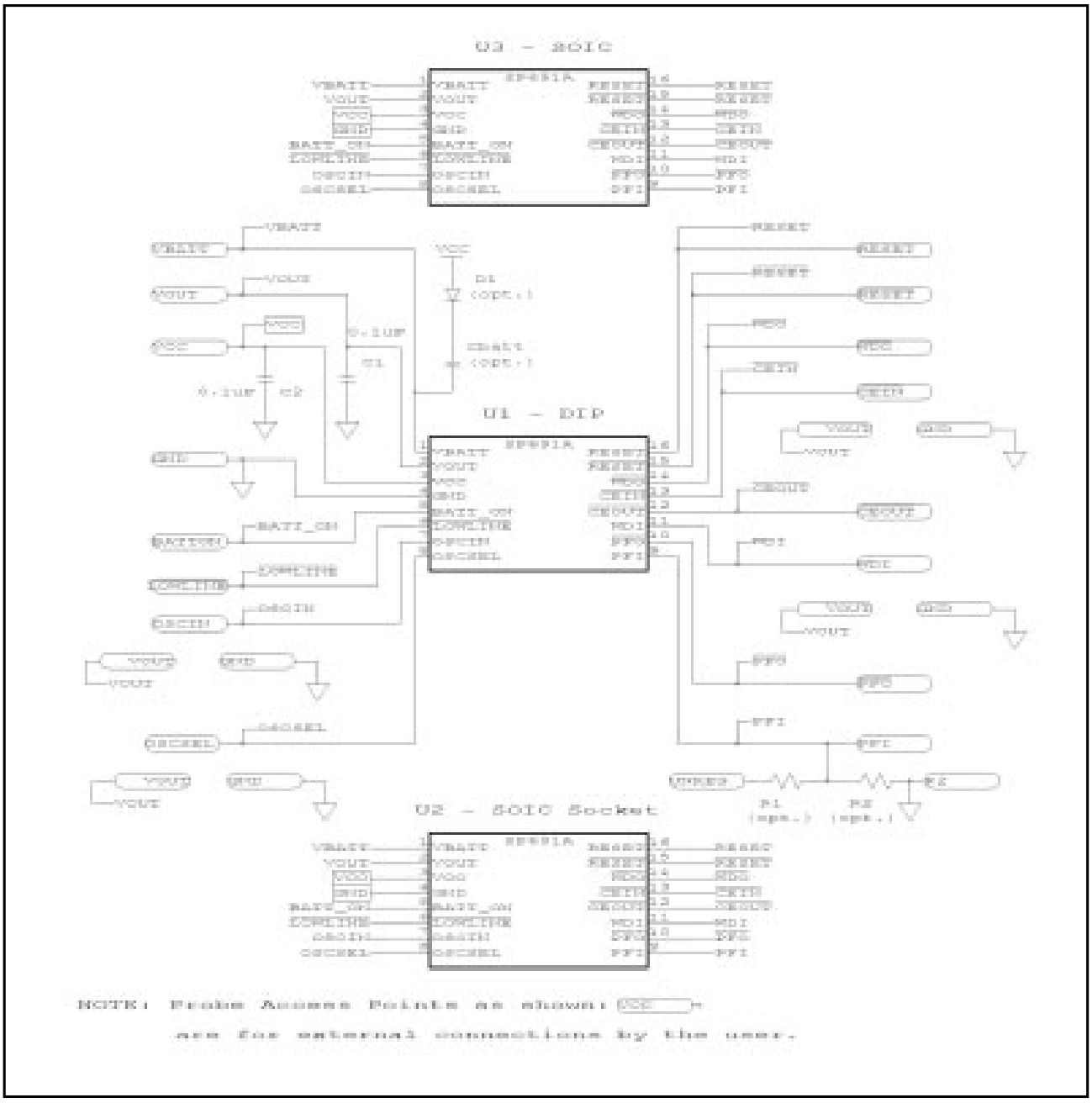
Pin 1 – V_{BATT} – connect to external V+ supply of 2.8 to 4.0 VDC, or install capacitor C_{BATT} and charging diode D1 (see List of Materials).

Pin 4 – GND – connect to negative or ground of +5VDC supply and ground of V+ supply for V_{BATT}
Note: Ensure V_{CC}, V_{BATT} and GND connections are made before operating device.

SP691A/693A Evaluation Board List of Materials

Component	Part Number	Manufacturer	Ref. Des.	Qty.
µP Supervisor IC	SP691ACN	Sipex	U3	1
Pin Receptacle-Female	300-1150-1472-7040	Mil-Max Mfg.		26
Ceramic Capacitor 0.1µF		Generic	C1, 2	2
Al. Spacers - 0.5"	8414	Keystone Elec.		4
6-32 Hex Nut		Generic		4
Optional:				
16 Pin DIP Socket	216-3340-00-0602	3M-Textool	U1	1
16 Pin SOIC Socket	216-7383-55-1902	3M-Textool	U2	1
Maxcap 1F 5.5V	LC055105A	Cesiwid Inc.	CBATT	1
Signal Diode		Generic	D1	1
Pin Receptacle-Male	3137-3002-10-0080	Mill-Max Mfg.		26

SP691A/693A Evaluation Board Schematic



ORDERING INFORMATION

Model	Package
SP691ANEB	SP691ACN Evaluation Board

SIGNAL PROCESSING EXCELLENCE

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