SC4612H
40V Synchronous Buck Controller

Description

SC4612H is a high performance synchronous buck controller that can be configured for a wide range of applications. The SC4612H utilizes synchronous rectified buck topology where high efficiency is the primary consideration. SC4612H can be used over a wide input voltage range with output voltage adjustable within limits set by the duty cycle boundaries.

SC4612H comes with a rich set of features such as regulated DRV supply, programmable soft-start, high current gate drivers, shoot through protection, R_{DS-ON} sensing with hiccup over current protection.

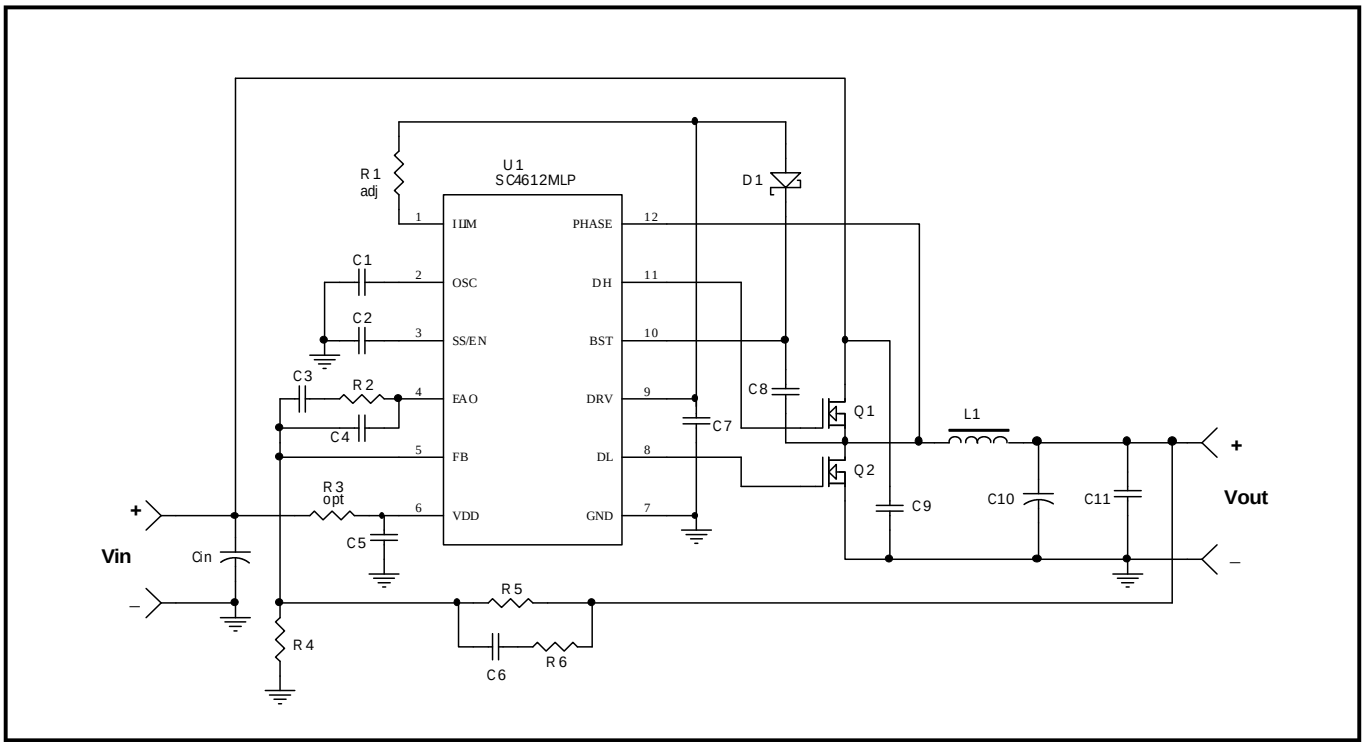
Features

- Wide input voltage range, 4.75V to 40V
- Internally regulated DRV
- 1.7A gate drive capability
- Low side R_{DS-ON} sensing with hiccup OCP
- Programmable current limit
- Programmable frequency up to 1.2 MHz
- Overtemperature protected
- Pre-bias startup
- Reference accuracy ±1%
- Available in MLPD-12 4 x 3 and SOIC-14 Pb-free packages. This product is fully WEEE and RoHS compliant

Applications

- Distributed power architectures
- Telecommunication equipment
- Servers/work stations
- Mixed signal applications
- Base station power management
- Point of use low voltage high current applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Bias Supply Voltage to GND	VDD	-0.3 to 45	V
PHASE to GND	VIN	-2 to +55	V
DRV, ILIM, DL to GND, BST, DH to PHASE		-0.3 to 10	V
EAO, SS/EN, FB, OSC to GND		-0.3 to +5	V
DRV Source Current (peak)		100	mA
Thermal Resistance Junction to Ambient (MLPD) (1)	θ_{JA}	45.3	°C/W
Thermal Resistance Junction to Case (MLPD)	θ_{JC}	11	°C/W
Thermal Resistance Junction to Ambient (SOIC) (1)	θ_{JA}	115	°C/W
Thermal Resistance Junction to Case (SOIC)	θ_{JC}	45	°C/W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Peak IR Reflow Temperature (10-40s)	$T_{IR\ Reflow}$	260	°C
Lead Temperature (10s), (SOIC-14)	T_{LEAD}	300	°C

All voltages with respect to GND. Positive currents are into, and negative currents are out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Data sheet for thermal limitations and considerations of packages.

Note:

(1). ThetaJA is calculated from a package in still air, mounted to a 3" x 4.5", 4 layer FR4PCB with thermal vias (if applicable) per JESD51 standards.

Recommended Operating Conditions

Performance is not guaranteed if the conditions below are exceeded.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	VDD		5		40	V
Ambient Temperature Range	T_A		-40		105	°C
Junction Temperature Range	T_J		-40		125	°C

Electrical Characteristics

Unless otherwise specified:
VIN = VDD = 12V, F_{OSC} = 600kHz, $T_A = T_J$ = 25°C.

Parameter	Test Conditions	Min	Typ	Max	Units
Bias Supply					
Quiescent Current	V_{DD} = 40V, No load, SS/EN = 0		5	7	mA
VDD Undervoltage Lockout					
Start Threshold		4.20	4.50	4.75	V
UVLO Hysteresis			400		mV
Drive Regulator					
DRV	10V ≤ V_{DD} ≤ 40V, I_{OUT} ≤ 1mA	7.3	7.8	8.3	V
Load Regulation	1mA ≤ I_{OUT} ≤ 70mA			100	mV
Oscillator					
Operation Frequency Range		100		1200	kHz
Initial Accuracy (1)	C_{OSC} = 160pF (Ref only)	540	600	660	kHz
Maximum Duty Cycle	$V_{DD} = V_{DR}$ = 8V; V_{OUT_NOM} = 5V; I_{OUT} = 0A V_{IN} adjust down to $V_{OUT} = 0.99 \cdot V_{OUT\_NOM}$	82			%
Ramp Peak to Valley (1)			850		mV
Oscillator Charge Current	V_{OSC} = 1V	90		110	µA
Current Limit (Low Side Rdson)					
Current Limit Threshold Voltage	See Pg. 12 & 13 on OCP		100		mV
Error Amplifier					
Feedback Voltage	T_J = 0 to +70°C	0.495	0.500	0.505	V
	T_J = -40 to +85°C	0.492	0.500	0.508	V
	T_J = -40 to +125°C	0.488	0.500	0.512	V
Input Bias Current	FB = 0.5V			200	nA
Open Loop Gain (1)			60		dB
Unity Gain Bandwidth (1)		7	10		MHz
Output Sink Current	Open Loop, FB = 0V		900		µA
Output Source Current	Open Loop, FB = 0.6V		1100		µA
Slew Rate (1)			1		V/µs

Electrical Characteristics (Cont.)

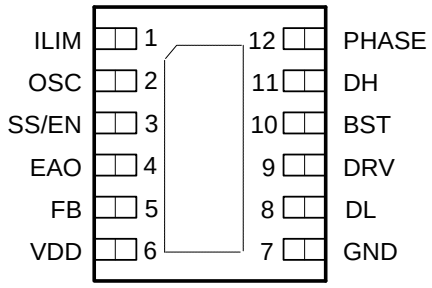
Unless otherwise specified:
VIN = VDD = 12V, F_{OSC} = 600kHz, $T_A = T_J$ = 25°C.

Parameter	Test Conditions	Min	Typ	Max	Units
SS/EN					
Disable Threshold Voltage				500	mV
Soft Start Charge Current			25		µA
Soft Start Discharge Current (1)			1		µA
Disable Low to Shut Down (1)			50		ns
Hiccup					
Hiccup duty cycle	C_{SS} = 0.1, current limit condition		1		%
Gate Drive					
Gate Drive On-Resistance (H)(2)	I_{SOURCE} = 100mA		3	4	Ω
Gate Drive On-Resistance (L)(2)	I_{SINK} = 100mA		3	4	Ω
DL Source/Sink Peak Current(2)	COUT = 2000pF	1.4	1.7		A
DH Source/Sink Peak Current(2)	COUT = 2000pF	1.4	1.7		A
Output Rise Time(2)	COUT = 2000pF		20		ns
Output Fall Time(2)	COUT = 2000pF		20		ns
Minimum Non-Overlap (1)			30		ns
Minimum On Time(2)				110	ns
Thermal Shutdown					
Shutdown Temperature (2)			165		°C
Thermal Shutdown Hysteresis (2)			15		°C

Notes:
(1) Guaranteed by design. Not production tested.
(2) Guaranteed by characterization.
(3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

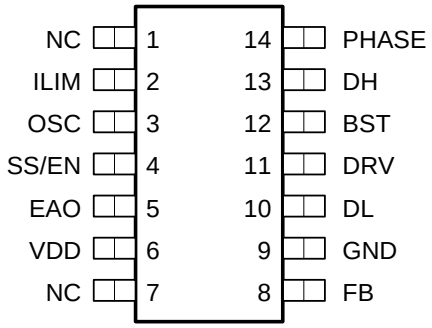
Pin Configurations

TOP VIEW



(12 Pin MLPD)

TOP VIEW



(14 Pin SOIC)

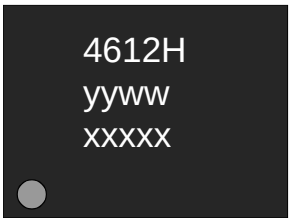
Ordering Information

Part Number[3]	Package[2]	Temp. Range (T_J)
SC4612HMLTRT	MLPD-12 4 x 3	-40°C to +125°C
SC4612HSTRT	SOIC-14	
SC4612HEVB[1]	EVALUATION BOARD	

Notes:
(1) When ordering please specify MLPD or SOIC package.
(2) Only available in tape and reel packaging. A reel contains 3000 devices for MLPD package and 2500 for SOIC package..
(3) Pb-free product. This product is fully WEEE and RoHS compliant.

Marking Information - MLPD

Top Mark



nnnn = Part Number (Example: 1531)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example:E9010)

Marking Information - SOIC

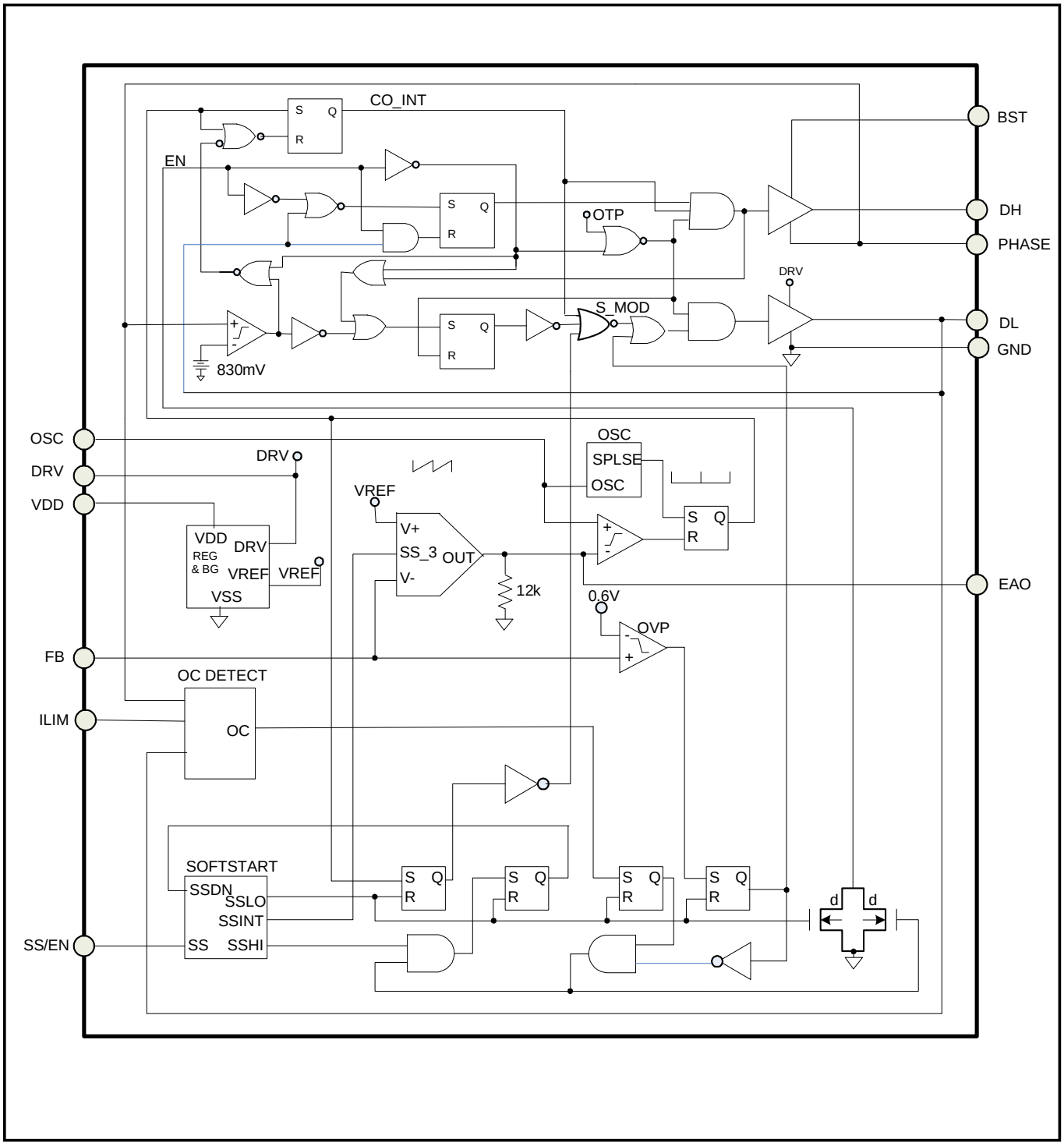
Top Mark

nnnn = Part Number (Example: SC4612H)
yyww =Date Code (Example: 0752)
xxxxx = Semtech Lot No. (Example:A01E90101)

Pin Descriptions

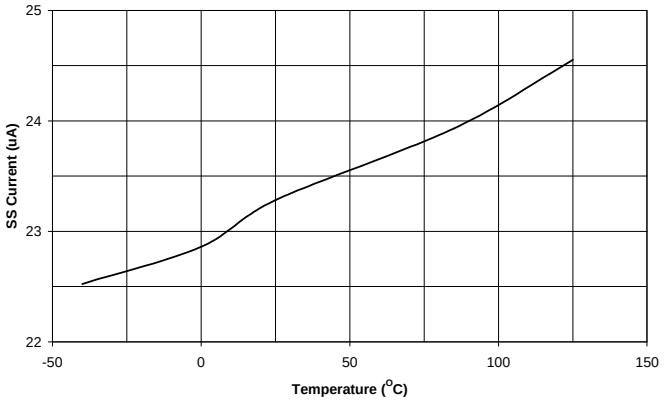
Pin # MLPD	Pin# SOIC	Pin Name	Pin Function
	1, 7	NC	No connection.
1	2	ILIM	The current limit programing resistor at this pin in conjunction with an internal current source programs the current limit threshold for the low side MOSFET R_{DS-ON} sensing. Once the voltage drop across the bottom MOSFET is larger than the programmed value, current limit condition occurs, and the hiccup current limit protection is activated.
2	3	OSC	Oscillator Frequency set pin. An external capacitor to GND will program the oscillator frequency. See Table 1 "Frequency vs. C_{OSC}" to determine oscillator frequency.
3	4	SS/EN	Soft Start pin. Internal current source connected to a single external capacitor will determine the soft-start duration for the output. Inhibits the chip if pulled down. $T_{SS} \approx \frac{C_{SS} \times 1.2}{I_{SS}}$
4	5	EAO	Error Amplifier Output. A compensation network is connected from this pin to FB.
5	8	FB	The inverting input of the error amplifier. Feedback pin is used to sense the output voltage via a resistive divider.
6	6	VDD	Bias supply. Also, VDD pin is internally used to provide the base drive to the internal pass transistor regulating the DRV supply.
7	9	GND	Ground.
8	10	DL	Drive Low. Gate drive for bottom MOSFET.
9	11	DRV	DRV supplies the external MOSFETs gate drive and the chips internal circuitry. This pin should be bypassed with a ceramic capacitor to GND. DRV is internally regulated from the external supply connected to VDD. If VDD is below 10V, the supply should be directly connected to the DRV pin.
10	12	BST	BST signal. Supply for high side driver; can be directly connected to an external supply or to a bootstrap circuit.
11	13	DH	Drive High. Gate drive for top MOSFET.
12	14	PHASE	The return path for the high side gate drive, also used to sense the voltage at the phase node for adaptive gate drive protection and the low-side R_{DS-ON} current sensing.
X	N/A	THERMAL PAD (GND)	Pad for heatsinking purposes. Connect to ground plane using multiple vias.

Block Diagram

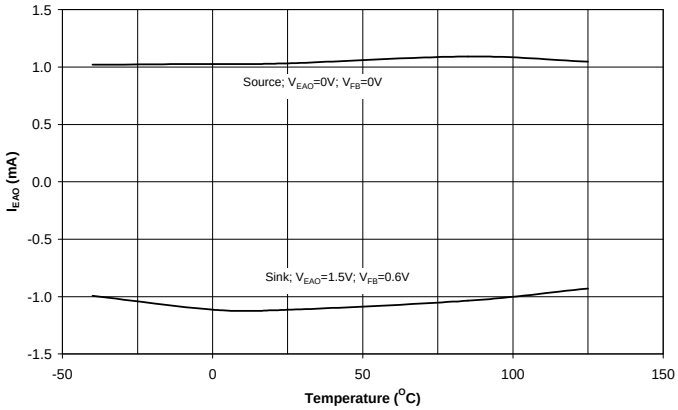


Typical Characteristics

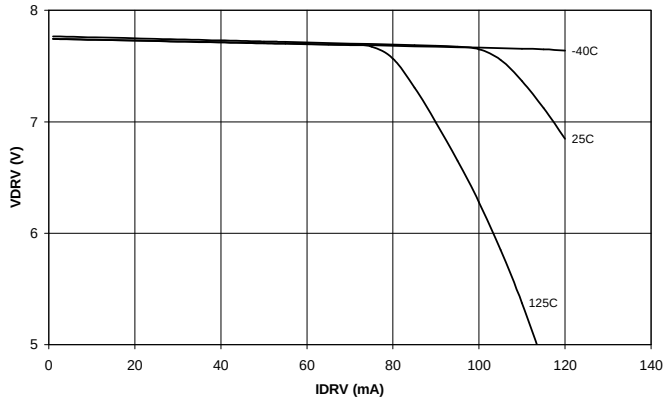
Typical Soft Start Current vs Temperature



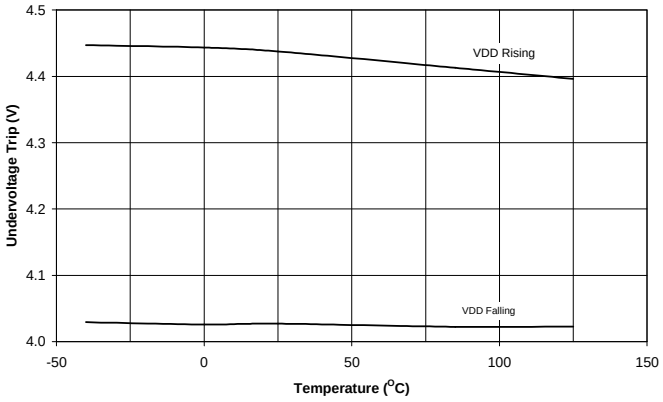
Typical Error Amp Output Current vs Temperature



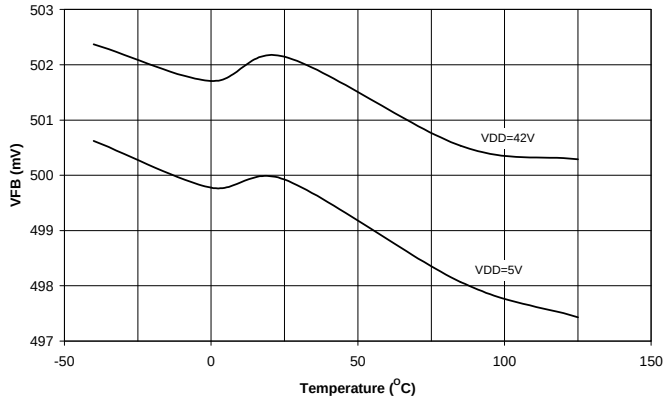
Typical DRV Voltage vs Load Current



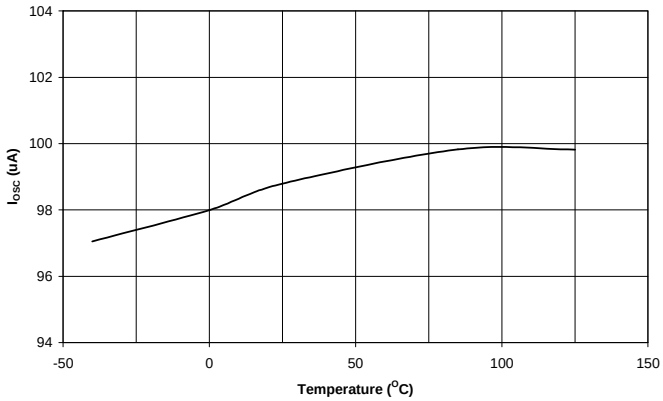
Typical UVLO vs Temperature



Typical VFB vs Temperature

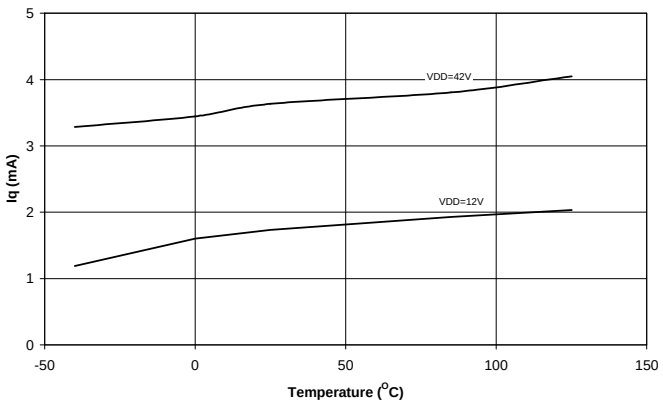


Typical Oscillator Charge Current vs Temperature

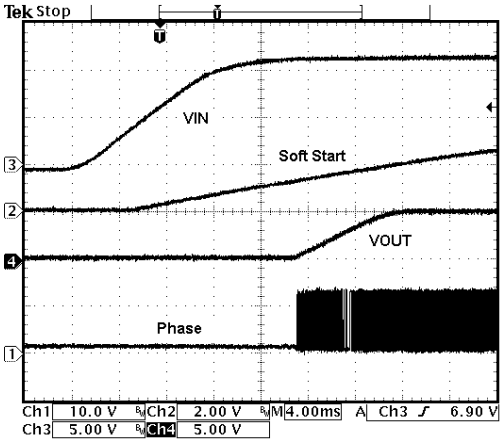


Typical Characteristics (Cont.)

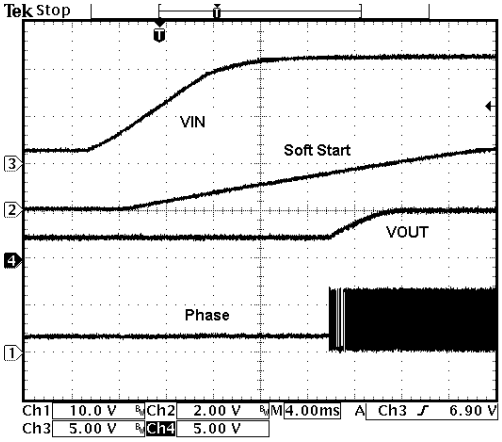
Typical VDD Quiescent current vs Temperature



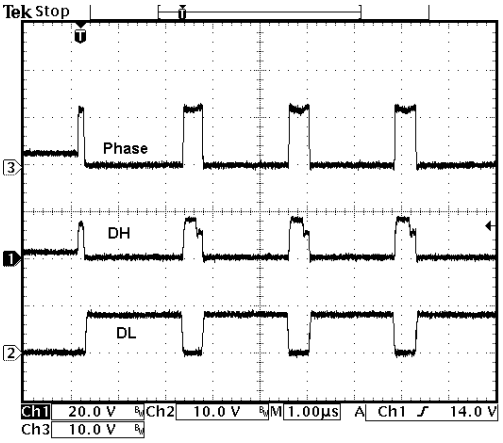
Start Up from VOUT = 0V



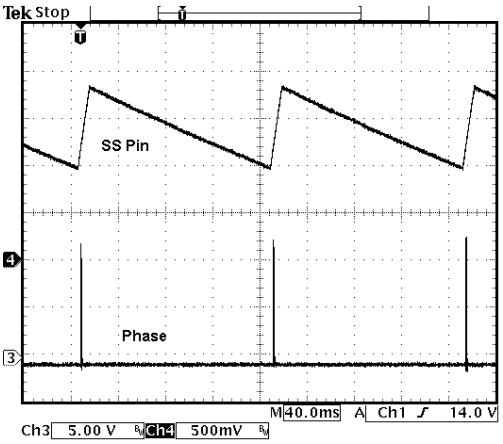
Start Up from VOUT = 2.5V



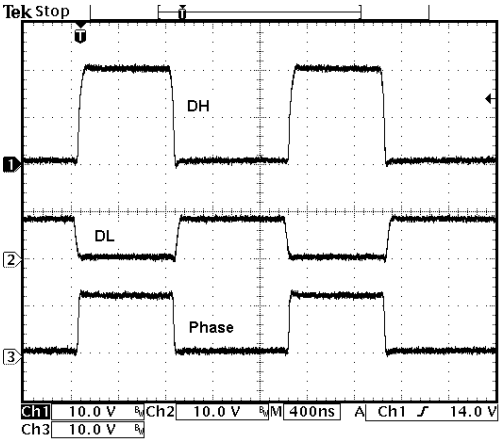
Start Up from VOUT = 2.5V
First DH/DL Pulses



Short Circuit Applied



Steady State Waveforms



Applications Information

INTRODUCTION

The SC4612H is a versatile voltage mode synchronous rectified buck PWM convertor, with an input supply (VIN) ranging from 4.5V to 40V designed to control and drive N-channel MOSFETs.
The power dissipation is controlled by allowing high speed and integration with the high drive currents to ensure low MOSFET switching loss. The synchronous buck configuration also allows converter sinking current from load without losing output regulation.

The internal reference is trimmed to 500mV with ± 1% accuracy, and the output voltage can be adjusted by an external resistor divider.

A fixed oscillator frequency (up to 1.2MHz) can be programmed by an external capacitor for design optimization.

Other features of the SC4612H include:

Wide input power voltage range (from 4.5V to 40V), low output voltages, externally programmable soft-start, hiccup over current protection, wide duty cycle range, thermal shutdown, and -40 to 125°C junction operating temperature range.

THEORY OF OPERATION

SUPPLIES

Two pins (VDD and DRV) are used to power up the SC4612H. If input supply (Vin) is less than 10V, tie DRV and VDD together.

This DRV supply should be bypassed with a low ESR 2.2uF (or greater) ceramic capacitor directly at the DRV to GND pins of the SC4612H.

The DRV supply also provides the bias for the low and the high side MOSFET gate drive.

The maximum rating for DRV supply is 10V and for applications where input supply is below 10V, it should be connected directly to VDD.

The internal pass transistor will regulate the DRV from an external supply connected to VDD to produce 7.8V typical at the DRV pin.

Soft Start / Shut down

The SC4612H performs a "pre-bias" type startup. This ensures that a pre-charged output capacitor will not cause the SC4612H to turn on the bottom FET during startup to discharge it, as a normal synchronous buck controller would do. An external capacitor on the SS/EN pin is used to set the Soft Start duration.

$$T_{SS} \approx \frac{0.5 \bullet C_{SS}}{25 \bullet 10^{-6}}$$

Startup is inhibited until VDD input reaches the UVLO threshold (typically 4.5V). Once VDD rises above UVLO, the external soft start capacitor begins to charge from an internal 25uA current source. When the SS/EN pin reaches approximately 0.8V, top side switching is enabled. However, a top side pulse will not occur until SS/EN has charged up to the level appropriate for the existing output voltage (a pre bias condition). Once the first top side gate pulse actually occurs, the bottom side driver is enabled and the remainder of the startup is fully synchronous.
In the event of an over current during startup, the SC4612H behaves in the same manner as an over current in steady state (see Over Current Protection).

Oscillator Frequency Selection

The internal oscillator sawtooth signal is generated by charging an external capacitor with a current source of 100µA charge current.

See Table 1 "Frequency vs. C_{OSC}" to determine oscillator frequency.

Frequency, vs. C_{OSC}

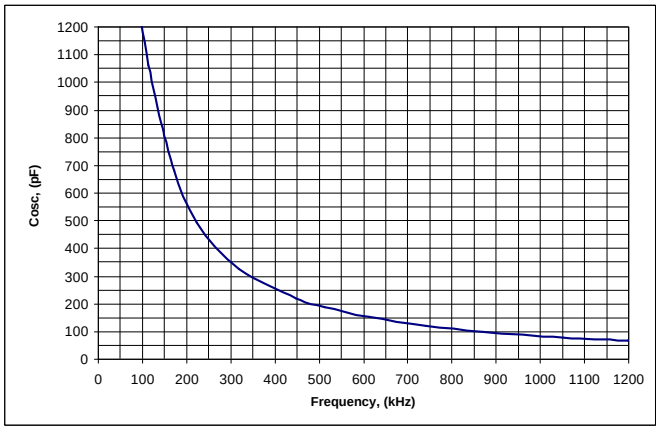


Table 1

Applications Information (Cont.)

Under Voltage Lock Out

Under Voltage Lock Out (UVLO) circuitry senses the VDD through a voltage divider. If this signal falls below 4.5V (typical) with a 400mV hysteresis (typical), the output drivers are disabled. During the thermal shutdown, the output drivers are disabled.

OVERCURRENT PROTECTION

The SC4612H features low side MOSFET $R_{DS(ON)}$ current sensing and hiccup mode over current protection. The voltage across the bottom FET is sampled approximately 150ns after it is turned on to prevent false tripping due to ringing of the phase node.

The internally set over current threshold is 100mV typical. This can be adjusted up or down by connecting a resistor between ILIM and DRV or GND respectively. When programming with an external resistor, threshold set point accuracy will be degraded to 30%. The FET $R_{DS(ON)}$ at temperature will typically be 150% or more of the room temperature value. Allowance should be made for these sources of error when programming a threshold value.

When an over current event occurs, the SC4612H immediately disables both gate drives. The SS ramp continues to its final value, if not already there. Once at final value, the SS capacitor is discharged at approximately 1uA until SS low value is reached (approx 0.8V). The SS/Hiccup cycle will then repeat until the fault condition is removed and the SC4612H starts up normally on the next SS cycle.

Gate Drive/Control

The SC4612H provides integrated high current drivers for fast switching of large MOSFETs. The higher gate current will reduce switching losses of the larger MOSFETs.

The low side gate drive is supplied directly from the DRV. The high side gate drive is bootstraped from the DRV pin.

Cross conduction prevention circuitry ensures a non overlapping (30ns typical) gate drive between the top and bottom MOSFETs. This prevents shoot through losses which provides higher efficiency. Typical total minimum off time for the SC4612H is about 30ns.

ERROR AMPLIFIER DESIGN

The SC4612H is a voltage mode buck controller that utilizes an externally compensated high bandwidth error amplifier to regulate the output voltage. The power stage of the synchronous rectified buck converter control-to-output transfer function is as shown below.

$$G_{VD}(s) = \frac{V_{IN}}{V_S} \times \left(\frac{1 + sESR_C C}{1 + s\frac{L}{R_L} + s^2 LC} \right)$$

where,

V_{IN} – Input voltage

L – Output inductance

ESR_C – Output capacitor ESR

V_S – Peak to peak ramp voltage

R_L – Load resistance

C – Output capacitance

The classical Type III compensation network can be built around the error amplifier as shown below:

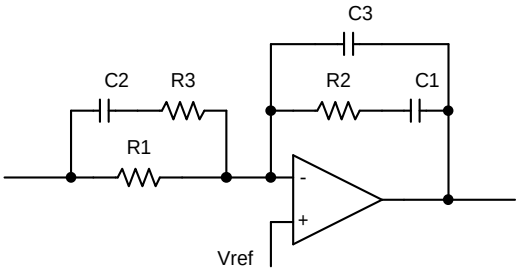


Figure 1. Voltage mode buck converter compensation network. The transfer function of the compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s} \cdot \frac{(1 + \frac{s}{\omega_{Z1}})(1 + \frac{s}{\omega_{Z2}})}{(1 + \frac{s}{\omega_{P1}})(1 + \frac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2 C_1}, \quad \omega_{Z2} = \frac{1}{(R_1 + R_3)C_2}, \quad \omega_o = \frac{1}{\sqrt{Lout \times Cout}}$$

$$\omega_I = \frac{1}{R_1(C_1 + C_3)}, \quad \omega_{P1} = \frac{1}{R_3 C_2}, \quad \omega_{P2} = \frac{1}{R_2 \frac{C_1 C_3}{C_1 + C_3}}$$

Applications Information (Cont.)

The design guidelines are as following:

1. Set the loop gain crossover frequency w_C for given switching frequency.

2. Place an integrator at the origin to increase DC and low frequency gains.

3. Select w_{Z1} and w_{Z2} such that they are placed near w_O to dampen peaking; the loop gain should cross 0dB at a rate of -20dB/dec.

4. Cancel w_{ESR} with compensation pole w_{P1} ($w_{P1} = w_{ESR}$).

5. Place a high frequency compensation pole w_{P2} at half the switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with adequate phase lag at w_C.

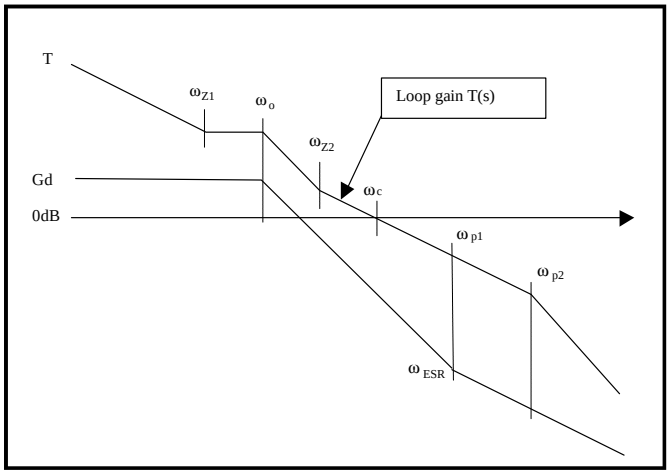


Figure 2. Simplified asymptotic diagram of buck power stage and its compensated loop gain.

Application Information (Cont.)

COMPONENT SELECTION:

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Capacitor		Qty Rqd.	Total	
	C (uF)	ESR (mΩ)		C (uF)	ESR (mΩ)
Ceramic	22	2-10	1	22	2-10
SP Cap	220	7	1	220	7.0
POS-CAP	680	18	2	1360	9.0
Low ESR Aluminum	1500	44	5	7500	8.8

The choice of which to use is simply a cost/performance issue, with low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above.

The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR}\ C}{I_t}\left(V_{IN} - V_O\right)$$

The calculated maximum inductor value assumes 100% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions. We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot D$$

where

$$D = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, If we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot \frac{100ns}{T_{SW}}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{2}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume

Application Information (Cont.)

that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

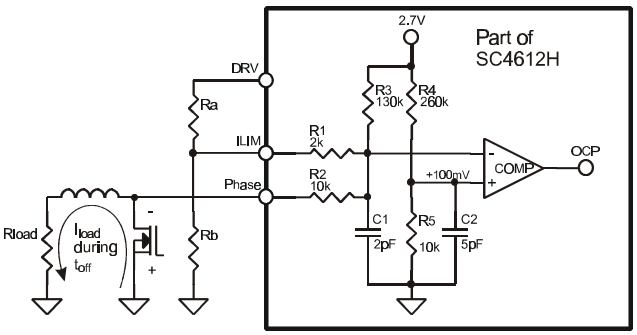
$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it resulting in very low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1-D)$$

INPUT CAPACITORS - Since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

Low Side R_{DS_ON} Current Limit



1. Programming resistors Ra and Rb - Not installed:

$$\frac{2.75V - 100mV}{R3} = \frac{100mV - Vphase}{R2}$$

solving for: V_{PHASE} = -100mV, therefore the circuit will trip @ R_{DS_ON} x I_{LOAD} = 100mV

2. To increase trip voltage - install Ra.

$$Ra = \frac{-772 - 20 \cdot V_{PHASE}}{1 + 10 \cdot V_{PHASE}}$$

solving for double the current limit: V_{PHASE} = -200mV.

Ra = 768kΩ.

3. To decrease trip voltage - install Rb

$$Rb = \frac{8 - 20 \cdot V_{PHASE}}{1 + 10 \cdot V_{PHASE}}$$

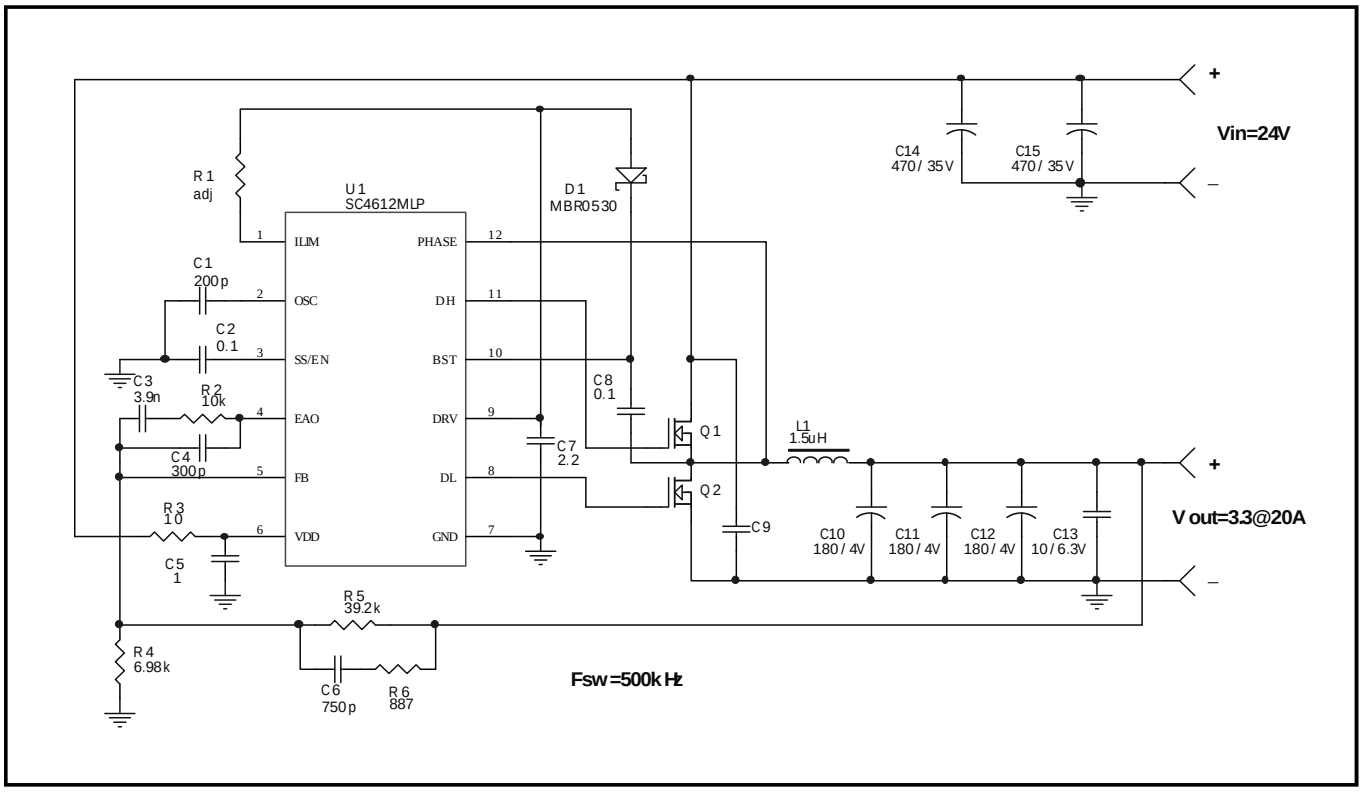
solving for half the current limit: V_{PHASE} = -50mV.

Rb = 18kΩ.

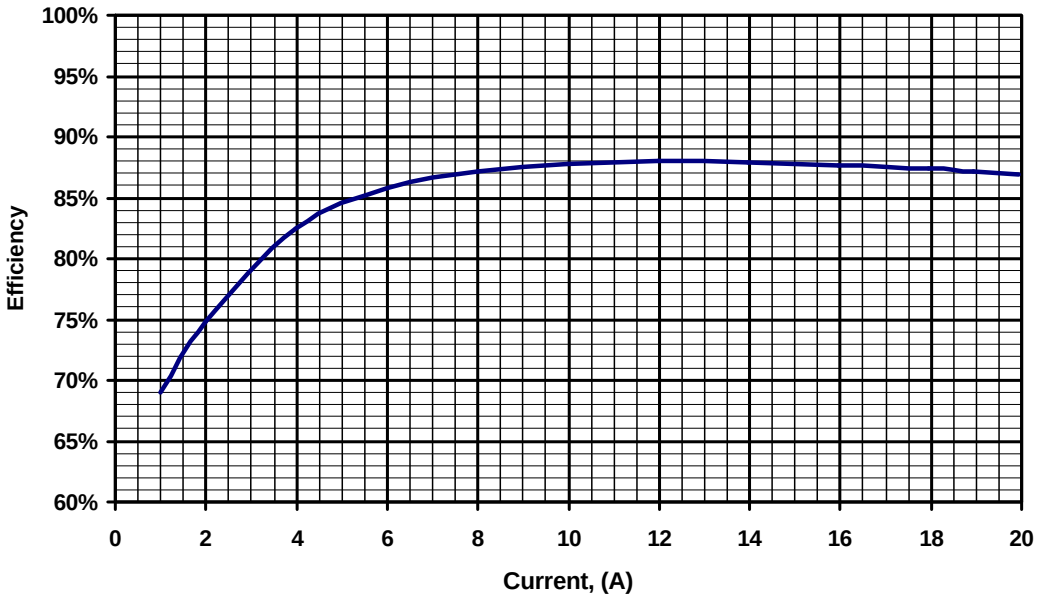
NOTE! Allow for tempco and R_{DS_ON} variation of the MOS-FET - see "overcurrent protection" information on page 11 in the datasheet.

Application Information (Cont.)

Application Circuit 1: Vin = 24V; Vout = 3.3V @ 20A, Fsw = 500kHz.

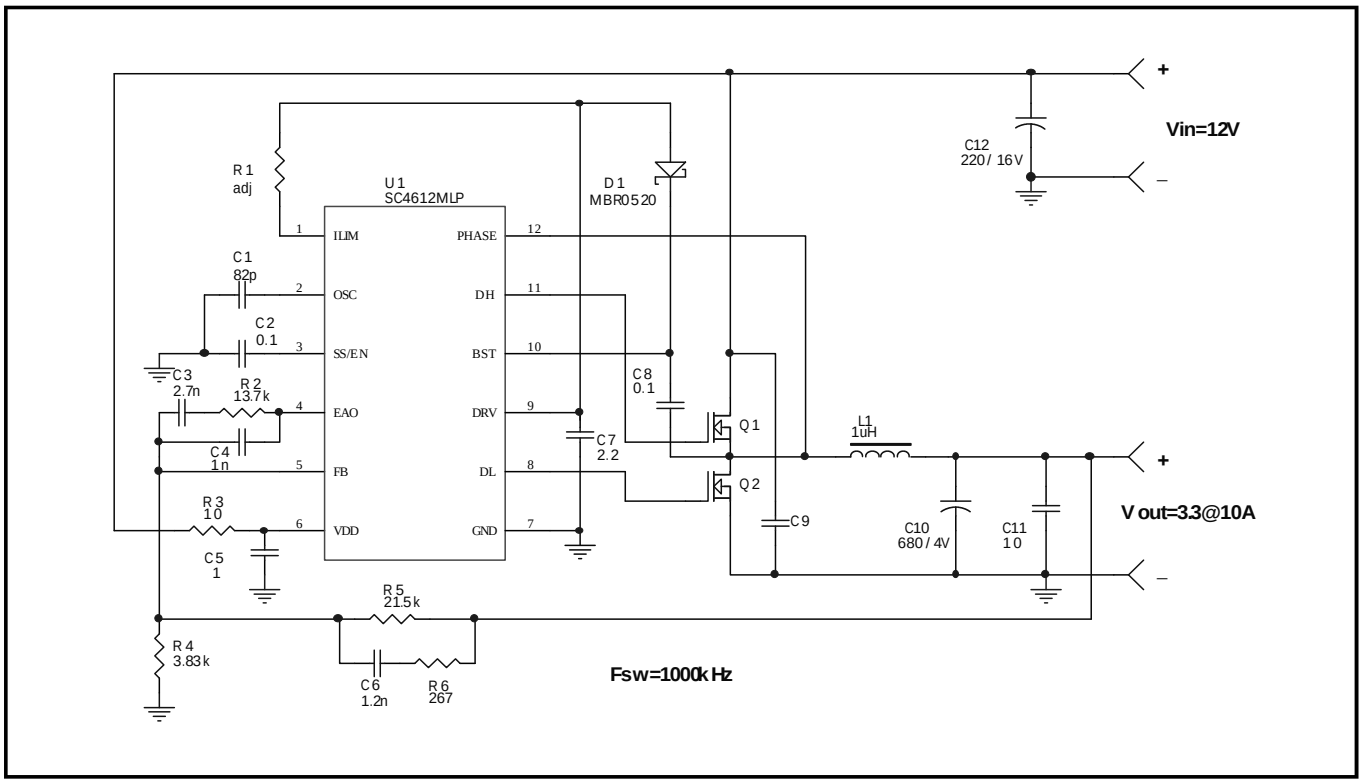


Vin=24V, Vout_nom=3.3V, Fsw=500kHz

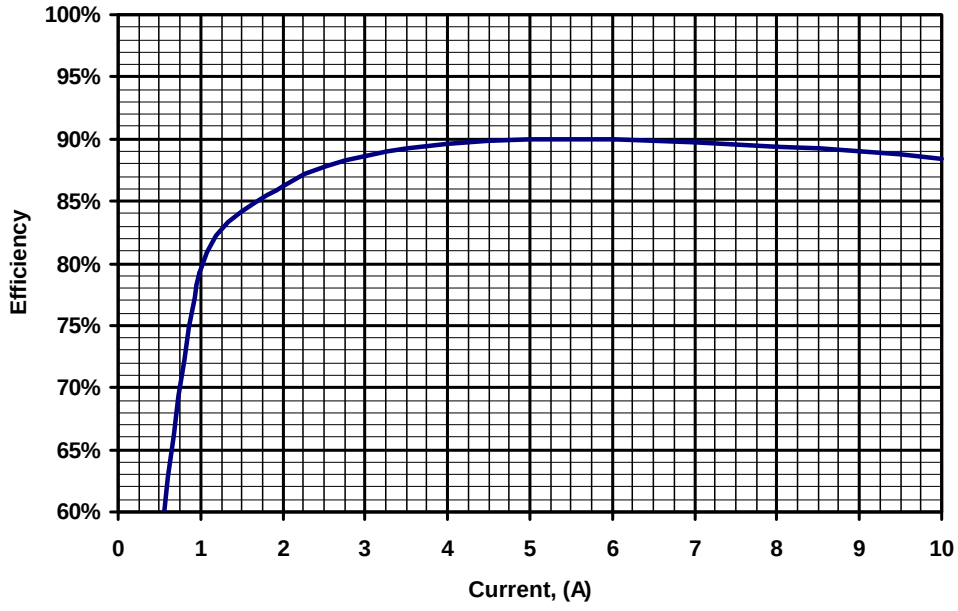


Application Information (Cont.)

Application Circuit 2: Vin = 12V; Vout = 3.3V @ 10A, Fsw = 1MHz

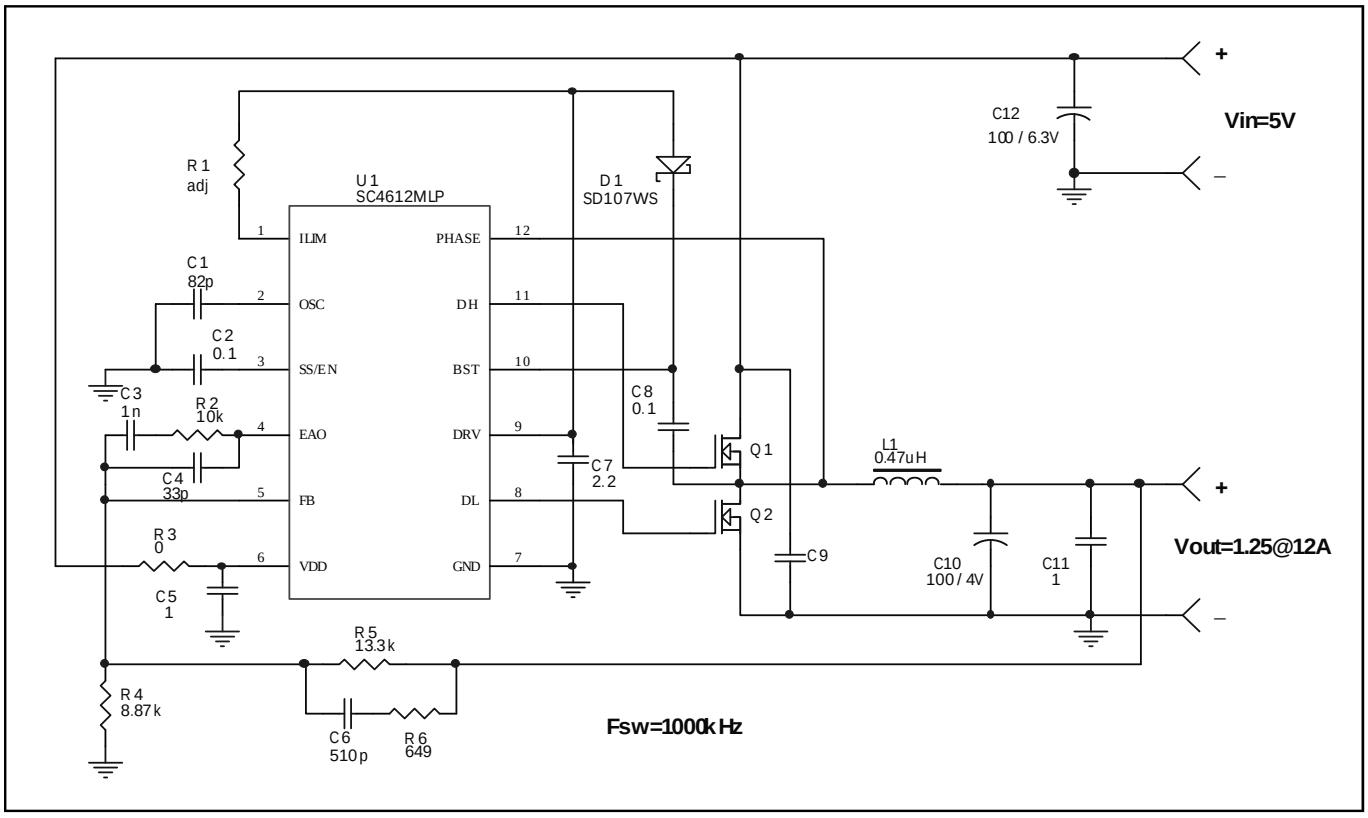


Vin=12V, Vout_nom=3.3V, Fsw=1MHz

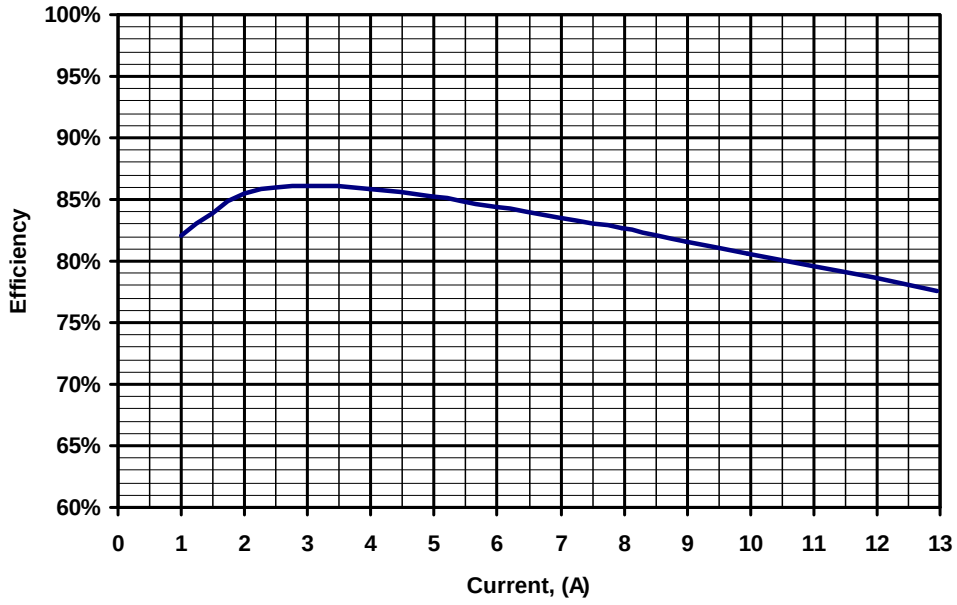


Application Information (Cont.)

Application Circuit 3: Vin = 5V; Vout = 1.25V @ 12A, Fsw = 1MHz.

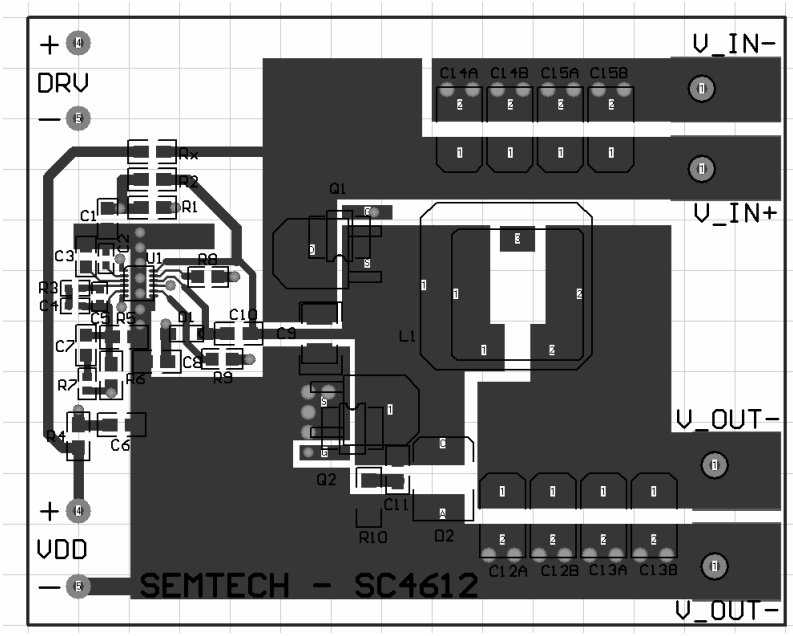


Vin=5V, Vout_nom=1.25V, Fsw=1MHz

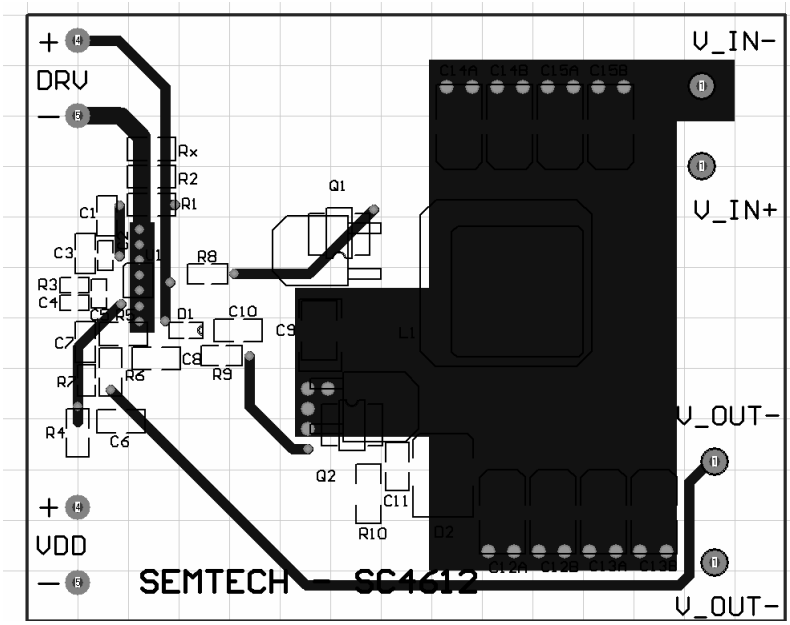


Evaluation Board:

Top layer and components view



Bottom Layer:



PCB Layout Guidelines

Careful attention to layout is necessary for successful implementation of the SC4612H PWM controller. High switching currents are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1) The high power section of the circuit should be laid out first. A ground plane should be used. The number and position of ground plane interruptions should not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas; for example, the input capacitor and bottom FET ground.

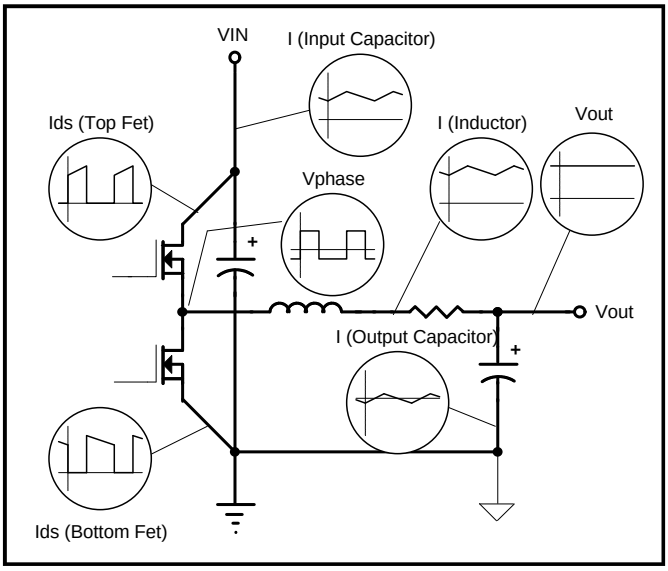
2) The loop formed by the Input Capacitor(s) (Cin), the Top FET (M1), and the Bottom FET (M2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3) The connection between the junction of M1, M2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. Top FET gate charge currents flow in this trace.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only, and therefore, connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

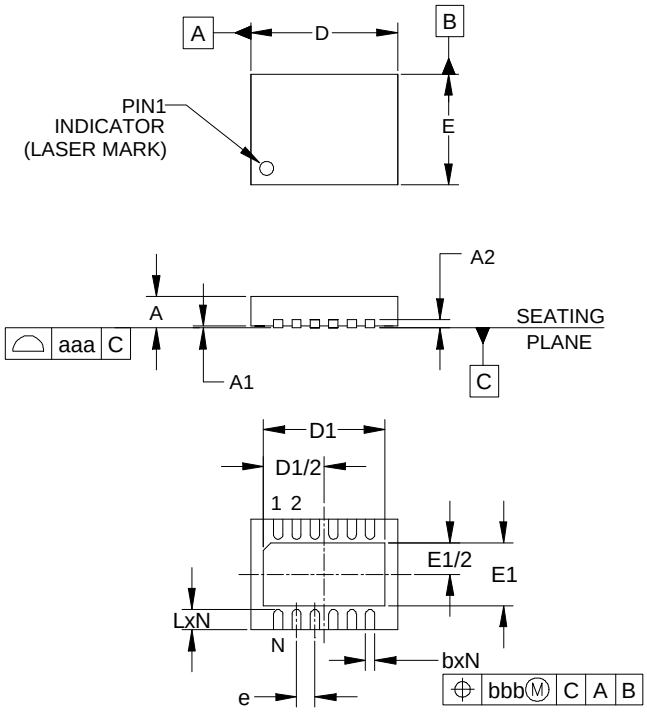
5) The SC4612H is best placed over a quiet ground plane area. Avoid pulse currents in the Cin, M1, M2 loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, M1, M2 loop. Under no circumstances should GND be returned to a ground inside the Cin, M1, M2 loop.

6) Allow adequate heat sinking area for the power components. If multiple layers will be used, provide sufficent vias for heat transfer.



Voltage and current waveforms of buck power stage .

Outline Drawing - MLPD - 12

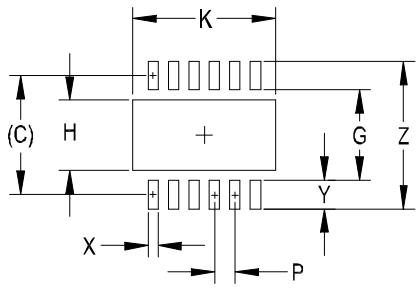


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	.035	.040	0.80	0.90	1.00
A1	.000	.001	.002	0.00	0.02	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.154	.157	.161	3.90	4.00	4.10
D1	.124	.130	.134	3.15	3.30	3.40
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	12			12		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPD - 12

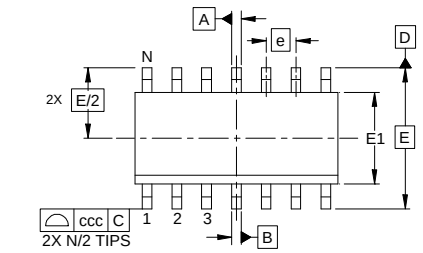


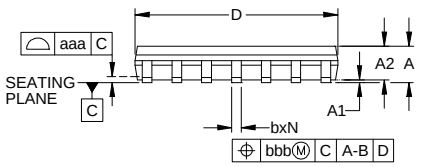
DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.087	2.20
H	.067	1.70
K	.138	3.50
P	.020	0.50
X	.012	0.30
Y	.028	0.70
Z	.142	3.60

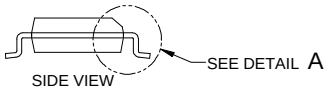
NOTES:

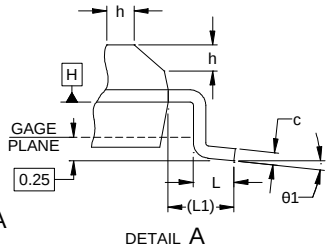
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Outline Drawing - SOIC - 14







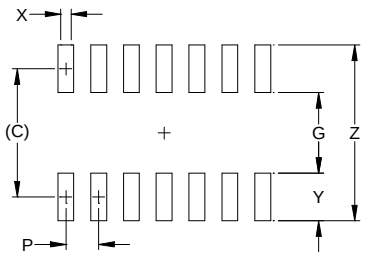


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.337	.341	.344	8.55	8.65	8.75
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	14			14		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AB.

Land Pattern - SOIC - 14



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 302A.

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