# 71M6511/71M6511H
## Single-Phase Energy Meter IC
## DATA SHEET

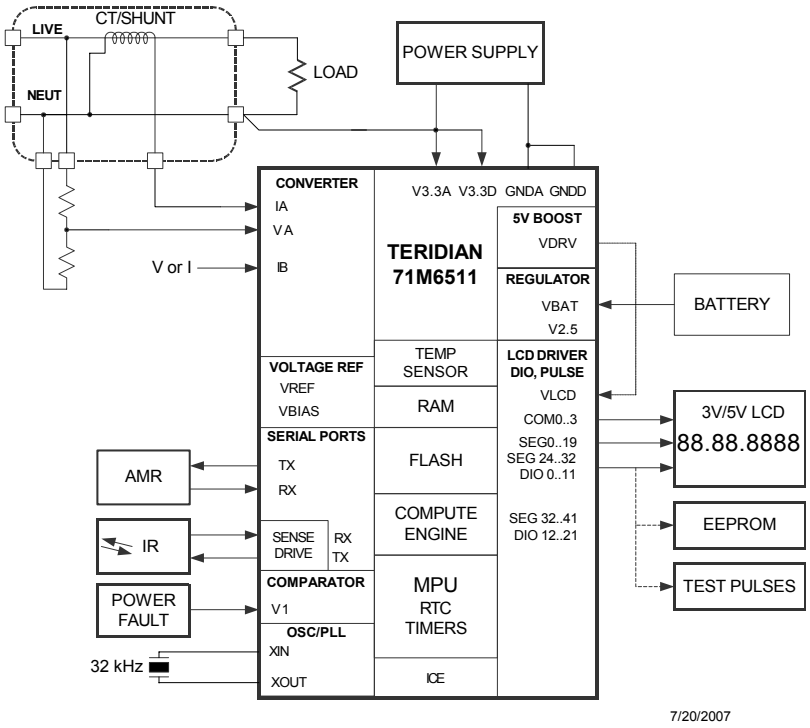
AUGUST 2007

## GENERAL DESCRIPTION

The TERIDIAN 71M6511 is a highly integrated SOC with an MPU core, RTC, FLASH and LCD driver. TERIDIAN's patented Single Converter Technology™ with a 22-bit delta-sigma ADC, 3 analog inputs, digital temperature compensation, precision voltage reference and 32-bit computation engine (CE) supports a wide range of single-phase metering applications with very few low cost external components. A 32kHz crystal time base for the entire system and internal battery backup support for RAM and RTC further reduce system cost.

Maximum design flexibility is supported with multiple UARTs, $I^2C$, a power fail comparator, a 5V LCD charge pump, up to 12 DIO pins and an in-system programmable FLASH. The device is offered in high (0.1%) and standard (0.5%) accuracy versions for multifunction residential/commercial meter applications requiring multiple voltage/current inputs and complex LCD or DIO configurations.

A complete array of ICE and development tools, programming libraries and reference designs enable rapid development and certification of meters that meet most demanding worldwide electricity metering standards.




### FEATURES

- Wh accuracy over temperature and 2000:1 range
  < 0.1% -- 71M6511H,
  <0.5% -- 71M6511
- Exceeds IEC62053 / ANSIC12.20.
- Voltage reference
  < 10ppm/°C -- 71M6511H,
  < 50ppm/°C -- 71M6511
- Three sensor inputs - VDD referenced
- Low jitter Wh/VARh pulse outputs
- Pulse count for pulse outputs
- Four-quadrant metering
- Voltage/current angle
- Line frequency count for RTC
- Digital temperature compensation
- Sag detection
- Independent 32-bit compute engine
- 40-70Hz line frequency range with same calibration
- Phase compensation (±7°)
- Battery Backup for RAM and RTC
- 22mW @3.3V, 7.2µW back up
- Flash memory option with security
- 22-bit delta-sigma ADC
- 8-bit MPU (80515) - 1 clock cycle per instruction
- LCD driver (≤128 pixels)
- High speed SSI serial output
- RTC for time-of-use functions
- Hardware watchdog timer
- Up to 12 general purpose I/O pins
- 64KB Flash, 7KB RAM
- Two UARTs for IR and AMR
- 64-lead LQFP package

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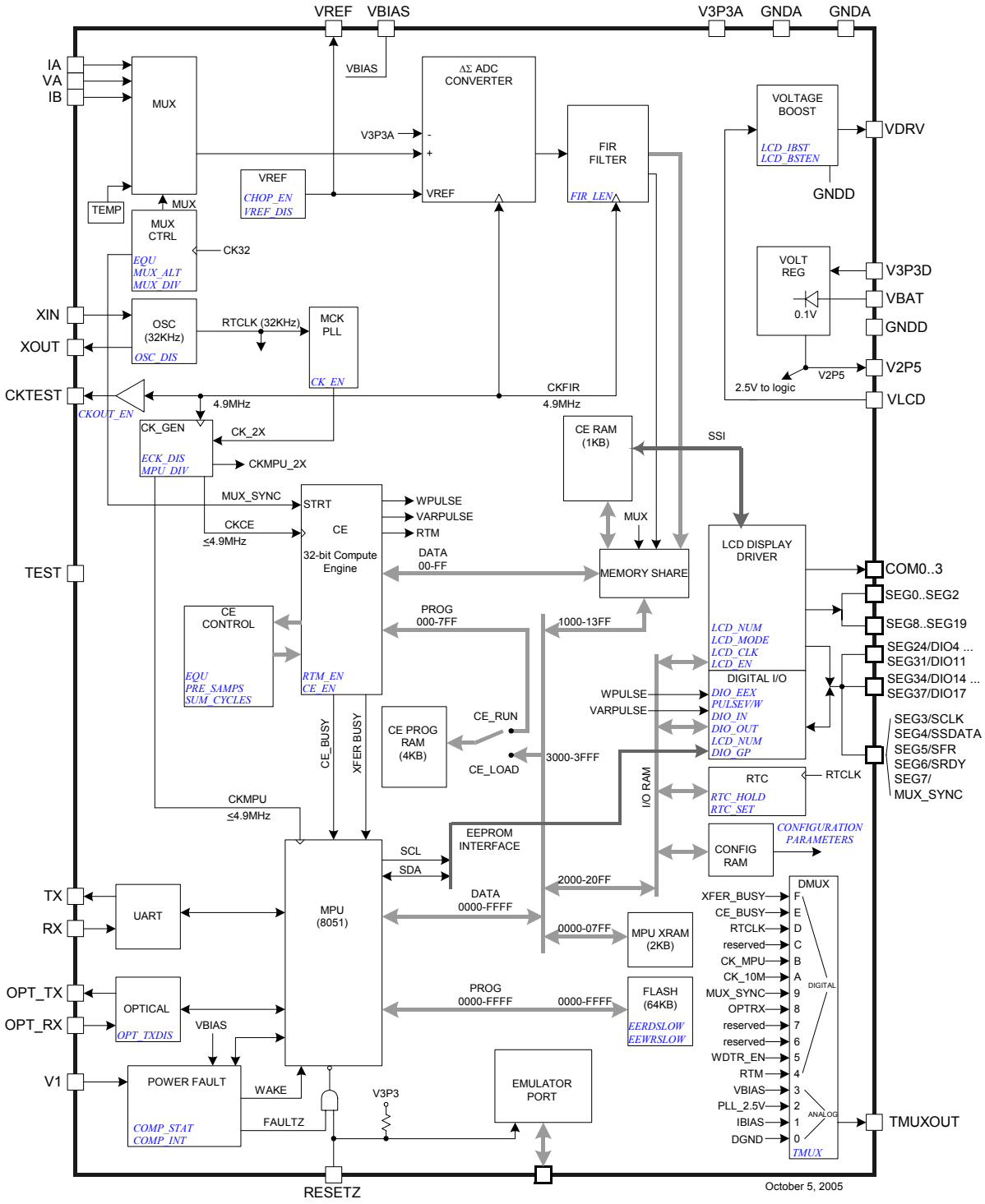



**Figure 1: IC Functional Block Diagram**

# HARDWARE DESCRIPTION

## Hardware Overview

The TERIDIAN 71M6511 single chip single-phase meter integrates all primary functional blocks required to implement a solid-state electricity meter. Included on chip are an analog front end (AFE), an 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515), an independent 32-bit digital computation engine (CE), a voltage reference, a temperature sensor, LCD drivers, RAM, FLASH memory, a real time clock (RTC), and a variety of I/O pins. Various current sensor technologies are supported including Current Transformers (CT), Resistive Shunts, and Rogowski (*di/dt)* Coils.

In addition to advanced measurement functions, the real time clock function allows the 71M6511/6511H to record time of use (TOU) metering information for multi-rate applications. Measurements can be displayed on either a 3V or a 5V LCD. Flexible mapping of LCD display segments will facilitate integration with any LCD format. The design trade-off between the number of LCD segments and DIO pins can be flexibly configured using memory-mapped I/O to accommodate various requirements.

The 71M6511 includes several I/O peripheral functions that improve the functionality of the device and reduce the component count for most meter applications. The I/O peripherals include two UARTs, digital I/O, comparator inputs, LCD display drivers, $I^2C$ interface and an optical/IR interface.

One of the two internal UARTs (UART1) is adapted to support an Infrared LED with internal drive output and sense input but it can also function as a standard UART.

A block diagram of the chip is shown in Figure 1. A detailed description of various hardware blocks follows.

## Analog Front End (AFE)

The AFE of the TERIDIAN 71M6511 Power Meter IC is comprised of an input multiplexer, a delta-sigma A/D converter with a voltage reference, followed by an FIR filter. A block diagram of the AFE is shown in Figure 3.

### Multiplexer

The input multiplexer supports four input signals that are applied to the pins IA, VA, and IB plus the output of the internal temperature sensor. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the pins IA, VA, and IB, are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) is selected, along with the other signal sources shown in Table 1.

Alternate multiplexer cycles are usually performed infrequently (every second or so). VA is not replaced in the alternate multiplexer cycles. Missing samples due to alternate multiplexer cycles are automatically interpolated by the CE.

| ***EQU*** | **Channels used from MUX Sequence** States 0 → 3 | | | | **Channels used from alternative MUX Sequence** States 0 → 3 | | | |
|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 000 | IA | VA | IB | - | TEMP | VA | - | - |
| 001 | IA | VA | IB | - | TEMP | VA | IB | - |

**Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles**

In a typical application, the IA input is connected to a current transformer that senses the line current. VA is typically connected to a voltage sensor through resistor dividers. IB may be connected to a second current transformer, e.g. for optional tamper detection.

The Multiplexer Control Circuit handles the setting of the multiplexer. The function of the Multiplexer Control Circuit is governed by the I/O RAM registers *MUX_ALT* (0x2005[2]), *EQU* (0x2000[7:5]), and *MUX_DIV* (0x2002[7:6]). *MUX_DIV* controls the number of samples per cycle. It can request 2, 3, 4, or 6 multiplexer states per cycle.

The *MUX_ALT* bit requests an alternate multiplexer cycle. The bit may be asserted on any MPU cycle and may be subsequently de-asserted on any cycle including the next one. A rising edge on *MUX_ALT* will cause the Control Circuit to wait until the next multiplexer cycle and implement a single alternate cycle.

Multiplexer Control Circuit also controls the FIR filter initiation and the chopping of the ADC reference voltage, VREF. The Multiplexer Control Circuit is clocked by CK32, the 32768Hz clock from the PLL block, and launches each pass through the CE program.

Table 2 shows the possible settings for *MUX_DIV* and *FIR_LEN* and the resulting channels sampled along with sample frequencies.

| ***MUX_DIV* (0x2002[7.6])** | **Number of channels selected (mux states per cycle)** | **Number of CK32 states for code pass** | **Effective sample frequency [Hz]** | **Number of CK32 states for code pass** | **Effective sample frequency [Hz]** |
|---|---|---|---|---|---|
| | | ***FIR_LEN* = 0** | | ***FIR_LEN* =1** | |
| 00 | --- | Not Allowed | | | |
| **01** | **4** | 9 | 3640.89 | **13** | **2520.615** |
| 10 | 3 | 7 | 4681.143 | 10 | 3276.8 |
| 11 | 2 | 5 | 6553.6 | 7 | 4681.143 |

**Table 2: Channel control based on *MUX_DIV* and *FIR_LEN***

## ADC

A single 21/22-bit delta-sigma A/D converter (ADC) digitizes the power inputs to the AFE. The resolution of the ADC is programmable using the I/O RAM register *FIR_LEN* register (0x2005[4]). ADC resolution may be selected to be 21 bits (*FIR_LEN*=0), or 22 bits (*FIR_LEN*=1). Conversion time is two cycles of CK32 with *FIR_LEN* = 0 and three cycles with *FIR_LEN* = 1.

**In order to provide the maximum resolution, the ADC should be operated with *FIR_LEN* = 1. Accuracy, timing and functional specifications in this data sheet are based on *FIR_LEN* = 1 and *MUX_DIV* = 1 (four CK32 cycles). Alternative specifications are also provided for *FIR_LEN* = 1 and *MUX_DIV* = 2 (three CK32 cycles) in the CE Program and Environment section.**

Initiation of each ADC conversion is controlled by the Multiplexer Control Circuit as described previously.

## FIR Filter

The finite impulse response (FIR) filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data of the FIR filter (raw data) is stored into the CE DRAM location determined by the multiplexer selection. The location of the raw data in the CE DRAM is specified in the CE Program and Environment Section.

## Voltage Reference

The 71M6511/6511H includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference of the 71M6511H is trimmed in production to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

The voltage reference is chopper stabilized, i.e. the polarity can be switched by the MPU using the I/O RAM register *CHOP_ENA* (0x2002[5:4]). The two bits in the *CHOP_ENA* register enable the MPU to operate the chopper circuit in regular or inverted operation, or in "toggling" mode. When the chopper circuit is toggled in between multiplexer cycles, DC offsets on the measured signals will automatically be averaged out.

The general topology of a chopped amplifier is given in Figure 2.

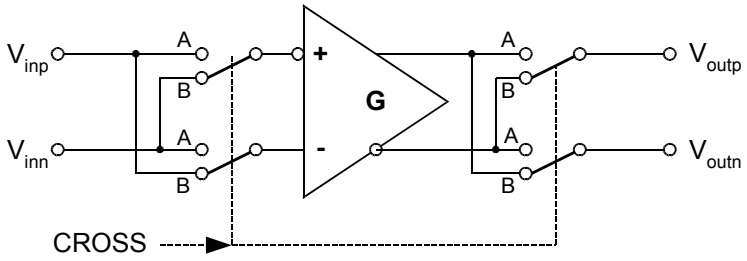



**Figure 2: General Topology of a Chopped Amplifier**

It is assumed that an offset voltage Voff appears at the positive amplifier input. With all switches, as controlled by CROSS in the "A" position, the output voltage is:

Voutp – Voutn = G (Vinp + Voff – Vinn) = G (Vinp – Vinn) + G Voff

With all switches set to the "B" position by applying the inverted CROSS signal, the output voltage is:

Voutn – Voutp = G (Vinn – Vinp + Voff) = G (Vinn – Vinp) + G Voff, or

Voutp – Voutn = G (Vinp – Vinn) - G Voff

Thus, when CROSS is toggled, e.g. after each multiplexer cycle, the offset will alternately appear on the output as positive and negative, which results in the offset effectively being eliminated, regardless of its polarity or magnitude.

The Functional Description Section contains a chapter with a detailed description on controlling the *CHOP_ENA* register.

### Temperature Sensor

The 71M6511/6511H includes an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature The MPU may request an alternate multiplexer cycle containing the temperature sensor output by asserting *MUX_ALT*.

The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see section titled "Temperature Compensation").

The zero reference for the temperature sensor is VBIAS.

### Functional Description

The AFE functions as a data acquisition system, controlled by the MPU. The main signals (IA, VA, IB) are sampled and the ADC counts obtained are stored in CE RAM where they can be accessed by the CE and, if necessary, by the MPU. Alternate multiplexer cycles are initiated less frequently by the MPU to gather access to the slow temperature signal.

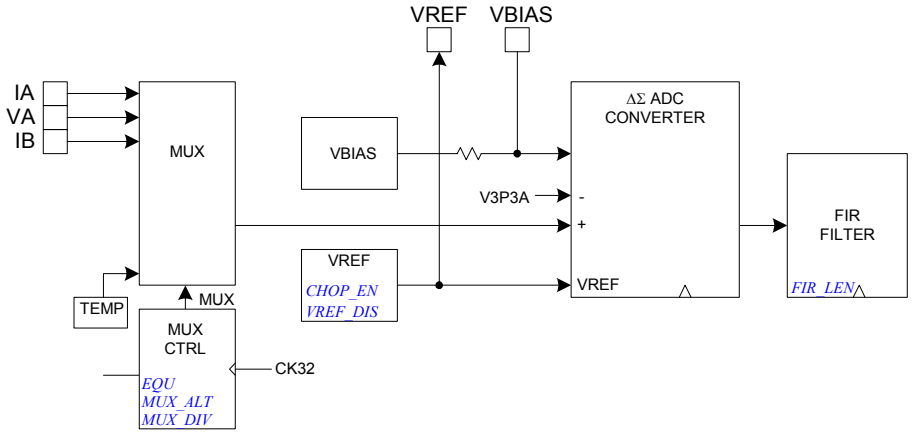



**Figure 3: AFE Block Diagram**

## Computation Engine (CE)

The CE, a dedicated 32-bit RISC processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all six channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on chip temperature (temperature compensation) and calibration coefficients.

The CE program RAM (CE PRAM) is loaded at boot time by the MPU and then executed by the CE. Each CE instruction word is 2 bytes long. The CE program counter begins a pass through the CE code each time multiplexer state 0 begins. The code pass ends when a HALT instruction is executed. For proper operation, the code pass must be completed before the multiplexer cycle ends (see System Timing Summary in the Functional Description Section).

The CE data RAM (CE DRAM) can be accessed by the FIR filter block, the RTM circuit, the CE, and the MPU. Assigned time slots are reserved for FIR, RTM, and MPU, respectively, such that memory accesses to CE_RAM do not collide. Holding registers are used to convert 8-bit wide MPU data to/from 32-bit wide CE DRAM data, and wait states are inserted as needed, depending on the frequency of CKMPU.

Table 3 shows the CE DRAM addresses allocated to analog inputs from the AFE.

| Address (hex) | Name | Description |
|---|---|---|
| 0x00 | IA | Phase A current |
| 0x01 | VA | Phase A voltage |
| 0x02 | IB | Phase B current |
| 0x03 | - | Reserved |
| 0x04 | - | Reserved |
| 0x05 | - | Reserved |
| 0x06 | TEMP | Temperature |
| 0x07 | -- | Reserved |

**Table 3: CE DRAM Locations for ADC Results**

## Meter Equations

The Compute Engine (CE) program for residential meter configurations implements the equations in Table 4. The I/O RAM register *EQU* specifies the equation to be used based on the number and arrangement of phases used for metering. In case of single-phase metering, the unconnected input should be tied to V3P3A, the analog supply voltage. The *EQU* selection enables the 71M6511 to calculate single-phase power measurement based on the type of service used. Table 4 also states the sequence of the multiplexer in the AFE.

| ***EQU*** | **Formula** | **Channels used from MUX Sequence** States 0 → 3 | | | | **Channels used from alternative MUX Sequence** States 0 → 3 | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 0 | 1 | 2 | 3 |
| 000 | **VA IA (1 element, 2W 1ϕ)** | IA | VA | IB | - | TEMP | VA | - | - |
| 001 | **VA(IA-IB)/2 (1 element, 3W 1ϕ)** | IA | VA | IB | - | TEMP | VA | IB | - |

**Table 4: Standard Meter Equations (inputs shown gray are scanned but not used for calculation)**

## Pulse Generator

The CE contains two pulse generators which create low jitter pulses at a rate set by the CE DRAM registers *APULSEW*WRATE* and *APULSER*WRATE* if *EXT_PULSE* (a CE input variable in CE DRAM) is 15. This mode puts the MPU in control of pulse generation by placing values into the *APULSEW* and *APULSER* registers ("external pulse generation").

If *EXT_PULSE* is 0, *APULSEW* is replaced with *WSUM_X* and *APULSER* is replaced with *VARSUM_X*. In this mode, the CE generates pulse based on its internal computation of *WSUM_X* and *VARSUM_X*, the signed sums of energy from all three elements ("internal pulse generation").

The *DIO_PV* and *DIO_PW* bits as described in the Digital I/O section can be programmed to route WPULSE and VARPULSE to the output pins DIO6 and DIO7 respectively. DIO6 and DIO7 can be configured to generate interrupts (useful for pulse counting by the MPU – see On-Chip Resources (DIO Section).

### Real-Time Monitor

The CE contains a Real Time Monitor (RTM), which can be programmed to monitor four selectable CE RAM locations at full sample rate. The four monitored locations are serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass (see the Test Ports Section for details)

### CE Functional Overview

The ADC processes one sample per channel per multiplexer cycle. Figure 4 shows the timing of the samples taken during one multiplexer cycle.

The number of samples processed during one accumulation cycle is controlled by the I/O RAM registers *PRE_SAMPS* (0x2001[7:6]) and *SUM_CYCLES* (0x2001[5:0]). The integration time for each energy output is

*PRE_SAMPS* * *SUM_CYCLES* / 2520.6, where 2520.6 is the sample rate [Hz] (for *MUX_DIV* = 1)

For example, *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50 will establish 2100 samples per accumulation cycle. *PRE_SAMPS* = 100 and *SUM_CYCLES* = 21 will result in the exact same accumulation cycle of 2100 samples or 833ms. After an accumulation cycle is completed, the XFER_BUSY interrupt signals to the MPU that accumulated data are available.

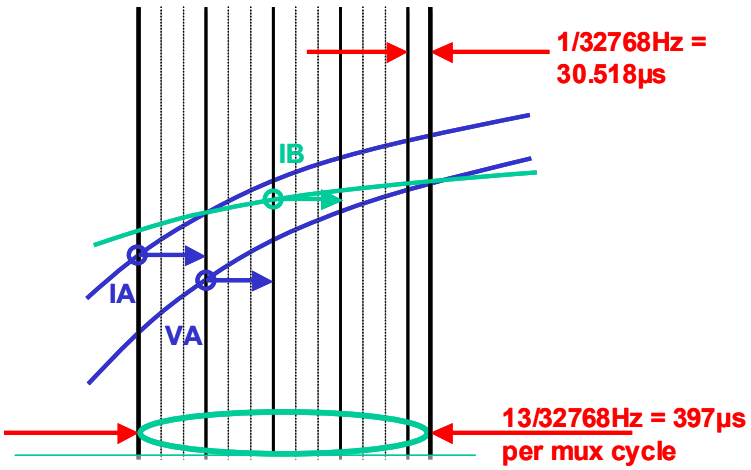



**Figure 4: Samples in Multiplexer Cycle**

The end of each multiplexer cycle is signaled to the MPU by the CE_BUSY interrupt. At the end of each multiplexer cycle, status information, such as sag data and the digitized input signal, is available to the MPU.

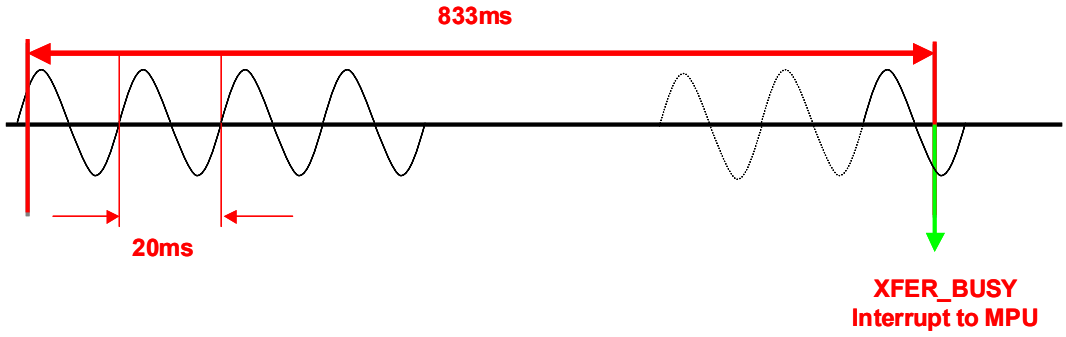



**Figure 5: Accumulation Interval**

Figure 5 shows the accumulation interval resulting from *MUX_DIV* = 1, *PRE_SAMPS* = 42 and *SUM_CYCLES* = 50, consisting of 2100 samples of 397µs each, followed by the XFER_BUSY interrupt. The sampling in this example is applied to a 50Hz signal.

There is no correlation between the line signal frequency and the choice of *PRE_SAMPS* or *SUM_CYCLES (*even though when *SUM_CYCLES* = 42 one set of *SUM_CYCLES* happens to sample a period of 16.6ms). Furthermore, sampling does not have to start when the line voltage crosses the zero line.

## 80515 MPU Core

### 80515 Overview

The 71M6511/6511H includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 5MHz clock results in a processing throughput of 5 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single cycle. This leads to an 8x performance (in average) improvement (in terms of MIPS) over the Intel 8051 device running at the same clock frequency.

Actual processor clocking speed can be adjusted to the total processing demand of the application (metering calculations, AMR management, memory management, LCD driver management and I/O management) using the I/O RAM register *MPU_DIV[2:0]*.

Typical measurement and metering functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of TERIDIAN's standard library. A standard ANSI "C" 80515-application programming interface library is available to help reduce design cycle.

### Memory Organization

The 80515 MPU core incorporates the Harvard architecture with separate code and data spaces.

Memory organization in the 80515 is similar to that of the industry standard 8051. There are three memory areas: Program memory (Flash), external data memory (XRAM), physically consisting of XRAM, CE DRAM, CE PRAM and I/O RAM, and internal data memory (Internal RAM). Figure 6 shows the memory map (see also Table 55).

**Internal and External Data Memory:** Both internal and external data memory are physically located on the 71M6511 IC. External data memory is only external to the 80515 MPU core.

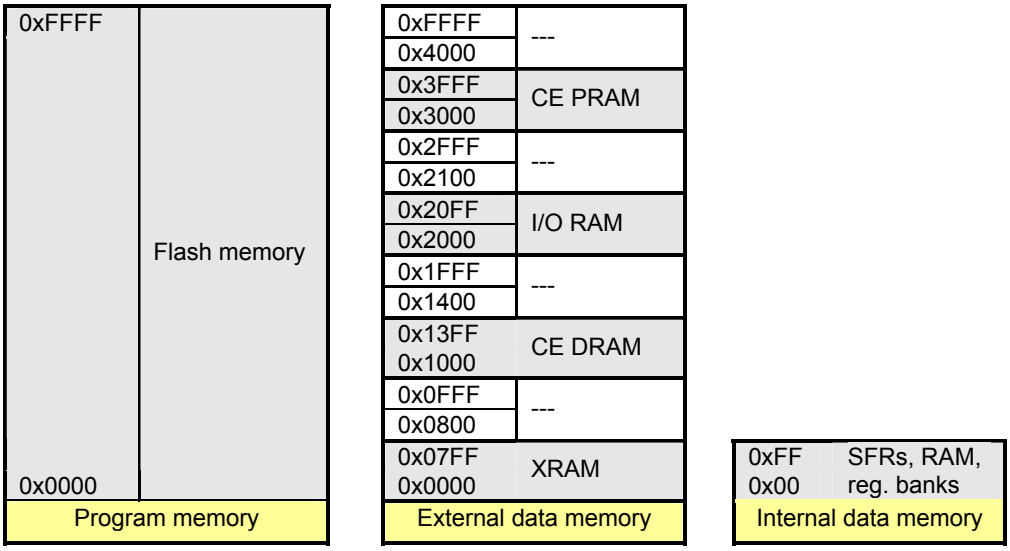



**Figure 6: Memory Map**

**Program Memory:** The 80515 can address up to 64KB of program memory space from 0x0000 to 0xFFFF. Program memory is read when the MPU fetches instructions or performs a MOVC operation.

After reset, the MPU starts program execution from location 0x0000. The lower part of the program memory includes reset and interrupt vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0x0003.

**External Data Memory:** While the 80515 can address up to 64KB of external data memory in the space from 0x0000 to 0xFFFF, only the memory ranges shown in Figure 6 contain physical memory. The 80515 writes into external data memory when the MPU executes a MOVX @Ri,A or MOVX @DPTR,A instruction. The MPU reads external data memory by executing a MOVX A,@Ri or MOVX A,@DPTR instruction (SFR USR2 provides the upper 8 bytes for the MOVX A,@Ri instruction).

**Clock Stretching:** MOVX instructions can access fast or slow external RAM and external peripherals. The three low ordered bits of the CKCON register define the stretch memory cycles. Setting all the *CKCON* stretch bits to one allows access to very slow external RAM or external peripherals.

Table 5 shows how the signals of the External Memory Interface change when stretch values are set from 0 to 7. The widths of the signals are counted in MPU clock cycles. The post-reset state of the CKCON register, which is in bold in the table, performs the MOVX instructions with a stretch value equal to 1.

| CKCON register | | | Stretch Value | Read signals width | | Write signal width | |
|---|---|---|---|---|---|---|---|
| CKCON.2 | CKCON.1 | CKCON.0 | | memaddr | memrd | memaddr | memwr |
| 0 | 0 | 0 | 0 | 1 | 1 | 2 | 1 |
| **0** | **0** | **1** | **1** | **2** | **2** | **3** | **1** |
| 0 | 1 | 0 | 2 | 3 | 3 | 4 | 2 |
| 0 | 1 | 1 | 3 | 4 | 4 | 5 | 3 |
| 1 | 0 | 0 | 4 | 5 | 5 | 6 | 4 |
| 1 | 0 | 1 | 5 | 6 | 6 | 7 | 5 |
| 1 | 1 | 0 | 6 | 7 | 7 | 8 | 6 |
| 1 | 1 | 1 | 7 | 8 | 8 | 9 | 7 |

**Table 5: Stretch Memory Cycle Width**

There are two types of instructions, differing in whether they provide an eight-bit or sixteen-bit indirect address to the external data RAM.

In the first type (MOVX A,@Ri), the contents of R0 or R1, in the current register bank, provide the eight lower-ordered bits of address. The eight high-ordered bits of address are specified with the USR2 SFR. This method allows the user paged access (256 pages of 256 bytes each) to the full 64KB of external data RAM. In the second type of MOVX instruction (MOVX A,@DPTR), the data pointer generates a sixteen-bit address. This form is faster and more efficient when accessing very large data arrays (up to 64 Kbytes), since no additional instructions are needed to set up the eight high ordered bits of address.

It is possible to mix the two MOVX types. This provides the user with four separate data pointers, two with direct access and two with paged access to the entire 64KB of external memory range.

**Dual Data Pointer:** The Dual Data Pointer accelerates the block moves of data. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the 80515 core, the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located at the LSB of the DPS register (DPS.0). DPTR is selected when DPS.0 = 0 and DPTR1 is selected when DPS.0 = 1.

The user switches between pointers by toggling the LSB of the DPS register. All DPTR-related instructions use the currently selected DPTR for any activity.

**The second data pointer may not be supported by certain compilers.**

**Internal Data Memory:** The Internal data memory provides 256 bytes (0x00 to 0xFF) of data memory. The internal data memory address is always 1 byte wide and can be accessed by either direct or indirect addressing. The Special Function Registers occupy the upper 128 bytes**. This SFR area is available only by direct addressing. Indirect addressing accesses the upper 128 bytes of Internal RAM.**

The lower 128 bytes contain working registers and bit-addressable memory. The lower 32 bytes form four banks of eight registers (R0-R7). Two bits on the program memory status word (PSW) select which bank is in use. The next 16 bytes form a block of bit-addressable memory space at bit addressees 0x00-0x7F. All of the bytes in the lower 128 bytes are accessible through direct or indirect addressing. Table 6 shows the internal data memory map.

| Address | Direct addressing | Indirect addressing |
|---|---|---|
| 0xFF | Special Function Registers (SFRs) | RAM |
| 0x80 | | |
| 0x7F | Byte-addressable area | |
| 0x30 | | |
| 0x2F | Bit-addressable area | |
| 0x20 | | |
| 0x1F | Register banks R0…R7 | |
| 0x00 | | |

**Table 6: Internal Data Memory Map**

## Special Function Registers (SFRs)

A map of the Special Function Registers is shown in Table 7.

| Hex\Bin | Bit-address-able | Byte-addressable | | | | | | | Bin/Hex |
|---|---|---|---|---|---|---|---|---|---|
| | X000 | X001 | X010 | X011 | X100 | X101 | X110 | X111 | |
| **F8** | ***INTBITS*** | | | | | | | | **FF** |
| **F0** | *B* | | | | | | | | **F7** |
| **E8** | ***WDI*** | | | | | | | | **EF** |
| **E0** | *A* | | | | | | | | **E7** |
| **D8** | *WDCON* | | | | | | | | **DF** |
| **D0** | *PSW* | | | | | | | | **D7** |
| **C8** | | | | | | | | | **CF** |
| **C0** | *IRCON* | | | | | | | | **C7** |
| **B8** | IEN1 | *IP1* | *S0RELH* | *S1RELH* | | | | *USR2* | **BF** |
| **B0** | | | ***FLSHCTL*** | | | | | ***PGADR*** | **B7** |
| **A8** | *IEN0* | *IP0* | *S0RELL* | | | | | | **AF** |
| **A0** | ***P2*** | ***DIR2*** | ***DIR0*** | | | | | | **A7** |
| **98** | *S0CON* | *S0BUF* | IEN2 | *S1CON* | *S1BUF* | *S1RELL* | ***EEDATA*** | ***EECTRL*** | **9F** |
| **90** | ***P1*** | ***DIR1*** | *DPS* | | ***ERASE*** | | | | **97** |
| **88** | *TCON* | *TMOD* | *TL0* | *TL1* | *TH0* | *TH1* | *CKCON* | | **8F** |
| **80** | ***P0*** | *SP* | *DPL* | *DPH* | *DPL1* | *DPH1* | *WDTREL* | *PCON* | **87** |

**Table 7: Special Function Registers Locations**

Only a few addresses are occupied, the others are not implemented. SFRs specific to the 651X are shown in **bold** print. Any read access to unimplemented addresses will return undefined data, while any write access will have no effect. The registers at 0x80, 0x88, 0x90, etc., are bit-addressable, all others are byte-addressable.

### Special Function Registers (Generic 80515 SFRs)

Table 8 shows the location of the SFRs and the value they assume at reset or power-up.

| Name | Location | Reset value | Description |
|---|---|---|---|
| P0 | 0x80 | 0xFF | Port 0 |
| SP | 0x81 | 0x07 | Stack Pointer |
| DPL | 0x82 | 0x00 | Data Pointer Low 0 |
| DPH | 0x83 | 0x00 | Data Pointer High 0 |
| DPL1 | 0x84 | 0x00 | Data Pointer Low 1 |
| DPH1 | 0x85 | 0x00 | Data Pointer High 1 |
| WDTREL | 0x86 | 0x00 | Watchdog Timer Reload register |
| PCON | 0x87 | 0x00 | UART Speed Control |
| TCON | 0x88 | 0x00 | Timer/Counter Control |
| TMOD | 0x89 | 0x00 | Timer Mode Control |
| TL0 | 0x8A | 0x00 | Timer 0, low byte |
| TL1 | 0x8B | 0x00 | Timer 1, high byte |
| TH0 | 0x8C | 0x00 | Timer 0, low byte |
| TH1 | 0x8D | 0x00 | Timer 1, high byte |
| CKCON | 0x8E | 0x01 | Clock Control (Stretch=1) |
| P1 | 0x90 | 0xFF | Port 1 |
| DPS | 0x92 | 0x00 | Data Pointer select Register |
| S0CON | 0x98 | 0x00 | Serial Port 0, Control Register |
| S0BUF | 0x99 | 0x00 | Serial Port 0, Data Buffer |
| IEN2 | 0x9A | 0x00 | Interrupt Enable Register 2 |
| S1CON | 0x9B | 0x00 | Serial Port 1, Control Register |
| S1BUF | 0x9C | 0x00 | Serial Port 1, Data Buffer |
| S1RELL | 0x9D | 0x00 | Serial Port 1, Reload Register, low byte |
| P2 | 0xA0 | 0x00 | Port 2 |
| IEN0 | 0xA8 | 0x00 | Interrupt Enable Register 0 |
| IP0 | 0xA9 | 0x00 | Interrupt Priority Register 0 |
| S0RELL | 0xAA | 0xD9 | Serial Port 0, Reload Register, low byte |
| P3 | 0xB0 | 0xFF | Port 3 |
| IEN1 | 0xB8 | 0x00 | Interrupt Enable Register 1 |
| IP1 | 0xB9 | 0x00 | Interrupt Priority Register 1 |
| S0RELH | 0xBA | 0x03 | Serial Port 0, Reload Register, high byte |
| S1RELH | 0xBB | 0x03 | Serial Port 1, Reload Register, high byte |
| USR2 | 0xBF | 0x00 | User 2 Port, high address byte for MOVX@Ri |
| IRCON | 0xC0 | 0x00 | Interrupt Request Control Register |
| PSW | 0xD0 | 0x00 | Program Status Word |
| WDCON | 0xD8 | 0x00 | Baud Rate Control Register (only WDCON.7 bit used) |
| A | 0xE0 | 0x00 | Accumulator |
| B | 0xF0 | 0x00 | B Register |

**Table 8: Special Function Registers Reset Values**

**Accumulator (ACC, A):** ACC is the accumulator register. Most instructions use the accumulator to hold the operand. The mnemonics for accumulator-specific instructions refer to accumulator as "A", not ACC.

**B Register:** The B register is used during multiply and divide instructions. It can also be used as a scratch-pad register to hold temporary data.

**Program Status Word (PSW):**

MSB LSB

| CV | AC | F0 | RS1 | RS | OV | - | P |
|---|---|---|---|---|---|---|---|

**Table 9: PSW Register Flags**

| Bit | Symbol | Function |
|---|---|---|
| PSW.7 | CV | Carry flag |
| PSW.6 | AC | Auxiliary Carry flag for BCD operations |
| PSW.5 | F0 | General purpose Flag 0 available for user. **Not to be confused with the F0 flag in the CE STATUS register.** |
| PSW.4 | RS1 | Register bank select control bits. The contents of RS1 and RS0 select the working register bank: |
| PSW.3 | RS0 | |
| PSW.2 | OV | Overflow flag |
| PSW.1 | - | User defined flag |
| PSW.0 | P | Parity flag, affected by hardware to indicate odd / even number of "one" bits in the Accumulator, i.e. even parity. |

| RS1/RS0 | Bank selected | Location |
|---|---|---|
| 00 | Bank 0 | (0x00 – 0x07) |
| 01 | Bank 1 | (0x08 – 0x0F) |
| 10 | Bank 2 | (0x10 – 0x17) |
| 11 | Bank 3 | (0x18 – 0x1F) |

**Table 10: PSW bit functions**

**Stack Pointer (SP):** The stack pointer is a 1-byte register initialized to 0x07 after reset. This register is incremented before PUSH and CALL instructions, causing the stack to begin at location 0x08.

**Data Pointer:** The data pointer (DPTR) is 2 bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (MOV DPTR,#data16) or as two registers (e.g. MOV DPL,#data8). It is generally used to access external code or data space (e.g. MOVC A,@A+DPTR or MOVX A,@DPTR respectively).

**Program Counter:** The program counter (PC) is 2 bytes wide initialized to 0x0000 after reset. This register is incremented during the fetching operation code or when operating on data from program memory.

**Port Registers:** The I/O ports are controlled by Special Function Registers *P0*, *P1*, and *P2*. The contents of the SFR can be observed on corresponding pins on the chip. Writing a '1' to any of the ports (see Table 11) causes the corresponding pin to be at high level (V3P3), and writing a '0' causes the corresponding pin to be held at low level (GND). The data direction registers *DIR0*, *DIR1*, and *DIR2* define individual pins as input or output pins (see section On-Chip Resources – DIO Ports for details).

| Register | SFR Address | R/W | Description |
|---|---|---|---|
| *P0* | 0x80 | R/W | Register for port 0 read and write operations (pins DIO4…DIO7) |
| *DIR0* | 0xA2 | R/W | Data direction register for port 0. Setting a bit to 1 means that the corresponding pin is an output. |
| *P1* | 0x90 | R/W | Register for port 1 read and write operations (pins DIO8…DIO14) |
| *DIR1* | 0x91 | R/W | Data direction register for port 1. |
| *P2* | 0xA0 | R/W | Register for port 2 read and write operations (pins DIO17) |
| *DIR2* | 0xA1 | R/W | Data direction register for port 2. |

**Table 11: Port Registers**

All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR 'P0' to 'P3'), an output driver, and an input buffer, therefore the MPU can output or read data through any of these ports. Even if a DIO pin is configured as an output, the state of the pin can still be read by the MPU, for example when counting pulses issued via DIO pins that are under CE control.

### Special Function Registers Specific to the 71M6511

Table 12 shows the location and description of the 71M6511-specific SFRs.

| Register | Alternative Name | SFR Address | R/W | Description |
|---|---|---|---|---|
| *ERASE* | *FLSH_ERASE* | 0x94 | W | This register is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for *FLSH_ERASE* in order to initiate the appropriate Erase cycle (default = 0x00).<br>0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to *FLSH_PGADR* @ SFR 0xB7.<br>0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to *FLSH_MEEN* @ SFR 0xB2 and the debug port must be enabled.<br>Any other pattern written to FLSH_ERASE will have no effect. |
| *PGADDR* | *FLSH_PGADR* | 0xB7 | R/W | Flash Page Erase Address register containing the flash memory page address (page 0 thru 127) that will be erased during the Page Erase cycle (default = 0x00).<br>Must be re-written for each new Page Erase cycle. |
| *EEDATA* | | 0x9E | R/W | I2C EEPROM interface data register |
| *EECTRL* | | 0x9F | R/W | I2C EEPROM interface control register. If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit sequence. See the section I2C Interface (EEPROM) for a description of the command and status bits available for *EECTRL*. |

| | | | | |
|---|---|---|---|---|
| *FLSHCRL* | | 0xB2 | R/W | Bit 0 (*FLSH_PWE*): Program Write Enable:<br>0 – MOVX commands refer to XRAM Space, normal operation (default).<br>1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.<br>This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled. |
| | | | W | Bit 1 (*FLSH_MEEN*): Mass Erase Enable:<br>0 – Mass Erase disabled (default).<br>1 – Mass Erase enabled.<br>Must be re-written for each new Mass Erase cycle. |
| | | | R/W | Bit 6 (*SECURE*):<br>Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored. |
| | | | R | Bit 7 (*PREBOOT*):<br>Indicates that the preboot sequence is active. |
| *WDI* | | 0xE8 | | **Only byte operations on the whole WDI register should be used when writing**. The byte must have all bits set except the bits that are to be cleared.<br>The multi-purpose register *WDI* contains the following bits: |
| | | | R/W | Bit 0 (*IE_XFER*): XFER Interrupt Flag:<br>This flag monitors the XFER_BUSY interrupt. It is set by hardware and must be cleared by the interrupt handler |
| | | | R/W | Bit 1 (*IE_RTC*): RTC Interrupt Flag:<br>This flag monitors the RTC_1SEC interrupt. It is set by hardware and must be cleared by the interrupt handler |
| | | | W | Bit 7 (*WD_RST*): WD Timer Reset:<br>The WDT is reset when a 1 is written to this bit. |
| *INTBITS* | INT0…INT6 | 0xF8 | R | Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use |

**Table 12: Special Function Registers**

### Instruction Set

All instructions of the generic 8051 microcontroller are supported. A complete list of the instruction set and of the associated op-codes is contained in the 651X Software User's Guide (SUG).

### UART

The 71M6511 includes a UART (UART0) that can be programmed to communicate with a variety of AMR modules. A second UART (UART1) is connected to the optical port, as described in the optical port description.

The UART is a dedicated 2-wire serial interface, which can communicate with an external host processor at up to 38,400 bits/s ((with MPU clock = 1.2288MHz). The operation of each pin is as follows:

**RX**: Serial input data are applied at this pin. Conforming to RS-232 standard, the bytes are input LSB first. The voltage applied at RX must not exceed 3.6V.

**TX**: This pin is used to output the serial data. The bytes are output LSB first.

The 71M6511 has several UART-related registers, which can be read and written. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF options for variable communication baud rates from 300 to 38400 bps. Table 13 shows how the baud rates are calculated. Table 14 shows the selectable UART operation modes.

| | Using Timer 1 | Using Internal Baud Rate Generator |
|---|---|---|
| **Serial Interface 0** | $2^{smod} * f_{CKMPU}/ (384 * (256-TH1))$ | $2^{smod} * f_{CKMPU}/(64 * (2^{10}-S0REL))$ |
| **Serial Interface 1** | N/A | $f_{CKMPU}/(32 * (2^{10}-S1REL))$ |

**Note:** S0REL and S1REL are 10-bit values derived by combining bits from the respective timer reload registers. SMOD is the SMOD bit in the SFR *PCON*. TH1 is the high byte of timer 1.

**Table 13: Baud Rate Generation**

| | UART 0 | UART 1 |
|---|---|---|
| **Mode 0** | N/A | Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator) |
| **Mode 1** | Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator or timer 1) | Start bit, 8 data bits, stop bit, variable baud rate (internal baud rate generator) |
| **Mode 2** | Start bit, 8 data bits, parity, stop bit, fixed baud rate 1/32 or 1/64 of $f_{CKMPU}$ | N/A |
| **Mode 3** | Start bit, 8 data bits, parity, stop bit, variable baud rate (internal baud rate generator or timer 1) | N/A |

**Table 14: UART Modes**

Parity of serial data is available through the P flag of the accumulator. Seven-bit serial modes with parity, such as those used by the FLAG protocol, can be simulated by setting and reading bit 7 of 8-bit output data. Seven-bit serial modes without parity can be simulated by setting bit 7 to a constant 1. 8-bit serial modes with parity can be simulated by setting and reading the 9$^{th}$ bit, using the control bits TB80 (S0CON.3) and TB81 (S1CON.3) in the S0COn and S1CON SFRs for transmit and RB81 (S1CON.2) for receive operations. SM20 (S0CON.5) and SM21 (S1CON.5) can be used as handshake signals for inter-processor communication in multi-processor systems.

**Serial Interface 0 Control Register (S0CON).**

The function of the UART0 depends on the setting of the Serial Port Control Register S0CON.

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SM0 | SM1 | SM20 | REN0 | TB80 | RB80 | TI0 | RI0 |

**Table 15: The S0CON Register**

**Serial Interface 1 Control Register (S1CON).**

The function of the serial port depends on the setting of the Serial Port Control Register S1CON.

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SM | - | SM21 | REN1 | TB81 | RB81 | TI1 | RI1 |

**Table 16: The S1CON register**

| Bit | Symbol | Function |
|---|---|---|
| S0CON.7 | SM0 | These two bits set the UART0 mode: |
| S0CON.6 | SM1 | |
| S0CON.5 | SM20 | Enables the inter-processor communication feature. |
| S0CON.4 | REN0 | If set, enables serial reception. Cleared by software to disable reception. |
| S0CON.3 | TB80 | The 9th transmitted data bit in Modes 2 and 3. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.) |
| S0CON.2 | RB80 | In Modes 2 and 3 it is the 9th data bit received. In Mode 1, if SM20 is 0, RB80 is the stop bit. In Mode 0 this bit is not used. Must be cleared by software |
| S0CON.1 | TI0 | Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software. |
| S0CON.0 | RI0 | Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software |

| Mode | Description | SM0 | SM1 |
|---|---|---|---|
| 0 | N/A | 0 | 0 |
| 1 | 8-bit UART | 0 | 1 |
| 2 | 9-bit UART | 1 | 0 |
| 3 | 9-bit UART | 1 | 1 |

**Table 17: The S0CON Bit Functions**

Note: The speed in Mode 2 depends on the SMOD bit in the SFR PCON. See the PCON register description.

| Bit | Symbol | Function |
|---|---|---|
| S1CON.7 | SM | Sets the baud rate for UART1 |
| S1CON.5 | SM21 | Enables the inter-processor communication feature. |
| S1CON.4 | REN1 | If set, enables serial reception. Cleared by software to disable reception. |
| S1CON.3 | TB81 | The 9th transmitted data bit in Mode A. Set or cleared by the MPU, depending on the function it performs (parity check, multiprocessor communication etc.) |
| S1CON.2 | RB81 | In Modes 2 and 3, it is the 9th data bit received. In Mode B, if sm21 is 0, rb81 is the stop bit. Must be cleared by software |
| S1CON.1 | TI1 | Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software. |
| S1CON.0 | RI1 | Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software |

| SM | Mode | Description | Baud Rate |
|---|---|---|---|
| 0 | A | 9-bit UART | variable |
| 1 | B | 8-bit UART | variable |

**Table 18: The S1CON Bit Functions**

## Timers and Counters

The 80515 has two 16-bit timer/counter registers: Timer 0 and Timer 1. These registers can be configured for counter or timer operations.

In timer mode, the register is incremented every machine cycle meaning that it counts up after every 12 periods of the MPU clock signal.

In counter mode, the register is incremented when the falling edge is observed at the corresponding input signal T0 or T1 (T0 and T1 are the timer gating inputs derived from certain DIO pins, see the DIO Ports chapter). Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function Registers (TMOD and TCON) are used to select the appropriate mode.

**Timer/Counter Mode Control register (TMOD):**

MSB LSB

| GATE | C/T | M1 | M0 | GATE | C/T | M1 | M0 |
|---|---|---|---|---|---|---|---|
| Timer 1 | | | | Timer 0 | | | |

**Table 19: The TMOD Register**

Bits TR1 (TCON.6) and TR0 (TCON.4) in the TCON register (see Table 22 and Table 23) start their associated timers when set.

| Bit | Symbol | Function |
|---|---|---|
| TMOD.7<br>TMOD.3 | Gate | If set, enables external gate control (pin int0 or int1 for Counter 0 or 1, respectively). When int0 or int1 is high, and TRX bit is set (see TCON register), a counter is incremented every falling edge on t0 or t1 input pin |
| TMOD.6<br>TMOD.2 | C/T | Selects Timer or Counter operation. When set to 1, a Counter operation is performed. When cleared to 0, the corresponding register will function as a Timer. |
| TMOD.5<br>TMOD.1 | M1 | Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description. |
| TMOD.4<br>TMOD.0 | M0 | Selects the mode for Timer/Counter 0 or Timer/Counter 1, as shown in TMOD description. |

**Table 20: TMOD Register Bit Description**

| M1 | M0 | Mode | Function |
|---|---|---|---|
| 0 | 0 | Mode 0 | 13-bit Counter/Timer with 5 lower bits in the TL0 or TL1 register and the remaining 8 bits in the TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are held at zero. |
| 0 | 1 | Mode 1 | 16-bit Counter/Timer. |
| 1 | 0 | Mode2 | 8-bit auto-reload Counter/Timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TL(x) overflows, a value from TH(x) is copied to TL(x). |
| 1 | 1 | Mode3 | If Timer 1 M1 and M0 bits are set to '1', Timer 1 stops. If Timer 0 M1 and M0 bits are set to '1', Timer 0 acts as two independent 8-bit Timer/Counters. |

**Table 21: Timers/Counters Mode Description**

Note: TL0 is affected by TR0 and gate control bits, and sets TF0 flag on overflow.
TH0 is affected by TR1 bit, and sets TF1 flag on overflow.

**Timer/Counter Control Register (TCON)**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

**Table 22: The TCON Register**

| Bit | Symbol | Function |
|---|---|---|
| TCON.7 | TF1 | The Timer 1 overflow flag is set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed. |
| TCON.6 | TR1 | Timer 1 Run control bit. If cleared, Timer 1 stops. |
| TCON.5 | TF0 | Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when an interrupt is processed. |
| TCON.4 | TR0 | Timer 0 Run control bit. If cleared, Timer 0 stops. |
| TCON.3 | IE1 | Interrupt 1 edge flag is set by hardware when the falling edge on external pin int1 is observed. Cleared when an interrupt is processed. |
| TCON.2 | IT1 | Interrupt 1 type control bit. Selects either the falling edge or low level on input pin to cause an interrupt. |
| TCON.1 | IE0 | Interrupt 0 edge flag is set by hardware when the falling edge on external pin int0 is observed. Cleared when an interrupt is processed. |
| TCON.0 | IT0 | Interrupt 0 type control bit. Selects either the falling edge or low level on input pin to cause interrupt. |

**Table 23: The TCON Register Bit Functions**

Table 24 specifies the combinations of operation modes allowed for timer 0 and timer 1:

| | Timer 1 | | |
|---|---|---|---|
| | **Mode 0** | **Mode 1** | **Mode 2** |
| **Timer 0 - mode 0** | YES | YES | YES |
| **Timer 0 - mode 1** | YES | YES | YES |
| **Timer 0 - mode 2** | Not allowed | Not allowed | YES |

**Table 24: Timer Modes**

**Timer/Counter Mode Control register (PCON):**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SMOD | | | | | | | |

**Table 25: The PCON Register**

The SMOD bit in the PCON register doubles the baud rate when set.

### WD Timer (Software Watchdog Timer)

The software watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After a reset, the watchdog timer is disabled and all registers are set to zero. The watchdog consists of a 16-bit counter (WDT), a reload register (WDTREL), prescalers (by 2 and by 16), and control logic. Once the watchdog is started, it cannot be stopped unless the internal reset signal becomes active.

**Note: It is recommended to use the hardware watchdog timer instead of the software watchdog timer.**

**WD Timer Start Procedure:** The WDT is started by setting the SWDT flag. When the WDT register enters the state 0x7CFF, an asynchronous WDTS signal will become active. The signal WDTS sets bit 6 in the IP0 register and requests a reset state. WDTS is cleared either by the reset signal or by changing the state of the WDT timer.

**Refreshing the WD Timer:** The watchdog timer must be refreshed regularly to prevent the reset request signal from becoming active. This requirement imposes an obligation on the programmer to issue two instructions. The first instruction sets WDT and the second instruction sets SWDT. The maximum delay allowed between setting WDT and SWDT is 12 clock cycles. If this period has expired and SWDT has not been set, WDT is automatically reset, otherwise the watchdog timer is reloaded with the content of the WDTREL register and WDT is automatically reset. Since the WDT requires exact timing, firmware needs to be designed with special care in order to avoid unwanted WDT resets. TERIDIAN strongly discourages the use of the software WDT.

**Special Function Registers for the WD Timer**

**Interrupt Enable 0 Register (IEN0):**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EAL | WDT | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 |

**Table 26: The IEN0 Register (see also Table 34)**

| Bit | Symbol | Function |
|---|---|---|
| IEN0.6 | WDT | Watchdog timer refresh flag.<br>Set to initiate a refresh of the watchdog timer. Must be set directly before SWDT is set to prevent an unintentional refresh of the watchdog timer. WDT is reset by hardware 12 clock cycles after it has been set. |

**Table 27: The IEN0 Bit Functions (see also Table 34)**

Note: The remaining bits in the IEN0 register are not used for watchdog control

**Interrupt Enable 1 Register (IEN1):**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| EXEN2 | SWDT | EX6 | EX5 | EX4 | EX3 | EX2 | |

**Table 28: The IEN1 Register (see also Tables 35/36)**

| Bit | Symbol | Function |
|---|---|---|
| IEN1.6 | SWDT | Watchdog timer start/refresh flag.<br>Set to activate/refresh the watchdog timer. When directly set after setting WDT, a watchdog timer refresh is performed. Bit SWDT is reset by the hardware 12 clock cycles after it has been set. |

**Table 29: The IEN1 Bit Functions (see also Tables 35/36)**

Note: The remaining bits in the IEN1 register are not used for watchdog control

**Interrupt Priority 0 Register (IP0):**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| -- | WDTS | IP0.5 | IP0.4 | IP0.3 | IP0.2 | IP0.1 | IP0.0 |

**Table 30: The IP0 Register (see also Table 46)**

| Bit | Symbol | Function |
|---|---|---|
| IP0.6 | WDTS | Watchdog timer status flag. Set when the watchdog timer was started. Can be read by software. |

**Table 31: The IP0 bit Functions (see also Table 46)**

Note: The remaining bits in the IP0 register are not used for watchdog control

**Watchdog Timer Reload Register (WDTREL):**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Table 32: The WDTREL Register**

| Bit | Symbol | Function |
|---|---|---|
| WDTREL.7 | 7 | Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler |
| WDTREL.6 to WDTREL.0 | 6-0 | Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the WDT when a refresh is triggered by a consecutive setting of bits WDT and SWDT. |

**Table 33: The WDTREL Bit Functions**

The WDTREL register can be loaded and read at any time.

## Interrupts

The 80515 provides 11 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register (TCON, IRCON, and SCON). Each interrupt requested by the corresponding flag can be individually enabled or disabled by the enable bits in SFRs IEN0, IEN1, and IEN2.

External interrupts are the interrupts external to the 80515 core, i.e. signals that originate in other parts of the 71M6511/6511H, for example the CE, DIO, RTC EEPROM interface, comparators.

**Interrupt Overview:** When an interrupt occurs, the MPU will vector to the predetermined address as shown in Table 51. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction, "RETI". When a RETI instruction is performed, the processor will return to the instruction that would have been next when the interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, then samples are polled by the hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then the interrupt request flag is set. On the next instruction cycle, the interrupt will be acknowledged by hardware forcing an LCALL to the appropriate vector address, if the following conditions are met:

- No interrupt of equal or higher priority is already in progress.
- An instruction is currently being executed and is not completed.
- The instruction in progress is not RETI or any write access to the registers IEN0, IEN1, IEN2, IP0 or IP1.

Interrupt response will require a varying amount of time depending on the state of the MPU when the interrupt occurs. If the MPU is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on the current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles to perform the LCALL.

**Special Function Registers for Interrupts:**

**Interrupt Enable 0 register (IE0)**

MSB LSB

| EAL | WDT | | ES0 | ET1 | EX1 | ET0 | EX0 |
|---|---|---|---|---|---|---|---|

**Table 34: The IEN0 Register**

| Bit | Symbol | Function |
|---|---|---|
| IEN0.7 | EAL | EAL=0 – disable all interrupts |
| IEN0.6 | WDT | Not used for interrupt control |
| IEN0.5 | - | |
| IEN0.4 | ES0 | ES0=0 – disable serial channel 0 interrupt |
| IEN0.3 | ET1 | ET1=0 – disable timer 1 overflow interrupt |
| IEN0.2 | EX1 | EX1=0 – disable external interrupt 1 |
| IEN0.1 | ET0 | ET0=0 – disable timer 0 overflow interrupt |
| IEN0.0 | EX0 | EX0=0 – disable external interrupt 0 |

**Table 35: The IEN0 Bit Functions**

**Interrupt Enable 1 Register (IEN1)**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | SWDT | EX6 | EX5 | EX4 | EX3 | EX2 | |

**Table 36: The IEN1 Register**

| Bit | Symbol | Function |
|---|---|---|
| IEN1.7 | - | |
| IEN1.6 | SWDT | Not used for interrupt control |
| IEN1.5 | EX6 | EX6=0 – disable external interrupt 6 |
| IEN1.4 | EX5 | EX5=0 – disable external interrupt 5 |
| IEN1.3 | EX4 | EX4=0 – disable external interrupt 4 |
| IEN1.2 | EX3 | EX3=0 – disable external interrupt 3 |
| IEN1.1 | EX2 | EX2=0 – disable external interrupt 2 |
| IEN1.0 | - | |

**Table 37: The IEN1 Bit Functions**

**Interrupt Enable 2 register (IE2)**

MSB LSB

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | ES1 |

**Table 38: The IEN2 Register**

| Bit | Symbol | Function |
|---|---|---|
| IEN2.0 | ES1 | ES1=0 – disable serial channel 1 interrupt |

**Table 39: The IEN2 Bit Functions**

**Timer/Counter Control register (TCON)**

MSB LSB

| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |
|---|---|---|---|---|---|---|---|

**Table 40: The TCON Register**

| Bit | Symbol | Function |
|---|---|---|
| TCON.7 | TF1 | Timer 1 overflow flag |
| TCON.6 | TR1 | Not used for interrupt control |
| TCON.5 | TF0 | Timer 0 overflow flag |
| TCON.4 | TR0 | Not used for interrupt control |
| TCON.3 | IE1 | External interrupt 1 flag |
| TCON.2 | IT1 | External interrupt 1 type control bit |
| TCON.1 | IE0 | External interrupt 0 flag |
| TCON.0 | IT0 | External interrupt 0 type control bit |

**Table 41: The TCON Bit Functions**

**Interrupt Request register (IRCON)**

MSB LSB

| | | EX6 | IEX5 | IEX4 | IEX3 | IEX2 | |
|---|---|---|---|---|---|---|---|

**Table 42: The IRCON Register**

| Bit | Symbol | Function |
|---|---|---|
| IRCON.7 | - | |
| IRCON.6 | - | |
| IRCON.5 | IEX6 | External interrupt 6 edge flag |
| IRCON.4 | IEX5 | External interrupt 5 edge flag |
| IRCON.3 | IEX4 | External interrupt 4 edge flag |
| IRCON.2 | IEX3 | External interrupt 3 edge flag |
| IRCON.1 | IEX2 | External interrupt 2 edge flag |
| IRCON.0 | - | |

**Table 43: The IRCON Bit Functions**

Note: Only TF0 and TF1 (timer 0 and timer 1 overflow flag) will be automatically cleared by hardware when the service routine is called (Signals T0ACK and T1ACK – port ISR – active high when the service routine is called).

## External Interrupts

The external interrupts are connected as shown in Table 44. The polarity of interrupts 2 and 3 is programmable in the MPU. Interrupts 2 and 3 should be programmed for falling sensitivity. The generic 8051 MPU literature states that interrupts 4 through 6 are defined as rising edge sensitive. Thus, the hardware signals attached to interrupts 5 and 6 are inverted to achieve the edge polarity shown in Table 44.

SFR (special function register) enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5).

XFER_BUSY and RTC_1SEC, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 45), and these interrupts must be cleared by the MPU software.

| External Interrupt | Connection | Polarity | Flag Reset |
|---|---|---|---|
| 0 | Digital I/O High Priority | see *DIO_Rx* | automatic |
| 1 | Digital I/O Low Priority | see *DIO_Rx* | automatic |
| 2 | Comparator 2 or 3 | falling | automatic |
| 3 | CE_BUSY | falling | automatic |
| 4 | Comparator 2 or 3 | rising | automatic |
| 5 | EEPROM busy | falling | automatic |
| 6 | XFER_BUSY OR RTC_1SEC | falling | manual |

**Table 44: External MPU Interrupts**

Interrupt 6 is edge-sensitive. The RTC_1SEC interrupt from the RTC and the XFER_BUSY interrupt from the CE are combined using a logic OR function and the result is routed into interrupt 6. Therefore, both flags must be cleared at least once during initialization, and both flags must always be cleared before exiting the interrupt service routine (ISR) for interrupt 6.

Note 1: If clearing of both flags is not performed, then no edge can occur to trigger interrupt 6 later resulting in the ISR for the XFER_BUSY ceasing to run.

Note 2: Clearing both flags reliably requires some care. Either flag can be set by hardware while interrupt 6 code is running on behalf of the other interrupt. In this situation, the unprocessed interrupt can create a lockout condition similar to the one in note 1. To prevent this lockout one must always process both interrupt flags in the same service routine.

Note 3: After a reset from an in-circuit emulator, the *IE_XFER* flag may not be cleared because the CE may continue to run.

The flags for the RTC_1SEC and the XFER_BUSY interrupts are located in the *WDI* SFR (address 0xE8).

| Enable Bit | Description |
|---|---|
| EX0 | Enable external interrupt 0 |
| EX1 | Enable external interrupt 1 |
| EX2 | Enable external interrupt 2 |
| EX3 | Enable external interrupt 3 |
| EX4 | Enable external interrupt 4 |
| EX5 | Enable external interrupt 5 |
| EX6 | Enable external interrupt 6 |
| *EX_XFER* | Enable XFER_BUSY interrupt |
| *EX_RTC* | Enable RTC_1SEC interrupt |

| Flag Bit | Description |
|---|---|
| IE0 | External interrupt 0 flag |
| IE1 | External interrupt 1 flag |
| IEX2 | External interrupt 2 flag |
| IEX3 | External interrupt 3 flag |
| IEX4 | External interrupt 4 flag |
| IEX5 | External interrupt 5 flag |
| IEX6 | External interrupt 6 flag |
| *IE_XFER* | XFER_BUSY interrupt flag |
| *IE_RTC* | RTC_1SEC interrupt flag |

**Table 45: Control Bits for External Interrupts**

### Interrupt Priority Level Structure

All interrupt sources are combined in groups, as shown in Table 46:

| Group | | | |
|---|---|---|---|
| **0** | External interrupt 0 | Serial channel 1 interrupt | |
| **1** | Timer 0 interrupt | - | External interrupt 2 |
| **2** | External interrupt 1 | - | External interrupt 3 |
| **3** | Timer 1 interrupt | - | External interrupt 4 |
| **4** | Serial channel 0 interrupt | - | External interrupt 5 |
| **5** | - | - | External interrupt 6 |

**Table 46: Priority Level Groups**

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level are received simultaneously, an internal polling sequence as per Table 50 determines which request is serviced first.

IEN enable bits must be set to permit any of these interrupts to occur. Likewise, each interrupt has its own flag bit that is set by the interrupt hardware and is reset automatically by the MPU interrupt handler (0 through 5). XFER_BUSY and RTC_1SEC, which are OR-ed together, have their own enable and flag bits in addition to the interrupt 6 enable and flag bits (see Table 45), and these interrupts must be cleared by the MPU software.

An overview of the interrupt structure is given in Figure 7.

**Interrupt Priority 0 Register (IP0)**

MSB LSB

| -- | WDTS | IP0.5 | IP0.4 | IP0.3 | IP0.2 | IP0.1 | IP0.0 |
|---|---|---|---|---|---|---|---|

**Table 47: The IP0 Register:**

Note: WDTS is not used for interrupt controls

**Interrupt Priority 1 Register (IP1)**

MSB LSB

| - | - | IP1.5 | IP1.4 | IP1.3 | IP1.2 | IP1.1 | IP1.0 |
|---|---|---|---|---|---|---|---|

**Table 48: The IP1 Register:**

| IP1.x | IP0.x | Priority Level |
|---|---|---|
| 0 | 0 | Level0 (lowest) |
| 0 | 1 | Level1 |
| 1 | 0 | Level2 |
| 1 | 1 | Level3 (highest) |

**Table 49: Priority Levels**

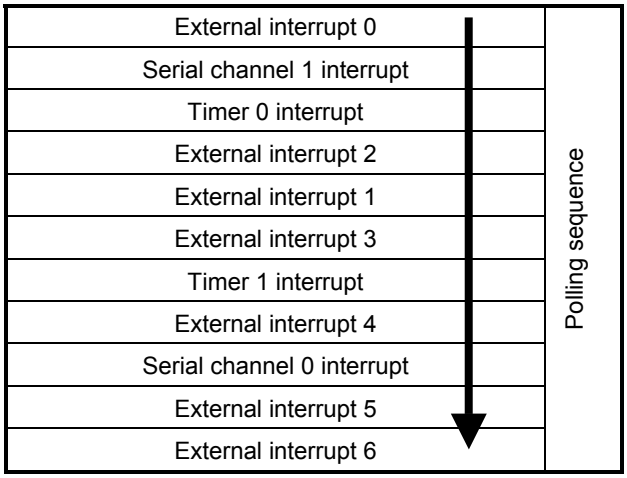



**Table 50: Interrupt Polling Sequence**

### Interrupt Sources and Vectors

Table 51 shows the interrupts with their associated flags and vector addresses.

| Interrupt Request Flag | Description | Interrupt Vector Address |
|---|---|---|
| IE0 | External interrupt 0 | 0x0003 |
| TF0 | Timer 0 interrupt | 0x000B |
| IE1 | External interrupt 1 | 0x0013 |
| TF1 | Timer 1 interrupt | 0x001B |
| RI0/TI0 | Serial channel 0 interrupt | 0x0023 |
| RI1/TI1 | Serial channel 1 interrupt | 0x0083 |
| IEX2 | External interrupt 2 | 0x004B |
| IEX3 | External interrupt 3 | 0x0053 |
| IEX4 | External interrupt 4 | 0x005B |
| IEX5 | External interrupt 5 | 0x0063 |
| IEX6 | External interrupt 6 | 0x006B |

**Table 51: Interrupt Vectors**

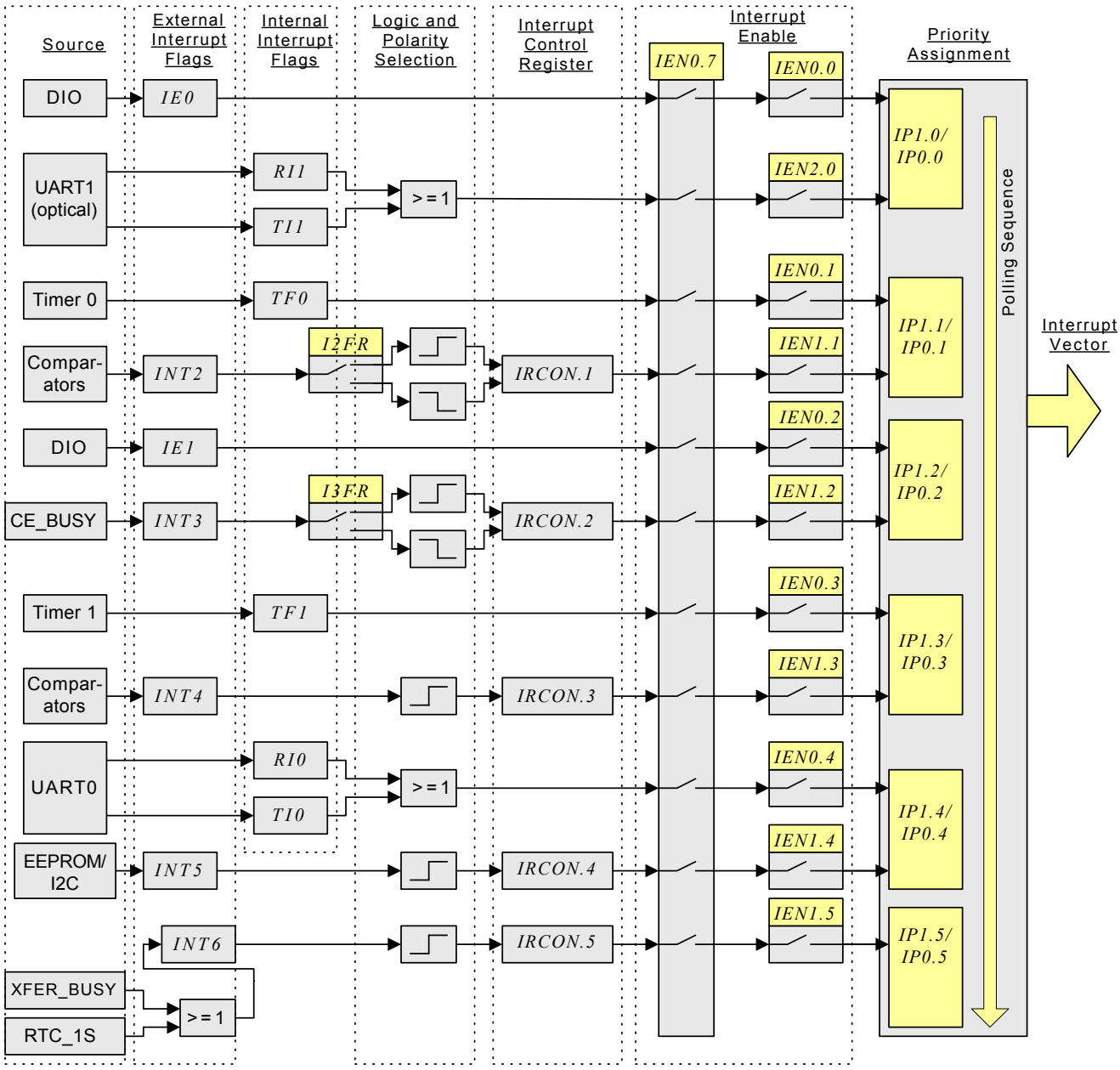



**Figure 7: Interrupt Structure**

## On-Chip Resources

### DIO Ports

The 71M6511/6511H includes up to 12 pins of general purpose digital I/O. These pins are dual function and can alternatively be used as LCD drivers. Figure 8 shows a block diagram of the DIO section.

On reset or power-up, all DIO pins are inputs until they are configured for the desired direction. The pins are configured and controlled by the *DIO* and *DIO_DIR* registers (SFRs) and by the five bits of the I/O register *LCD_NUM* (0x2020[4:0]). See the description for *LCD_NUM* in the I/O RAM Section for a table listing the available segment pins versus DIO pins, depending on the selection for *LCD_NUM*. Generally, increasing the value for *LCD_NUM* will configure an increasing number of general purpose pins to be LCD segment pins, starting at the higher pin numbers.

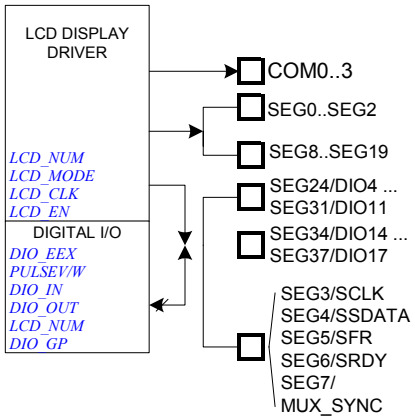



**Figure 8: DIO Ports Block Diagram**

Each pin declared as DIO can be configured independently as an input or output with the bits of the *DIO_DIRn* registers. Table 52 lists the direction registers and configurability associated with each group of DIO pins. Table 53 shows the configuration for a DIO pin through its associated bit in its *DIO_DIR* register.

| DIO | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin number | -- | -- | -- | -- | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | -- | -- | 20 | 21 |
| Data Register bit | -- | -- | -- | -- | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | -- | -- | 6 | 7 |
| | *DIO0=P0* (SFR 0x80) | | | | | | | | *DIO1=P1* (SFR 0x90) | | | | | | | |
| Direction Register bit | -- | -- | -- | -- | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | -- | -- | 6 | 7 |
| | *DIO_DIR0* (SFR 0xA2) | | | | | | | | *DIO_DIR1* (SFR 0x91) | | | | | | | |
| Internal Resources Configurable | -- | -- | -- | -- | Y | Y | Y | Y | Y | Y | Y | Y | -- | -- | N | N |

| DIO | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
|---|---|---|---|---|---|---|---|---|
| Pin number | 22 | 12 | -- | -- | -- | -- | -- | -- |
| Data Register bit | 0 | 1 | -- | -- | -- | -- | -- | -- |
| | *DIO2=P2* (SFR 0xA0) | | | | | | | |
| Direction Register bit | 0 | 1 | -- | -- | -- | -- | -- | -- |
| | *DIO_DIR2* (SFR 0xA1) | | | | | | | |
| Internal Resources Configurable | N | N | -- | -- | -- | -- | -- | -- |

**Table 52: Data/Direction Registers and Internal Resources for DIO Pin Groups**

| | *DIO_DIR* bit | |
|---|---|---|
| | **0** | **1** |
| **DIO Pin Function** | input | output |

**Table 53: *DIO_DIR* Control Bit**

Values read from and written into the DIO ports use the data registers *P0*, *P1* and *P2*.

A 3-bit configuration word, I/O RAM register, *DIO_Rx* (0x2009[2:0] through 0x200E[6:4]) can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control (see Table 52 for DIO pins available for this option). This way, DIO pins can be tracked even if they are configured as outputs. This feature is useful for pulse counting. The control resources selectable for the DIO pins are listed in Table 54. If more than one input is connected to the same resource, the resources are combined using a logical OR.

| *DIO_R* Value | Resource Selected for DIO Pin |
|---|---|
| 0 | NONE |
| 1 | Reserved |
| 2 | T0 (counter0 clock) |
| 3 | T1 (counter1 clock) |
| 4 | High priority I/O interrupt (INT0 rising) |
| 5 | Low priority I/O interrupt (INT1 rising) |
| 6 | High priority I/O interrupt (INT0 falling) |
| 7 | Low priority I/O interrupt (INT1 falling) |

**Table 54: Selectable Controls using the *DIO_DIR* Bits**

Additionally, if DIO6 and DIO7 are declared outputs, they can be configured as dedicated pulse outputs (WPULSE = DIO6, VARPULSE = DIO7) using the I/O RAM registers *DIO_PW* (0x2008[2]) and *DIO_PV* (0x2008[3]). In this case, DIO6 and DIO7 are under CE control. DIO4 and DIO5 can be configured to implement the EEPROM Interface by setting the I/O RAM register *DIO_EEX* (0x2008[4]).

### Physical Memory

Data bus address space is allocated to on-chip memory as shown in Table 55.

| Address (hex) | Memory Technology | Memory Type | Typical Usage | Wait States (at 5MHz) | Memory Size (bytes) |
|---|---|---|---|---|---|
| 0000-FFFF | Flash Memory | Non-volatile | Program and non-volatile data | 0 | 64KB |
| 0000-07FF | Static RAM | Battery-buffered | MPU data | 0 | 2KB |
| 1000-13FF | Static RAM | Volatile | CE data | 5 | 1KB |
| 2000-20FF | Static RAM | Volatile | Configuration RAM (I/O RAM) | 0 | 256 |
| 3000-3FFF | Static RAM | Volatile | CE Program code | 5 | 4KB |

**Table 55: MPU Data Memory Map**

**Flash Memory:** The 71M6511 includes 64KB of on-chip flash memory. The flash memory is intended to primarily contain MPU program code. In a typical application, it also contains images of the CE program code, CE coefficients, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU must copy these images to their respective memory locations.

The I/O RAM bit register *FLASH66Z* defines the pulse width for accessing flash memory. **To minimize supply current draw, this bit should be set to 1**.

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94)

Note: The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1]
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94)

Writing to flash memory:

The MPU may write to the flash memory for non-volatile data storage or when implementing a boot-loader. The I/O RAM register *FLSH_PWE* (flash program write enable, SFR B2[0]) differentiates 80515 data store instructions (MOVX@DPTR,A) between Flash and XRAM writes. Before setting *FLSH_PWE*, all interrupts need to be disabled by setting EAL =1. After the write operation, *FLSH_PWE* must be cleared.

The original state of a flash byte is 0xFF (all bits are 1). Overwriting programmed flash cells with a different value usually requires that the cell is erased first. Since cells cannot be erased individually, the page has to be copied to RAM, followed by a page erase. After this, the page can be updated in RAM and then written back to the flash memory.

Writing to flash locations will affect the corresponding XRAM cells, i.e. 0x2000 to 0x20FF (I/O RAM), 0x0000 to 0x07FF (MPU RAM), plus CE DRAM and CE PRAM. It is critical to maintain the integrity of the cells 0x2000…0x2007 as a minimum (where important system settings are stored) during the flash-write operation. This can be achieved by excluding the critical addresses from the write operation.

**MPU RAM**: The 71M6511 includes 2KB of static RAM memory on-chip (XRAM), which are backed-up by the battery plus 256-bytes of internal RAM in the MPU core. The 2KB of static RAM are used for data storage during normal MPU operations.

**CE DRAM:** The CE DRAM is the data memory of the CE. The MPU can read and write the CE DRAM as the primary means of data communication between the two processors.

**CE PRAM:** The CE PRAM is the program memory of the CE. The CE PRAM has to be loaded with CE code before the CE starts operating. CE PRAM cannot be accessed by the MPU when the CE is running.

### Oscillator

The oscillator drives a standard 32.768kHz watch crystal (see Figure 9). Crystals of this type are accurate and do not require a high current oscillator circuit. The oscillator in the TERIDIAN 71M6511 Power Meter IC has been designed specifically to handle watch crystals and is compatible with their high impedance and limited power handling capability. The oscillator power dissipation is very low to maximize the lifetime of any battery backup device attached to the VBAT pin.

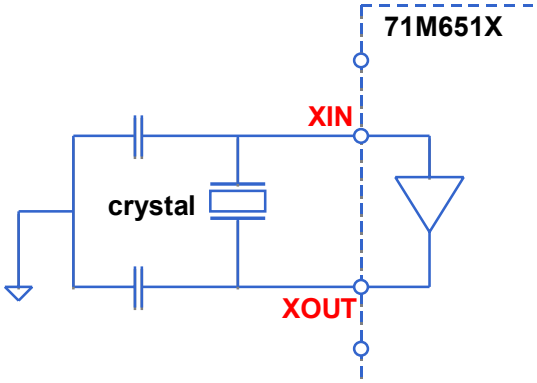



**Figure 9: Oscillator Circuit**

**The oscillator should be placed as close as possible to the IC, and vias should be avoided. An external resistor across the crystal must not be added.**

### Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. In the absence of the 3.3V supply, the RTC is powered by the external battery (VBAT pin). The RTC consists of a counter chain and output registers. The counter chain consists of seconds, minutes, hours, day of week, day of month, month, and year. The RTC is capable of processing leap years. Each counter has its own output register. Whenever the MPU reads the seconds register, all other output registers are automatically updated. Since the RTC clock is not coherent to the MPU clock, the MPU must read the seconds register until two consecutive reads are the same (requires either 2 or 3 reads). At this point, all RTC output registers will have the correct time. Regardless of the MPU clock speed, RTC reads require one wait state.

The RTC interrupt must be enabled using the I/O RAM register *EX_RTC* (address 0x2002[1]). RTC time is set by writing to the I/O RAM registers *RTC_SEC*, *RTC_MIN,* through *RTC_YR*. Each byte written to RTC must be delayed at least 3 CK32 cycles from any previous byte written to RTC.

Two time correction bits, the I/O RAM registers *RTC_DEC_SEC* (0x201C[1]) and *RTC_INC_SEC* (0x201C[0]) are provided to adjust the RTC time. A pulse on one of these bits causes the time to be decremented or incremented by an additional second at the next update of the *RTC_SEC* register. Thus, if the crystal temperature coefficient is known, the MPU firmware can integrate temperature and correct the RTC time as necessary as discussed in temperature compensation.

### LCD Drivers

The 71M6511 contains 15 dedicated LCD segment pins, 5 LCD segment pins that rare shared with the SSI port and/or other functions, and an additional 12 multi-purpose pins (LCD/DIO) that may be configured as LCD segment drivers (see I/O RAM register *LCD_NUM*). Thus, the 71M6511/6511H is capable of driving between 80 to 128 pixels of LCD display with 25% duty cycle. At seven segments per digit, the LCD can be designed for 11 to 18 digits for display. Since each pixel is addressed individually, the LCD display can be a combination of alphanumeric digits and enunciator symbols. The information to be displayed is written into the lower four bits of I/O RAM registers *LCD_SEG0* through *LCD_SEG37*. Bit 0 corresponds to the segment selected when COM0 pin is active while bit 1 is allocated to COM1.

The LCD driver circuitry is grouped into four common outputs (COM0 to COM3) and up to 32 segment outputs (see Table 56).

| | Dedicated Segment Pins | | | | Shared w/ DIO4-DIO11 | | | Shared w/ DIO14-DIO17 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SEG0 | SEG1 | … | SEG19 | SEG24 | … | SEG31 | SEG34 | … | SEG37 |
| COM0 | P0 | P4 | … | P76 | P80 | … | P108 | P112 | … | P124 |
| COM1 | P1 | P5 | … | P77 | P81 | … | P109 | P113 | ... | P125 |
| COM2 | P2 | P6 | … | P78 | P82 | … | P110 | P114 | … | P126 |
| COM3 | P3 | P7 | … | P79 | P83 | … | P111 | P115 | … | P127 |

**Table 56: Liquid Crystal Display Segment Table (Typical)**

Note: P0, P1, … Represent the pixel/segment numbers on the LCD.

A charge pump suitable for driving VLCD is included on-chip. This circuit creates 5V from the 3.3V supply. A contrast DAC is provided that permits the LCD full-scale voltage to be adjusted between VLCD and 70% of VLCD. The *LCD_NUM* register defines the number of dual purpose pins used for LCD segment interface.

### LCD Voltage Boost Circuitry

A voltage boost circuit may be used to generate 5V from the 3.3V supply to support low-power 5V devices, such as LCDs. Figure 10 shows a block diagram of the voltage boost circuitry including the voltage regulators for V2P5 and V2P5NV. When activated using the I/O RAM register *LCD_BSTEN* (0x2020[7]), the boost circuitry provides an AC voltage at the VDRV output pin (see the Applications section for details).

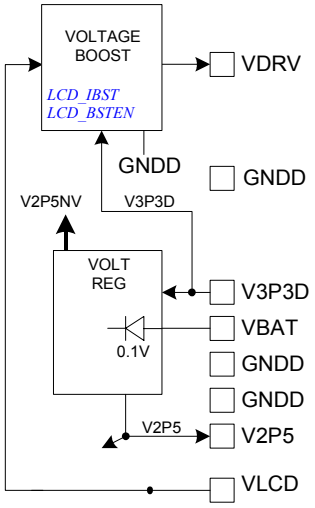



**Figure 10: LCD Voltage Boost Circuitry**

### UART (UART0) and Optical Port (UART1)

The 71M6511/6511H includes an interface to implement an IR or optical port. The pin OPT_TX is designed to directly drive an external LED for transmitting data on an optical link (low-active). The pin OPT_RX, also low-active, is designed to sense the input from an external photo detector used as the receiver for the optical link. These two pins are connected to a dedicated UART port. OPT_TX can be tristated if it is desired to multiplex another I/O pin to the OPT_TX output. The control bit for the OPT_TX output is the I/O RAM register *OPT_TXDIS* (0x2008[5]).

### Hardware Reset Mechanisms

Several conditions will cause a hardware reset of the 71M6511/6511H:

- Voltage at the RESETZ pin low
- Voltage at the E_RST pin low
- Voltage at the V1 pin below reset threshold (VBIAS)
- The crystal frequency monitor detected a crystal malfunction
- Hardware Watchdog timer

### Reset Pin (RESETZ)

When the RESETZ pin is pulled low (or when V1 < VBIAS), all digital activity in the chip stops while analog circuits are still active. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are cleared.

### Hardware Watchdog Timer

In addition to the basic software watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, hardware watchdog timer (WDT) is included in the 71M6511/6511H. This timer will reset the MPU if it is not refreshed periodically, and can be used to recover the MPU in situations where program control is lost.

The watchdog timer uses the RTC crystal oscillator as its time base and requires a reset under MPU program control at least every 1.5 seconds. When the WDT overflow occurs, the MPU is momentarily reset as if RESETZ were pulled low for half of a crystal oscillator cycle. Thus, after 4100 cycles of the CK32 (32768Hz clock), the MPU program will be launched from address 00.

**An I/O RAM register status bit, *WD_OVF* (0x2002[2]), is set when WDT overflow occurs**. This bit is powered by the VBAT pin and can be read by the MPU to determine if the part is initializing after a WDT overflow event or after a power up. After reading this bit, MPU firmware must clear *WD_OVF*. The *WD_OVF* bit is also cleared by the RESETZ pin.

The watchdog timer also includes an oscillator check. If the crystal oscillator stops or slows down, *WD_OVF* is set and a system reset will be performed when the crystal oscillator resumes.

There is no internal digital state that deactivates the WDT. For debug purposes, however, the WDT can be disabled by tying the V1 pin to V3P3 (see Figure 11 and WD Disable Threshold [V1-V3P3A] in the Comparator Section of the Electrical Specifications). Of course, this also deactivates the power fault detection implemented with V1. Since there is no way in firmware to disable the crystal oscillator or the WDT, it is guaranteed that whatever state the MPU might find itself in, it will be reset to a known state upon watchdog timer overflow.

In normal operation, the WDT is reset by periodically writing a one to the *WDT_RST* bit. The watchdog timer is also reset when WAKE=0 and, during development, when a 0x14 command is received from the ICE port.

### Crystal Frequency Monitor

The hardware watchdog timer also includes an oscillator check. If the crystal oscillator stops or slows down, the I/O RAM register WD_OVF is set and a system reset will be performed when the crystal oscillator resumes.

### V1 Pin

The comparator at the V1 pin controls the state of the digital circuitry on the chip. When V1 < VBIAS (or when the RESTZ pin is pulled low), all digital activity in the chip stops while analog circuits including the oscillator and RTC module are still active. Additionally, when V1 < VBIAS, all I/O RAM bits are cleared. As long as V1 is greater than VBIAS, the internal 2.5V regulator will continue to provide power to the digital section.

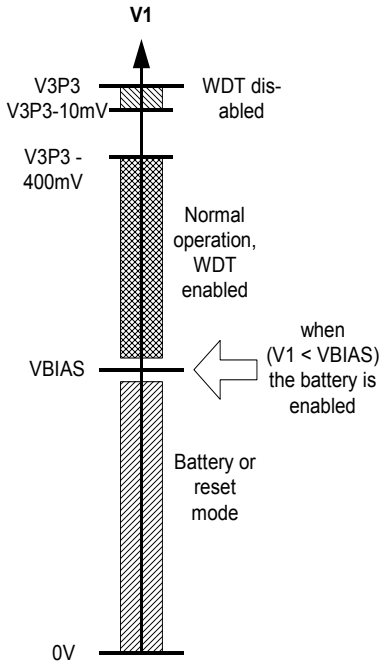



**Figure 11: Voltage Range for V1**

### I2C Interface (EEPROM)

A dedicated 2-pin serial interface implements an I2C driver that can be used to communicate with external EEPROM devices. The interface can be multiplexed onto the DIO pins DIO4 (SCK) and DIO5 (SDA) by setting the I/O RAM register *DIO_EEX* (0x2008[4]). The MPU communicates with the interface through two SFR registers: *EEDATA* (0x9E) and *EECTRL* (0x9F). If the MPU wishes to write a byte of data to EEPROM, it places the data in *EEDATA* and then writes the 'Transmit' code to *EECTRL*. The write to *EECTRL* initiates the transmit sequence. By observing the *BUSY* bit in *EECTRL* the MPU can determine when the transmit operation is finished (i.e. when the *BUSY* bit transitions from 1 to 0). INT5 is also asserted when *BUSY* falls. The MPU can then check the *RX_ACK* bit to see if the EEPROM acknowledged the transmission.

A byte is read by writing the 'Receive' command to *EECTRL* and waiting for *BUSY* to fall. Upon completion, the received data will appear in *EEDATA*.

The serial transmit and receive clock is 78kHz during each transmission, and SCL is held in a high state until the next transmission. The bits in *EECTRL* are shown in Table 57.

The EEPROM interface can also be operated by controlling the DIO4 and DIO5 pins directly. **However, controlling DIO4 and DIO5 directly is discouraged, because it may tie up the MPU to the point where it may become too busy to process interrupts**.

Note: Clock stretching and multi-master operation is not supported for the $I^2C$ interface.

<table>
<tr><th>Status Bit</th><th>Name</th><th>Read/ Write</th><th>Reset State</th><th>Polarity</th><th>Description</th></tr>
<tr><td>7</td><td>ERROR</td><td>R</td><td>0</td><td>Positive</td><td>1 when an illegal command is received.</td></tr>
<tr><td>6</td><td>BUSY</td><td>R</td><td>0</td><td>Positive</td><td>1 when serial data bus is busy.</td></tr>
<tr><td>5</td><td>RX_ACK</td><td>R</td><td>1</td><td>Negative</td><td>0 indicates that the EEPROM sent an ACK bit.</td></tr>
<tr><td>4</td><td>TX_ACK</td><td>R</td><td>1</td><td>Negative</td><td>0 indicates when an ACK bit has been sent to the EEPROM</td></tr>
<tr><td>3-0</td><td>CMD[3:0]</td><td>W</td><td>0</td><td>Positive, see CMD Table</td><td>
<table>
<tr><th>CMD</th><th>Operation</th></tr>
<tr><td>0</td><td>No-op. Applying the no-op command will stop the I2C clock (SCK, DIO4). Failure to issue the no-op command will keep the SCK signal toggling.</td></tr>
<tr><td>2</td><td>Receive a byte from EEPROM and send ACK.</td></tr>
<tr><td>3</td><td>Transmit a byte to EEPROM.</td></tr>
<tr><td>5</td><td>Issue a ‘STOP’ sequence.</td></tr>
<tr><td>6</td><td>Receive the last byte from EEPROM and do not send ACK.</td></tr>
<tr><td>9</td><td>Issue a ‘START’ sequence.</td></tr>
<tr><td>Others</td><td>No Operation, set the ERROR bit.</td></tr>
</table>
</td></tr>
</table>

**Table 57: *EECTRL* Status Bits**

### Internal Clocks and Clock Dividers

All internal clocks are based on the watch crystal frequency (CK32 = 32,768Hz) applied to the XIN and XOUT pins. The PLL multiplies this frequency by 150 to 4.9152MHz. This frequency is supplied to the ADC, the FIR filter (CKFIR), the clock test output pin (CKTEST), the CE DRAM and the clock generator. The clock generator provides two clocks, one for the MPU (CKMPU) and one for the CE (CKCE).

The MPU clock frequency is determined by the I/O RAM register *MPU_DIV* (0x2004[2:0]) and can be $CE*2^{-MPU\_DIV}$ Hz where *MPU_DIV* varies from 0 to 7 (*MPU_DIV* is 0 on power-up). This makes the MPU clock scalable from 4.9152MHz down to 38.4kHz.

The circuit also generates a 2x MPU clock for use by the emulator. This clock is not generated when the I/O RAM register *ECK_DIS* (0x2005[5]) is asserted by the MPU.

### Battery

The VBAT pin provides an input for an external battery that can be used to support the crystal oscillator, RTC, the *WD_OVF* bit and XRAM in the absence of the main power supply. If the battery is not used, the VBAT pin should be connected to V3P3.

### Internal Voltages (VBIAS, VBAT, V2P5)

The 71M6511 requires two supply voltages, V3P3A, for the analog section, and V3P3D, for the digital section. Both voltages can be tied together outside the chip. The internal supply voltage V2P5 is generated by a regulator from the 3.3V supplies.

The battery voltage, VBAT, is required when crystal oscillator, RTC and XRAM are required to keep operating while V3P3D is removed (battery mode). VBAT, usually supplied by an external battery, powers crystal oscillator, RTC and XRAM (and the *WD_OVF* bit).

VBIAS (1.5V) is generated internally and used for the V1 comparator and for the reference of the temperature sensor.

### Test Ports

**TMUXOUT Pin:** One out of 16 digital or 4 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is controlled with the I/O RAM register *TMUX* (0x2000[3:0]), as shown in Table 58.

| TMUX[3:0] | Mode | Function |
|---|---|---|
| 0 | analog | DGND |
| 1 | analog | IBIAS |
| 2 | analog | PLL_2.5V |
| 3 | analog | VBIAS |
| 4 | digital | RTM (Real time output from CE) |
| 5 | digital | WDTR_EN (Comparator 1 Output AND V1LT3) |
| 6 | digital | reserved |
| 7 | digital | reserved |
| 8 | digital | RXD (from Optical interface) |
| 9 | digital | MUX_SYNC |
| A | digital | CK_10M |
| B | digital | CK_MPU |
| C | -- | reserved for production test |
| D | digital | RTCLK |
| E | digital | CE_BUSY |
| F | digital | XFER_BUSY |

**Table 58: *TMUX[3:0]* Selections**

**Emulator Port:** The emulator port, consisting of the pins E_RST, E_TCLK and E_RXTX provides control of the MPU through an external in-circuit emulator. The emulator port is compatible with the ADM51 emulators manufactured by Signum Systems.

The signals of the emulator port have weak pull-ups. Adding 1kΩ pull-up resistors on the PCB is recommended.

**Real-Time Monitor:** The RTM output of the CE is available as one of the digital multiplexer options. RTM data is read from the CE DRAM locations specified by I/O RAM registers *RTM0*, *RTM1*, *RTM2*, and *RTM3* after the rise of MUX_SYNC. The RTM can be enabled and disabled with I/O RAM register *RTM_EN*. The RTM output is clocked by CKTEST. Each RTM word is clocked out in 35 cycles and contains a leading flag bit. Figure 13 in the System Timing Section illustrates the RTM output format. RTM is low when not in use.

**SSI Interface:** A high-speed serial interface with handshake capability is available to send a contiguous block of CE data to an external data logger or DSP. The block of data, configurable as to location and size, is sent starting 1 cycle of 32kHz before each CE code pass begins. If the block of data is big enough that transmission has not completed when the code pass begins, it will complete during the CE code pass with no timing impact to the CE or the serial data. In this case, care must be taken that the transmitted data is not modified unexpectedly by the CE. The SSI interface is enabled by the *SSI_EN* bit and consists of SCLK, SSDATA, and SFR as outputs and, optionally, SRDY as input. The interface is compatible with 16bit and 32bit processors. The operation of each pin is as follows:

SCLK is the serial clock. The clock can be 5MHz or 10MHz, as specified by the *SSI_10M* bit. The *SSI_CKGATE* bit controls whether SCLK runs continuously or is gated off when no SSI activity is occurring. If SCLK is gated, it will begin 3 cycles before SFR rises and will persist 3 cycles after the last data bit is output.

The pins used for the SSI are multiplexed with the LCD segment outputs, as shown in Table 59. **Thus, the LCD should be disabled when the SSI is in use.**

| SSI Signal | LCD Segment Output Pin |
|---|---|
| SCLK | SEG3 |
| SSDATA | SEG4 |
| SFR | SEG5 |
| SRDY | SEG6 |

**Table 59: SSI Pin Assignment**

SRDY is an optional handshake input that indicates that the DSP or data-logging device is ready to receive data. SRDY must be high to enable SFR to rise and initiate the transfer of the next field. It is expected that SRDY changes state on the rising edges of SCLK. If SRDY is not high when the SSI port is ready to transmit the next field, transmission will be delayed until it is. SRDY is ignored except at the beginning of a field transmission. If SRDY is not enabled (by *SSI_RDYEN*), the SSI port will behave as if SRDY is always one.

SSDATA is the serial output data. SSDATA changes on the rising edge of SCLK and outputs the contents of a block of CE RAM words starting with address *SSI_STRT* and ending with *SSI_END*. The words are output MSB first.

The field size is set with the *SSI_FSIZE* register: 0 entire data block, 1-8 bit fields, 2-16 bit fields, 3-32 bit fields. The polarity of the SFR pulse can be inverted with *SSI_FPOL*. If SRDY does not delay it, the first SFR pulse in a frame will rise on the third SCLK after MUX_SYNC (fourth SCLK if 10MHz). MUX_SYNC can be used to synchronize the fields arriving at the data logger or DSP.

## FUNCTIONAL DESCRIPTION

### Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

Assuming phase angles are constant, the following formulae apply:

- P = Real Energy [Wh] = V * A * cos φ* t
- Q = Reactive Energy [VARh] = V * A * sin φ * t
- S = Apparent Energy [VAh] = $\sqrt{P^2 + Q^2}$

For a practical meter, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity meter IC such as the 71M6511/6511H functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling will yield an accurate quantity for the momentary energy. Summing up the momentary energy quantities over time will result in accumulated energy.

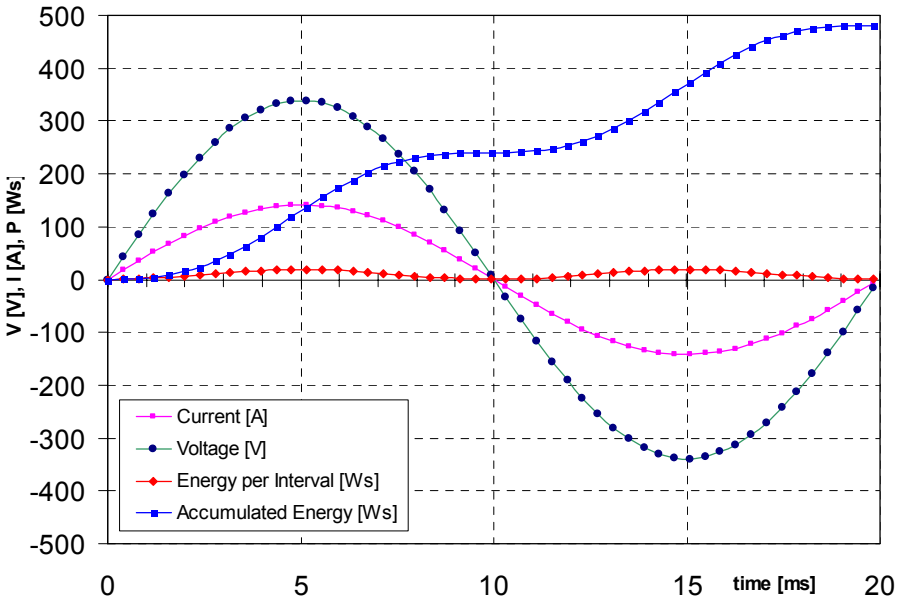



**Figure 12: Voltage. Current, Momentary and Accumulated Energy**

Figure 12 shows the shapes of V(t), I(t), the momentary and the accumulated energy, resulting from 50 samples of the voltage and current signals over a period of 20ms. The application of 240VAC and 100A results in an accumulation of 480Ws over the 20ms period, as indicated by the Accumulated Power curve.

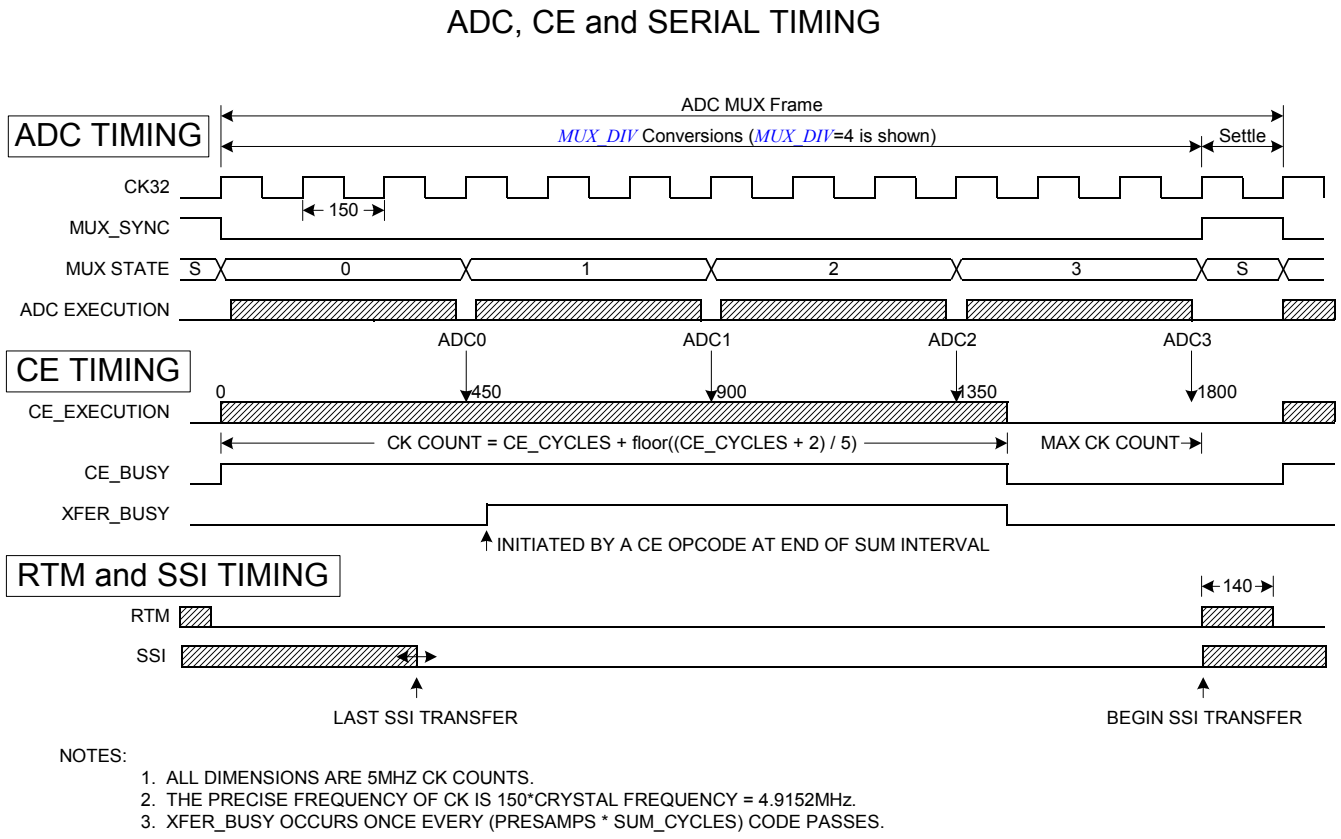
The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

### System Timing Summary

Figure 13 summarizes the timing relationships between the input MUX states, the CE_BUSY signal, and the two serial output streams. In this example, *MUX_DIV* = 1 (four mux states) and *FIR_LEN* = 1 (3 CK32 cycles). Since FIR filter conversions require two or three CK32 cycles, the duration of each MUX cycle is 1 + 2 * states defined by *MUX_DIV* if *FIR_LEN* = 0, and 1 + 3 * states defined by *MUX_DIV* if *FIR_LEN* = 1. Followed by the conversions is a single CK32 cycle.

Each CE program pass begins when MUX_SYNC falls. Depending on the length of the CE program, it may continue running until the end of the ADC5 conversion. CE opcodes are constructed to ensure that all CE code passes consume exactly the same number of cycles. The result of each ADC conversion is inserted into the CE DRAM when the conversion is complete. The CE code is designed to tolerate sudden changes in ADC data. The exact CK count when each ADC value is loaded into DRAM is shown in Figure 13.

Figure 13 also shows that the two serial data streams, RTM and SSI, begin transmitting at the beginning of MUX_SYNC. RTM, consisting of 140 CK cycles, will always finish before the next code pass starts. The SSI port begins transmitting at the same time as RTM, but may significantly overrun the next code pass if a large block of data is required. Neither the CE nor the SSI port will be affected by this overlap.




NOTES:
1. ALL DIMENSIONS ARE 5MHZ CK COUNTS.
2. THE PRECISE FREQUENCY OF CK IS 150*CRYSTAL FREQUENCY = 4.9152MHz.
3. XFER_BUSY OCCURS ONCE EVERY (PRESAMPS * SUM_CYCLES) CODE PASSES.

**Figure 13: Timing Relationship between ADC MUX, CE, and Serial Transfers**

Figure 14, Figure 15, and Figure 16 show the RTM and SSI timing, respectively.

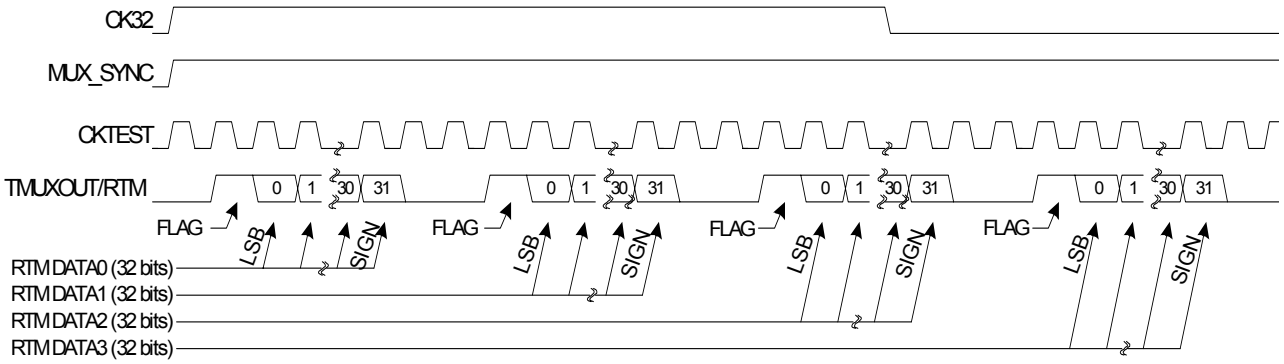



**Figure 14: RTM Output Format**

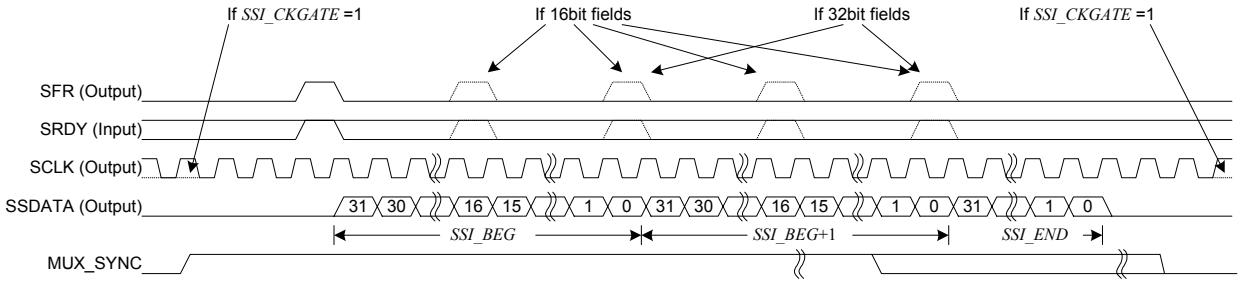



**Figure 15: SSI Timing, (*SSI_FPOL* = *SSI_RDYPOL* = 0)**

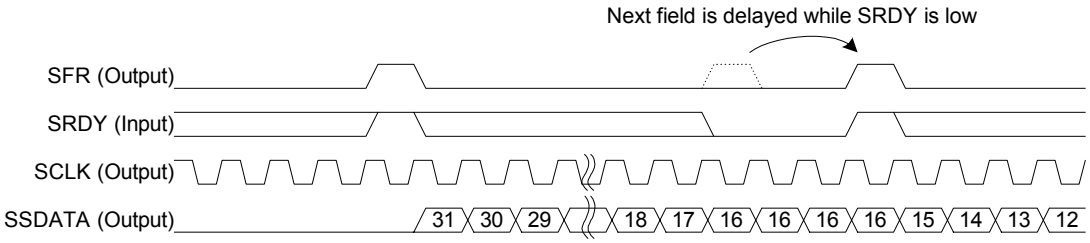



**Figure 16: SSI Timing, 16-bit Field Example (External Device Delays SRDY)**

SFR is the framing pulse. Although CE words are always 32 bits, the SSI interface will frame the entire data block as a single field, as multiple 16-bit fields, or as multiple 32-bit fields. The SFR pulse is one SCLK clock cycle wide, changes state on the rising edge of SCLK and precedes the first bit of each field.

### Data Flow

The data flow between CE and MPU is shown in Figure 17. In a typical application, the 32-bit compute engine (CE) sequentially processes the samples from the voltage inputs on pins IA, VA, and IB, performing calculations to measure active power (Wh), reactive power (VARh), $A^2h$, and $V^2h$ for four-quadrant metering. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

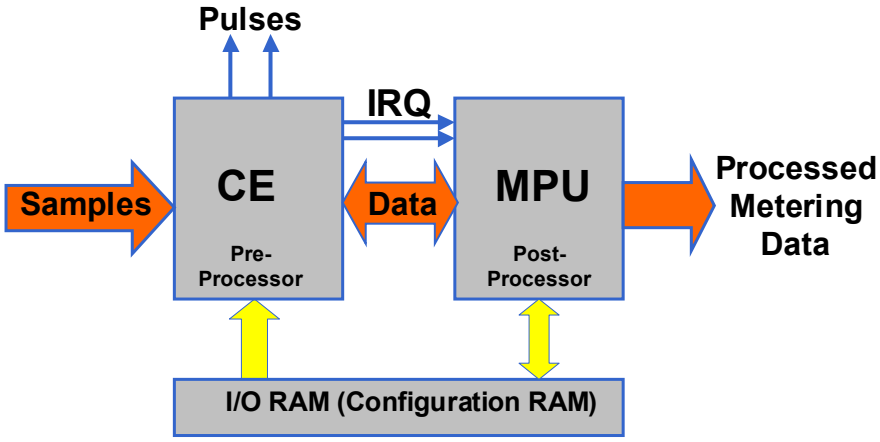



**Figure 17: MPU/CE Data Flow**

### CE/MPU Communication

Figure 18 shows the functional relationship between CE and MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and by registers in the CE DRAM. The CE outputs two interrupt signals to the MPU: CE_BUSY and XFER_BUSY, which are connected to the MPU interrupt service inputs as external interrupts. CE_BUSY indicates that the CE is actively processing data. This signal will occur once every multiplexer cycle. XFER_BUSY indicates that the CE is updating data to the output region of the CE RAM. This will occur whenever the CE has finished generating a sum by completing an accumulation interval determined by *SUM_CYCLES* * *PRE_SAMPS* samples. Interrupts to the MPU occur on the falling edges of the XFER_BUSY and CE_BUSY signals.

Figure 19 shows the sequence of events between CE and MPU upon reset or power-up. In a typical application, the sequence of events is as follows:

1) Upon power-up, the MPU initializes the hardware, including disabling the CE
2) The MPU loads the code for the CE into the CE PRAM
3) The MPU loads CE data into the CE DRAM.
4) The MPU starts the CE by setting the *CE_EN* bit in the I/O RAM.
5) The CE then repetitively executes its code, generating results and storing them in the CE DRAM

It is important to note that the length of the accumulation interval, as determined by $N_{ACC}$, the product of *SUM_CYCLES* and *PRE_SAMPS* is not an exact multiple of 1000ms. For example, if *SUM_CYCLES* = 60, and *PRE_SAMPS* = 00 (42), the resulting accumulation interval is:

$$\tau = \frac{N_{ACC}}{f_S} = \frac{60 \cdot 42}{\frac{32768Hz}{13}} = \frac{2520}{2520.62Hz} = 999.75ms$$

This means that accurate time measurements should be based on the RTC, not the accumulation interval.

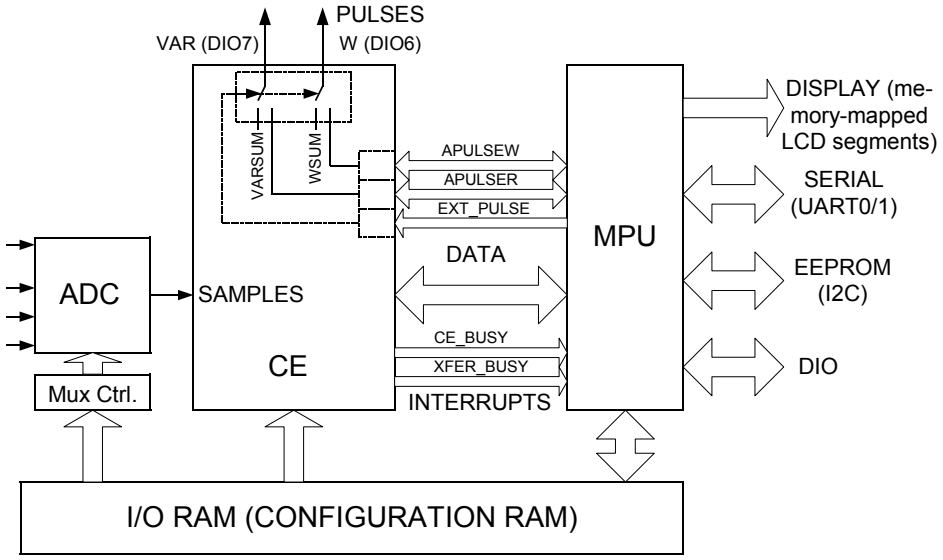



**Figure 18: MPU/CE Communication (Functional)**

The MPU will wait for the CE to signal that fresh data is ready (the XFER interrupt). It will read the data and perform additional processing such as energy accumulation.

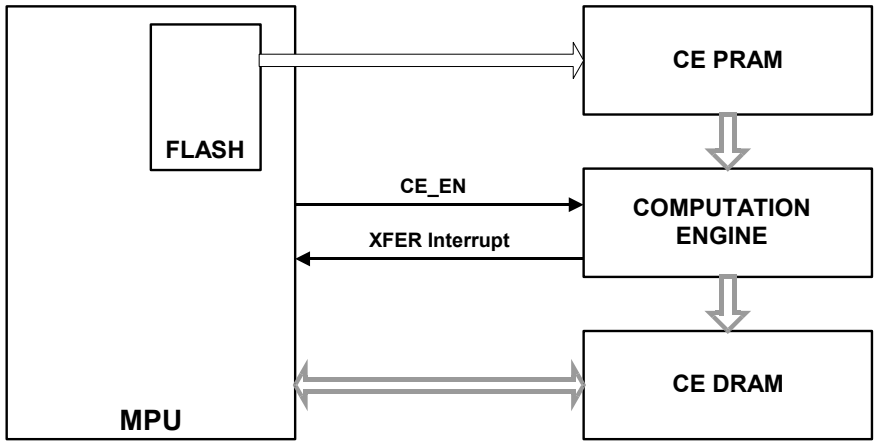



**Figure 19: MPU/CE Communication (Processing Sequence)**

### Fault, Reset, Power-Up

**Reset Mode:** When the RESETZ pin is pulled low or when V1 < VBIAS, all digital activity in the chip stops while analog circuits are still active. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are cleared. As long as V1, the input voltage at the power fault block, is greater than VBIAS, the internal 2.5V regulator will continue to provide power to the digital section.

Once initiated, the reset mode will persist until the reset timer times out, signified by WAKE rising. This will occur in 4100 cycles of the real time clock after RESETZ goes high, at which time the MPU will begin executing its preboot and boot sequences from address 00. See the security section for more description of preboot and boot.

**Power-Up:** After power-up, the 71M6511/6511H is in reset as long as V1 < VBIAS. As soon as V1 exceeds VBIAS, the reset timer is started which takes the MPU out of reset after 4100 oscillator cycles (see Figure 20). The MPU then initiates its pre-boot phase lasting 32 cycles. The supply current will be low but not zero during power-up. It will increase, once V1 exceeds VBIAS and will increase to the nominal value once the preboot phase starts. The supply current may then be reduced under firmware control, following the steps specified in Battery Operation and Power Save Modes.

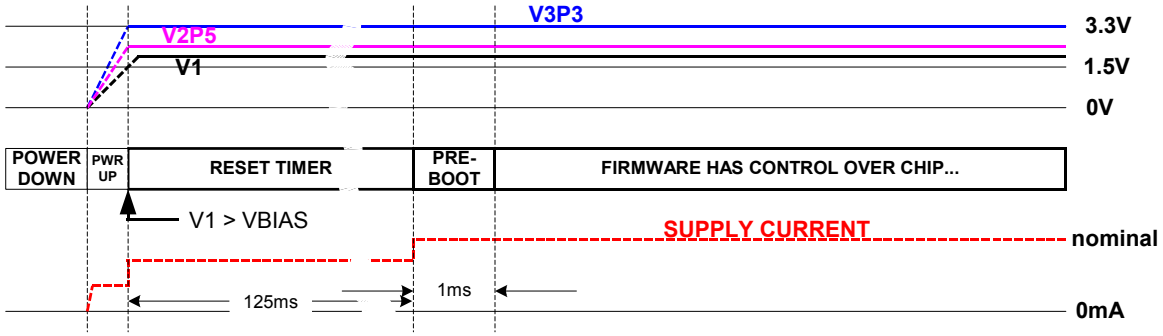



**Figure 20: Timing Diagram for Voltages, Current and Operation Modes after Power-Up**

## Battery Operation

When V1 is lower than VBIAS, the external battery will power the following parts of the 71M6511/6511H:

- RTC
- Crystal oscillator circuitry
- MPU XRAM
- *WD_OVF* bit

## Power Save Modes

In normal mode of operation, running on 3.3V supply, various resources of the 71M6511/6511H may be shut down by the MPU firmware in order to reduce power consumption while other essential resources such as UARTs may remain active. Table 60 outlines these resources and their typical current consumption (based on initial condition *MPU_DIV* = 0).

| Power Saving Measure | Software Control | Typical Savings |
|---|---|---|
| Disable the CE | *CE_EN* = 0 | 0.16mA |
| Disable the ADC | *ADC_DIS* = 1 | 1.8mA |
| Disable clock test output CKTEST | *CKOUTDIS* = 1 | 0.6mA |
| Disable emulator clock | *ECK_DIS* = 1 *) | 0.1mA |
| Set flash read pulse timing to 33 ns | *FLASH66Z* =1 | 0.04mA |
| Disable the LCD voltage boost circuitry | *LCD_BSTEN* = 0 | 0.9mA |
| Disable RTM outputs | *RTM_EN* = 0 | 0.01mA |
| Increase the clock divider for the MPU | *MPU_DIV* = X | 0.4mA/MHz |

*) This bit is to be used with caution! Inadvertently setting this bit will inhibit access to the part with the ICE interface and thus preclude flash erase and programming operations.

**Table 60: Power Saving Measures**

### Temperature Compensation

**Internal Compensation:** The internal voltage reference is calibrated during device manufacture. Trim data is stored in on-chip fuses.

For the 71M6511, the temperature coefficients TC1 and TC2 are given as constants that represent typical component behavior.

For the 71M6511H, the temperature characteristics of the chip are measured during production and then stored in the fuse registers *TRIMBGA, TRIMBGB* and *TRIMM[2:0]*. TC1 and TC2 can be derived from the fuses by using the relations given in the Electrical Specifications section. TC1 and TC2 can be further processed to generate the coefficients *PPMC* and *PPMC2*.

*TRIMM[2:0], TRIMBGA* and *TRIMBGB* are read by first writing either 4, 5 or 6 to *TRIMSEL* (0x20FD) and then reading the value of *TRIM* (0x20FF).

When the *EXT_TEMP* register in CE DRAM (address 0x38) is set to 0, the CE automatically compensates for temperature errors by controlling the *GAIN_ADJ* register (address 0x2E) based on the *PPMC*, *PPMC2*, and *TEMP_X* register values. In the case of internal compensation, *GAIN_ADJ* is an output of the CE.

**External Compensation**: Rather than internally compensating for the temperature variation, the bandgap temperature is provided to the embedded MPU, which then may digitally compensate the power outputs. This permits a system-wide temperature correction over the entire system rather than local to the chip. The incorporated thermal coefficients may include the current sensors, the voltage sensors, and other influences. Since the band gap is chopper stabilized via the *CHOP_EN* bits, the most significant long-term drift mechanism in the voltage reference is removed.

When the *EXT_TEMP* register in CE DRAM is set to 15, the CE ignores the *PPMC*, *PPMC2*, and *TEMP_X* register values and applies the gain supplied by the MPU in *GAIN_ADJ*. External compensation enables the MPU to control the CE gain based on any variable, and when *EXT_TEMP* = 15, GAIN_ADJ is an input to the CE.

### Chopping Circuitry

As explained in the hardware section, the bits of the I/O RAM register *CHOP_ENA[1:0]* have to be toggled in between multiplexer cycles to achieve the desired elimination of DC offset.

The amplifier within the reference is auto-zeroed by means of an internal signal that is controlled by the *CHOP_EN* bits. When this signal is HIGH, the connection of the amplifier inputs is reversed. This preserves the overall polarity of the amplifier gain but inverts the input offset. By alternately reversing the connection, the offset of the amplifier is averaged to zero. The two bits of the *CHOP_EN* register have the function specified in Table 61.

| CHOP_EN[1] | CHOP_EN[0] | Function |
|---|---|---|
| 0 | 0 | Toggle chop signal |
| 0 | 1 | Reference connection positive |
| 1 | 0 | Reference connection reversed |
| 1 | 1 | Toggle chop signal |

**Table 61: *CHOP_EN* Bits**

For automatic chopping, the *CHOP_EN* bits are set to either 00 or 11. In this mode, the polarity of the signals feeding the reference amplifier will be automatically toggled for each multiplexer cycle as shown in Figure 21. With an even number of multiplexer cycles in each accumulation interval, the number of cycles with positive reference connection will equal the number of cycles with reversed connection, and the offset for each sampled signal will be averaged to zero. This sequence is acceptable when only the primary signals (meter voltage, meter current) are of interest.

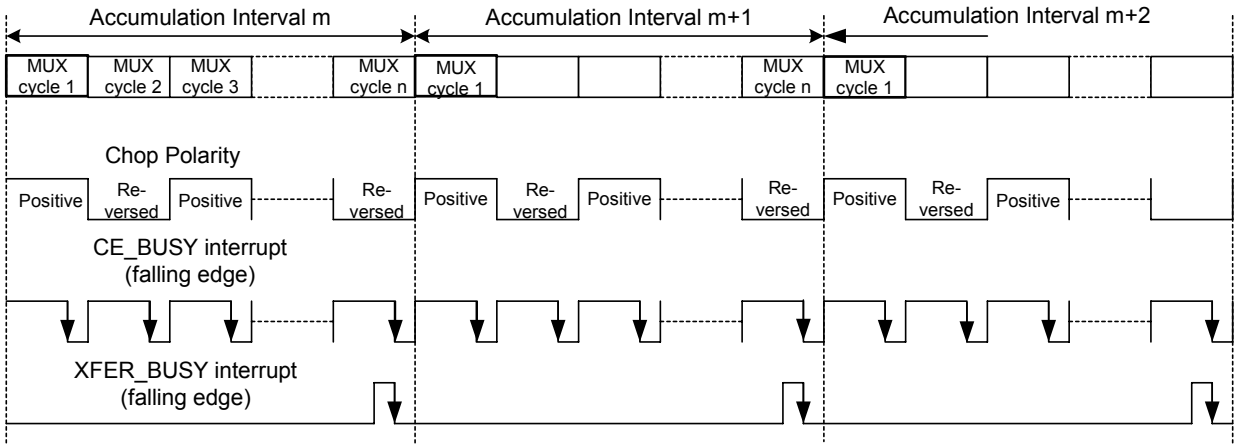



**Figure 21: Chop Polarity w/ Automatic Chopping**

If temperature compensation or accurate reading of the die temperature is required, alternate multiplexer cycles have to be inserted in between the regular cycles. This is done under MPU firmware control by asserting the *MUX_ALT* bit whenever necessary. Since die temperature usually changes very slowly, alternate multiplexer cycles have to be inserted very infrequently. Usually, an alternate multiplexer cycle is inserted once for every accumulation period, i.e. after each XFER_BUSY interrupt. This sequence is shown in Figure 22.

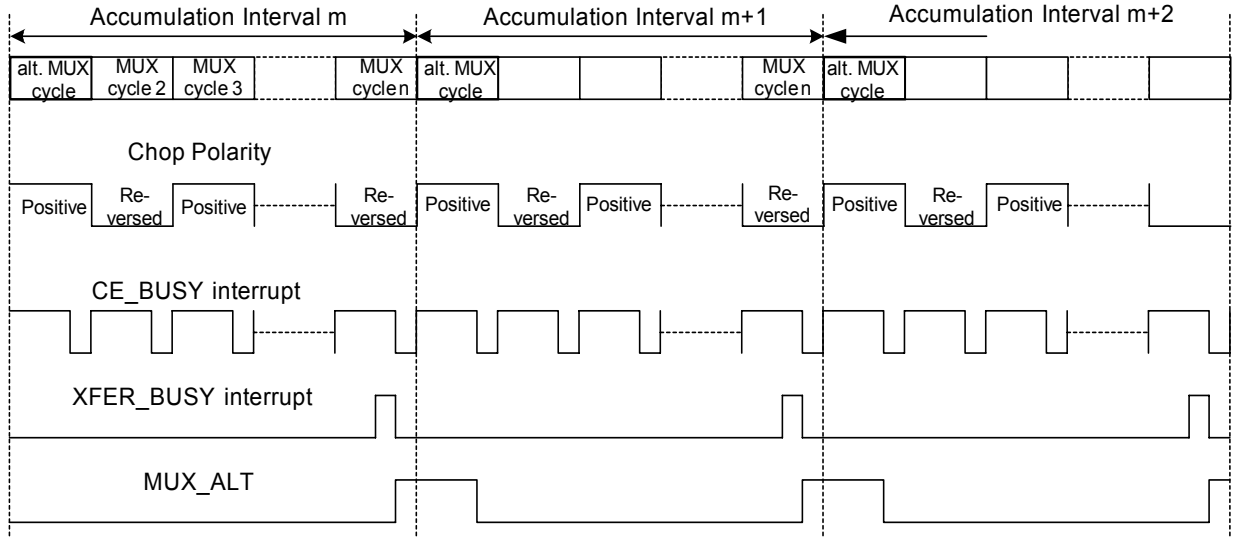



**Figure 22: Sequence with Alternate Multiplexer Cycles**

This sequence has the disadvantage that the alternate multiplexer cycle is always operated with positive connection. Consequently, DC offset will appear on the temperature measurement, which will decrease the accuracy of this measurement and thus cause temperature reading and compensation to be less accurate.

The sequence shown in Figure 23 uses the *CHOP_EN* bits to control the chopper polarity after each XFER_BUSY interrupt. *CHOP_EN* is controlled to alternate between 10 (positive) and 01 (reversed) for the first multiplexer cycle following each

XFER_BUSY interrupt. After these first two cycles, *CHOP_EN* returns to 11 (automatic toggle). The value of *CHOP_EN*, when set after the XFER_BUSY interrupt, is in force for the entire following multiplexer cycle.

When using this sequence, the alternate multiplexer cycle is toggled between positive and reversed connection resulting in accurate temperature measurement.

An example for proper application of the *CHOP_EN* bits can be found in the Demo Code shipped with the 6511 and 6511 Demo Kits. Firmware implementations should closely follow this example.

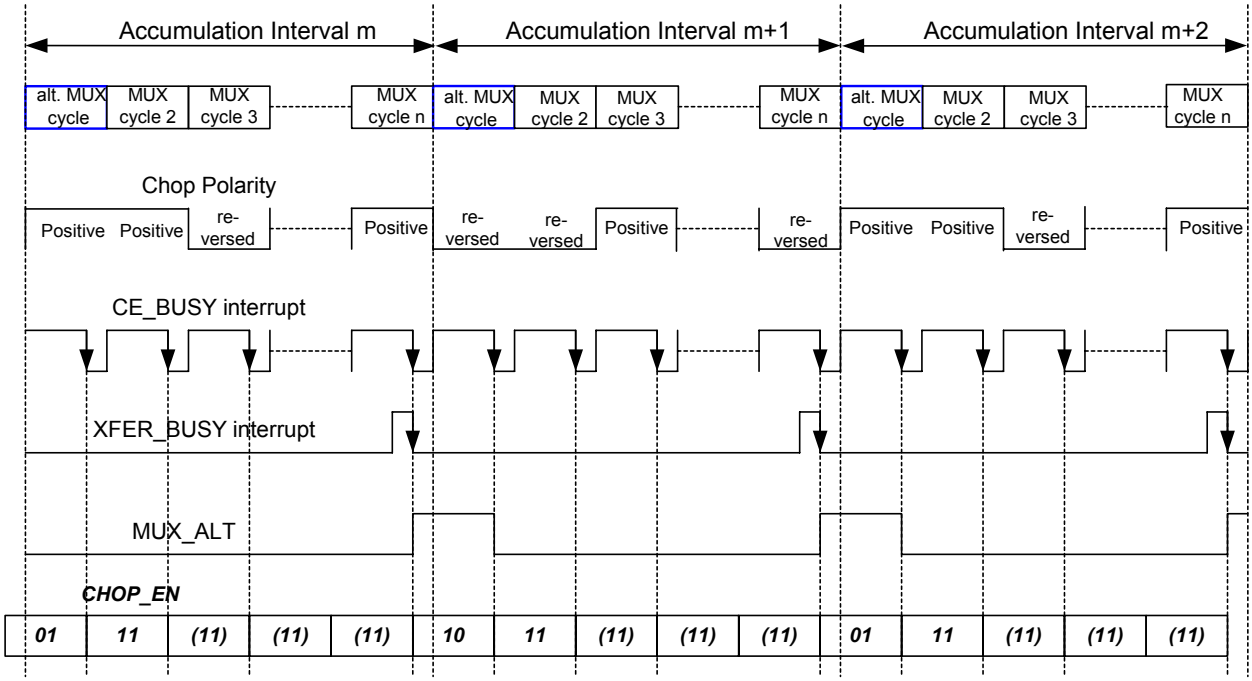



**Figure 23: Sequence with Alternate Multiplexer Cycles and Controlled Chopping**

### Internal/External Pulse Generation and Pulse Counting

The CE is the source for pulses. It can generate pulses directly based on the voltage and current inputs and the configured pulse generation parameters. This is called “internal pulse generation”, and applies when the CE RAM register *EXT_PULSE* (address 0x37) equals 0. Alternatively, the CE can be configured to generate pulses based on registers that are controlled by the MPU (“external pulse generation”), i.e. when the register *EXT_PULSE* equals 15. In the case of external pulse generation, the MPU writes values to the CE registers *APULSEW* (0x26) and *APULSER* (0x27).

The pulse rate, usually inversely expressed as “Kh” (and measured in Wh per pulse), is determined by the CE RAM registers *WRATE*, *PULSE_SLOW*, *PULSE_FAST*, *In_8*, as well as by the sensor scaling *VMAX* and *IMAX* per the equation:

$$Kh = \frac{VMAX \cdot IMAX \cdot 47.1132}{In\_8 \cdot WRATE \cdot N_{ACC} \cdot X}[Wh/\,pulse]$$

where

*In_8* is the gain factor (1 or 8) controlled by the CE variable *In_SHUNT*,
X is the pulse gain factor controlled by the CE variables *PULSE_SLOW* and *PULSE_FAST*
$N_{ACC}$ is the accumulation count (*PRE_SAMPS* * *SUM_CYCLES*)

### Program Security

When enabled, the security feature limits the ICE to global flash erase operations only. All other ICE operations are blocked. This guarantees the security of the user's MPU and CE program code. Security is enabled by MPU code that is executed in a 32 cycle preboot interval before the primary boot sequence begins. Once security is enabled, the only way to disable it is to perform a global erase of the flash memory, followed by a chip reset. Global flash erase also clears the CE PRAM.

The first 32 cycles of the MPU boot code are called the preboot phase because during this phase the ICE is inhibited. A read-only status bit, *PREBOOT* (SFR 0xB2[7]), identifies these cycles to the MPU. Upon completion of the preboot sequence, the ICE can be enabled and is permitted to take control of the MPU.

*SECURE* (SFR 0xB2[6]), the security enable bit, is reset whenever the MPU is reset. Hardware associated with the bit permits only ones to be written to it. Thus, preboot code may set *SECURE* to enable the security feature but may not reset it. Once *SECURE* is set, the preboot code is protected and no external read of program code is possible.

Specifically, when *SECURE* is set:

- The ICE is limited to bulk flash erase only.
- Page zero of flash memory, the preferred location for the user's preboot code, may not be page-erased by either MPU or ICE. Page zero may only be erased with global flash erase. Note that global flash erase erases CE program RAM whether *SECURE* is set or not.
- Writes to page zero, whether by MPU or ICE, are inhibited.

**The *SECURE* bit is to be used with caution!** Inadvertently setting this bit will inhibit access to the part via the ICE interface, if no mechanism for actively resetting the part between reset and erase operations is provided (see ICE Interface description).

Additionally, by setting the I/O RAM register *ECK_DIS* to 1, the emulator clock is disabled, inhibiting access to the program with the emulator. **See the cautionary note in the I/O RAM Register description!**

## FIRMWARE INTERFACE

### I/O RAM MAP – In Numerical Order

'Not Used' bits are blacked out and contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed.

| Name | Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Configuration:** | | | | | | | | | |
| CE0 | 2000 | *EQU[2:0]* | | | *CE_EN* | *TMUX[3:0]* | | | |
| CE1 | 2001 | *PRE_SAMPS[1:0]* | | *SUM_CYCLES[5:0]* | | | | | |
| CE2 | 2002 | *MUX_DIV[1:0]* | | *CHOP_EN[1:0]* | | *RTM_EN* | *WD_OVF* | *EX_RTC* | *EX_XFR* |
| COMP0 | 2003 | | | | RESERVED | | RESERVED | | *COMP_STAT[0]* |
| CONFIG0 | 2004 | *VREF_CAL* | | RESERVED | *CKOUT_DIS* | *VREF_DIS* | *MPU_DIV* | | |
| CONFIG1 | 2005 | RESERVED | | *ECK_DIS* | *FIR_LEN* | *ADC_DIS* | *MUX_ALT* | *FLASH66Z* | *MUX_E* |
| VERSION | 2006 | *VERSION[7:0]* | | | | | | | |
| **Digital I/O:** | | | | | | | | | |
| DIO0 | 2008 | | | *OPT_TXDIS* | *DIO_EEX* | *DIO_PW* | *DIO_PV* | | |
| DIO1 | 2009 | | RESERVED | | | | RESERVED | | |
| DIO2 | 200A | | RESERVED | | | | RESERVED | | |
| DIO3 | 200B | | *DIO_R5[2:0]* | | | | *DIO_R4[2:0]* | | |
| DIO4 | 200C | | *DIO_R7[2:0]* | | | | *DIO_R6[2:0]* | | |
| DIO5 | 200D | | *DIO_R9[2:0]* | | | | *DIO_R8[2:0]* | | |
| DIO6 | 200E | | *DIO_R11[2:0]* | | | | *DIO_R10[2:0]* | | |
| **Real Time Clock:** | | | | | | | | | |
| RTC0 | 2015 | | | *RTC_SEC[5:0]* | | | | | |
| RTC1 | 2016 | | | *RTC_MIN[5:0]* | | | | | |
| RTC2 | 2017 | | | | *RTC_HR[4:0]* | | | | |
| RTC3 | 2018 | | | | | | *RTC_DAY[2:0]* | | |
| RTC4 | 2019 | | | | *RTC_DATE[4:0]* | | | | |
| RTC5 | 201A | | | | | *RTC_MO[3:0]* | | | |
| RTC6 | 201B | *RTC_YR[7:0]* | | | | | | | |
| RTC7 | 201C | | | | | | | *RTC_DEC_SEC* | *RTC_INC_SEC* |
| **LCD Display Interface:** | | | | | | | | | |
| LCDX | 2020 | *LCD_BSTEN* | | | *LCD_NUM[4:0]* | | | | |
| LCDY | 2021 | | | *LCD_EN* | *LCD_MODE[2:0]* | | | *LCD_CLK[1:0]* | |
| LCDZ | 2022 | | | | *LCD_FS[4:0]* | | | | |
| LCD0 | 2030 | | | | | *LCD_SEG0[3:0]* | | | |
| LCD1 | 2031 | | | | | *LCD_SEG1[3:0]* | | | |
| … | … | | | | | … | | | |
| LCD19 | 2043 | | | | | *LCD_SEG19[3:0]* | | | |
| LCD20 | 2044 | | | | | RESERVED | | | |
| … | … | | | | | … | | | |
| LCD23 | 2047 | | | | | RESERVED | | | |
| LCD24 | 2048 | | | | | *LCD_SEG24[3:0]* | | | |
| … | … | | | | | … | | | |
| LCD31 | 204F | | | | | *LCD_SEG31[3:0]* | | | |
| LCD32 | 2050 | | | | | *LCD_SEG32[3:0]* | | | |
| LCD33 | 2051 | | | | | *LCD_SEG33[3:0]* | | | |
| LCD34 | 2052 | | | | | *LCD_SEG34[3:0]* | | | |
| LCD35 | 2053 | | | | | *LCD_SEG35[3:0]* | | | |
| LCD36 | 2054 | | | | | *LCD_SEG36[3:0]* | | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| LCD37 | 2055 | | | | | *LCD_SEG37[3:0]* | | |
| LCD38 | 2056 | | | | | RESERVED | | |
| LCD39 | 2057 | | | | | RESERVED | | |
| LCD40 | 2058 | | | | | RESERVED | | |
| LCD41 | 2059 | | | | | RESERVED | | |
| **RTM Probes:** | | | | | | | | |
| RTM0 | 2060 | *RTM0[7:0]* | | | | | | |
| RTM1 | 2061 | *RTM1[7:0]* | | | | | | |
| RTM2 | 2062 | *RTM2[7:0]* | | | | | | |
| RTM3 | 2063 | *RTM3[7:0]* | | | | | | |
| **Synchronous Serial Interface:** | | | | | | | | |
| SSI | 2070 | *SSI_EN* | *SSI_10M* | *SSI_CKGATE* | *SSI_FSIZE[1:0]* | | *SSI_FPOL* | *SSI_RDYEN* | *SSI_RDYPOL* |
| SSI_BEG | 2071 | *SSI_BEG[7:0]* | | | | | | |
| SSI_END | 2072 | *SSI_END[7:0]* | | | | | | |
| **Fuse Selection Registers:** | | | | | | | | |
| TRIMSEL | 20FD | *TRIMSEL[7:0]* | | | | | | |
| TRIM | 20FF | *TRIM[7:0]* | | | | | | |

### SFR MAP (SFRs Specific to TERIDIAN 80515) – In Numerical Order

'Not Used' bits are blacked out and contain no memory and are read by the MPU as zero. *RESERVED* bits are in use and should not be changed. This table lists only the SFR registers that are not generic 8051 SFR registers.

| Name | SFR Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| **Digital I/O:** | | | | | | | | | |
| *P0* | 80 | *DIO_0[7:4]* (Port 0) | | | | RESERVED | | | |
| *DIR0* | A2 | *DIO_DIR0[7:4]* | | | | 1111 | | | |
| *P1* | 90 | *DIO_1[7:6]* (Port 1) | | | | *DIO_1[3:0]* (Port 1) | | | |
| *DIR1* | 91 | *DIO_DIR1[7:6]* | | | | *DIO_DIR1[3:0]* | | | |
| *P2* | A0 | | | RESERVED | | | | *DIO_2[1:0]* (Port 2) | |
| *DIR2* | A1 | | | 1111 | | | | *DIO_DIR2[1:0]* | |
| **Interrupts and WD Timer:** | | | | | | | | | |
| *INTBITS* | F8 | | *INT6* | *INT5* | *INT4* | *INT3* | *INT2* | *INT1* | *INT0* |
| *WDI* | E8 | *WD_RST* | | | | | | *IE_RTC* | *IE_XFER* |
| **Flash:** | | | | | | | | | |
| *ERASE* | 94 | *FLSH_ERASE[7:0]* | | | | | | | |
| *FLSHCTL* | B2 | *PREBOOT* | *SECURE* | | | | | *FLSH_MEEN* | *FLSH_PWE* |
| *PGADR* | B7 | *FLSH_PGADR[6:0]* | | | | | | | |
| **Serial EEPROM:** | | | | | | | | | |
| *EEDATA* | 9E | *EEDATA[7:0]* | | | | | | | |
| *EECTRL* | 9F | *EECTRL[7:0]* | | | | | | | |

### I/O RAM (Configuration RAM) – Alphabetical Order

Many functions of the chip can be controlled via the I/O RAM (Configuration RAM). The CE will also take some of its parameters from the I/O RAM.

Bits with a W (write) direction are written by the MPU into I/O RAM. Typically, they are initially stored in flash memory and copied to the I/O RAM by the MPU. Some of the more frequently programmed bits are mapped to the MPU SFR memory space. The remaining bits are mapped to 2xxx. Bits with R (read) direction can only be read by the MPU. **On power up, all bits are cleared to zero unless otherwise stated.** Generic SFR registers are not listed.

<table>
<tr><th>Name</th><th>Location [Bit(s)]</th><th>Dir</th><th>Description</th></tr>
<tr><td>ADC_DIS</td><td>2005[3]</td><td>R/W</td><td>Disables ADC and removes bias current</td></tr>
<tr><td>CE_EN</td><td>2000[4]</td><td>R/W</td><td>CE enable.</td></tr>
<tr><td>CHOP_EN[1:0]</td><td>2002[5:4]</td><td>R/W</td><td>Chop enable for the reference band gap circuit.<br>00: enabled 01: disabled 10: disabled 11: enabled</td></tr>
<tr><td>RESERVED</td><td>2004[5]</td><td>R/W</td><td>Must be 0.</td></tr>
<tr><td>CKOUT_DIS</td><td>2004[4]</td><td>R/W</td><td>CKOUT Disable. When zero, CKTEST is an active output.</td></tr>
<tr><td>RESERVED</td><td>2003[4:3]</td><td>R/W</td><td>Must be 0.</td></tr>
<tr><td>RESERVED</td><td>2003[2:0]</td><td>R</td><td>Reserved</td></tr>
<tr><td>DIO_R4[2:0]<br>DIO_R5[2:0]<br>DIO_R6[2:0]<br>DIO_R7[2:0]<br>DIO_R8[2:0]<br>DIO_R9[2:0]<br>DIO_R10[2:0]<br>DIO_R11[2:0]</td><td>200B[2:0]<br>200B[6:4]<br>200C[2:0]<br>200C[6:4]<br>200D[2:0]<br>200D[6:4]<br>200E[2:0]<br>200E[6:4]</td><td>R/W<br>R/W<br>R/W<br>R/W<br>R/W<br>R/W<br>R/W<br>R/W</td><td>Connects dedicated I/O pins 4 to 11 to selectable internal resources. If more than one input is connected to the same resource, the ‘Multiple’ column below specifies how they are combined. See Software User’s Guide for details).
<table>
<tr><th>DIO_GP</th><th>Resource</th><th>Multiple</th></tr>
<tr><td>0</td><td>NONE</td><td>--</td></tr>
<tr><td>1</td><td>Reserved</td><td>OR</td></tr>
<tr><td>2</td><td>T0 (counter0 clock)</td><td>OR</td></tr>
<tr><td>3</td><td>T1 (counter1 clock)</td><td>OR</td></tr>
<tr><td>4</td><td>High priority I/O interrupt (int0 rising)</td><td>OR</td></tr>
<tr><td>5</td><td>Low priority I/O interrupt (int1 rising)</td><td>OR</td></tr>
<tr><td>6</td><td>High priority I/O interrupt (int0 falling)</td><td>OR</td></tr>
<tr><td>7</td><td>Low priority I/O interrupt (int1 falling)</td><td>OR</td></tr>
</table></td></tr>
<tr><td>DIO_DIR0[7:4]</td><td>SFR A2</td><td>R/W</td><td>Programs the direction of DIO pins 7 through 4. 1 indicates output. Ignored if the pin is not configured as I/O. See DIO_PV and DIO_PW for special option for DIO6 and DIO7 outputs. See DIO_EEX for special option for DIO4 and DIO5.<br>Note: Bit 0, Bit 1, Bit 2 and Bit 3 must be set to 1.</td></tr>
</table>

| | | | | |
|---|---|---|---|---|
| *DIO_DIR1[7:6]*<br>*DIO_DIR1[3:0]* | SFR91 | R/W | Programs the direction of DIO pins 15, 14 and 11 through 8. 1 indicates output. Ignored if the pin is not configured as I/O.<br>**Note: Bit 4 and Bit 5 must be set to 1.** | |
| *DIO_DIR2[1:0]* | SFRA1[5:0] | R/W | Programs the direction of DIO pins 17 and 16. 1 indicates output. Ignored if the pin is not configured as I/O.<br>**Note: Bit 2, Bit 3, Bit 4 and Bit 5 must be set to 1.** | |
| *DIO_0[7:4]*<br>*DIO_1[7:6],*<br>*DIO_1[3:0]*<br>*DIO_2[1:0]* | SFR80<br>SFR90<br>SFR90<br>SFRA0[1:0] | R/W<br>R/W<br>R/W<br>R/W | Port 0<br>Port 1<br>Port 1<br>Port 2 | The value on the DIO pins. Pins configured as LCD will read zero. When written, changes data on pins configured as outputs. Pins configured as LCD or input will ignore writes. |
| *DIO_EEX* | 2008[4] | R/W | When set, converts DIO4 and DIO5 to interface with external EEPROM. DIO4 becomes SCK and DIO5 becomes bi-directional SDA. *LCD_NUM* must be less than 18. | |
| *DIO_PV* | 2008[2] | R/W | Causes VARPULSE to be output on DIO7, if DIO7 is configured as output. *LCD_NUM* must be less than 15. | |
| *DIO_PW* | 2008[3] | R/W | Causes WPULSE to be output on DIO6, if DIO6 is configured as output. *LCD_NUM* must be less than 17. | |
| *EEDATA[7:0]* | SFR 9E | R/W | Serial EEPROM interface data | |
| *EECTRL[7:0]* | SFR 9F | R/W | Serial EEPROM interface control | |
| *ECK_DIS* | 2005[5] | R/W | Emulator clock disable. When one, the emulator clock is disabled. **This bit is to be used with caution! Inadvertently setting this bit will inhibit access to the part with the ICE interface and thus preclude flash erase and programming operations**. If *ECK_DIS* is set, it should be done at least 1000ms after power-up to give emulators and programming devices enough time to complete an erase operation. | |
| *EQU[2:0]* | 2000[7:5] | R/W | Specifies the power equation to the CE. | |
| *EX_XFR*<br>*EX_RTC* | 2002[0]<br>2002[1] | R/W | Interrupt enable bits. These bits enable the XFER_BUSY and the RTC_1SEC interrupts to the MPU. Note that if either interrupt is to be enabled, EX6 in the 80515 must also be set. | |
| *FIR_LEN* | 2005[4] | R/W | The length of the ADC decimation FIR filter.<br>1: 22 ADC bits/3 CK32 cycles (384 CKFIR cycles),<br>0: 21 ADC bits/2 CK32 cycles (288 CKFIR cycles) | |
| *FLASH66Z* | 2005[1] | R/W | Should be set to 1 to minimize supply current. | |

| | | | |
|---|---|---|---|
| *FLSH_ERASE* | SFR 94 | W | Flash Erase Initiate<br>FLSH_ERASE is used to initiate either the Flash Mass Erase cycle or the Flash Page Erase cycle. Specific patterns are expected for FLSH_ERASE in order to initiate the appropriate Erase cycle.<br>(default = 0x00).<br>0x55 – Initiate Flash Page Erase cycle. Must be proceeded by a write to FLSH_PGADR @ SFR 0xB7.<br>0xAA – Initiate Flash Mass Erase cycle. Must be proceeded by a write to FLSH_MEEN @ SFR 0xB2 and the debug (CC) port must be enabled.<br>Any other pattern written to FLSH_ERASE will have no effect. |
| *FLSH_MEEN* | SFR B2[1] | W | Mass Erase Enable<br>0 – Mass Erase disabled (default).<br>1 – Mass Erase enabled.<br>***Must be re-written for each new Mass Erase cycle.*** |
| *FLSH_PGADR* | SFR B7[7:1] | W | Flash Page Erase Address<br>FLSH_PGADR[6:0] – Flash Page Address (page 0 thru 127) that will be erased during the Page Erase cycle. (default = 0x00).<br>***Must be re-written for each new Page Erase cycle.*** |
| *FLSH_PWE* | SFR B2[0] | R/W | Program Write Enable<br>0 – MOVX commands refer to XRAM Space, normal operation (default).<br>1 – MOVX @DPTR,A moves A to Program Space (Flash) @ DPTR.<br>This bit is automatically reset after each byte written to flash. Writes to this bit are inhibited when interrupts are enabled. |
| *IE_XFER*<br>*IE_RTC* | SFR E8[0]<br>SFR E8[1] | R/W | Interrupt flags. These flags are part of the *WDI* SFR register and monitor the XFER_BUSY interrupt and the RTC_1SEC interrupt. The flags are set by hardware and must be cleared by the interrupt handler. See also *WD_RST*. |
| *INTBITS* | SFR F8[6:0] | R | Interrupt inputs. The MPU may read these bits to see the input to external interrupts INT0, INT1, up to INT6. These bits do not have any memory and are primarily intended for debug use. |
| *LCD_BSTEN* | 2020[7] | R/W | Enables the LCD voltage boost circuit. |
| *LCD_CLK[1:0]* | 2021[1:0] | R/W | Sets the LCD clock frequency for COM/SEG pins (not the frame rate. Note: $f_w$ = CKFIR/128<br>00: $f_w/2^9$, 01: $f_w/2^8$, 10: $f_w/2^7$, 11: $f_w/2^6$ |
| *LCD_EN* | 2021[5] | R/W | Enables the LCD display. When disabled, VLC2, VLC1, and VLC0 are ground as are the COM and SEG outputs. |
| *LCD_FS[4:0]* | 2022[4:0] | R/W | Controls the LCD full scale voltage, VLC2:<br>$VLC2 = VLCD \cdot (0.7 + 0.3\frac{LCD\_FS}{31})$ |

<table>
<tr><td>LCD_MODE[2:0]</td><td>2021[4:2]</td><td>R/W</td><td>The LCD bias mode.<br>000: 4 states, 1/3 bias<br>001: 3 states, 1/3 bias<br>010: 2 states, ½ bias<br>011: 3 states, ½ bias<br>100: static display</td></tr>
<tr><td>LCD_NUM[4:0]</td><td>2020[4:0]</td><td>R/W</td><td>Controls the number of dual-purpose LCD/DIO pins to be configured as LCD. LCD_NUM will be between 0 and 18. The first dual-purpose pin to be allocated as LCD is SEG37/DIO17. The table below lists which SEG and DIO functions are selected for each LCD_NUM value.
<table>
<tr><th>LCD_NUM</th><th>SEG</th><th>DIO</th></tr>
<tr><td>1-4</td><td>None</td><td>DIO4-11, DIO14-17</td></tr>
<tr><td>5</td><td>SEG37</td><td>DIO4-11, DIO14-16</td></tr>
<tr><td>6</td><td>SEG36-37</td><td>DIO4-11, DIO14-15</td></tr>
<tr><td>7</td><td>SEG35-37</td><td>DIO4-11, DIO14</td></tr>
<tr><td>8-10</td><td>SEG34-37</td><td>DIO4-11</td></tr>
<tr><td>11</td><td>SEG34-37, SEG31</td><td>DIO4-10</td></tr>
<tr><td>12</td><td>SEG34-37, SEG30-31</td><td>DIO4-9</td></tr>
<tr><td>13</td><td>SEG34-37, SEG29-31</td><td>DIO4-8</td></tr>
<tr><td>14</td><td>SEG34-37, SEG28-31</td><td>DIO4-7</td></tr>
<tr><td>15</td><td>SEG34-37, SEG27-31</td><td>DIO4-6</td></tr>
<tr><td>16</td><td>SEG34-37, SEG26-31</td><td>DIO4-5</td></tr>
<tr><td>17</td><td>SEG34-37, SEG25-31</td><td>DIO4</td></tr>
<tr><td>18</td><td>SEG34-37, SEG24-31</td><td>None</td></tr>
</table></td></tr>
<tr><td>LCD_SEG0[3:0]-<br>LCD_SEG19[3:0],<br>LCD_SEG24[3:0]-<br>LCD_SEG31[3:0],<br>LCD_SEG34[3:0]-<br>LCD_SEG37[3:0],</td><td>2030[3:0]-<br>2043[3:0],<br>2048[3:0]-<br>204f[3:0],<br>2052[3:0]-<br>2055[3:0]</td><td>R/W</td><td>LCD Segment Data. Each word contains information for from 1 to 4 time divisions of each segment. In each word, bit 0 corresponds to COM0, on up to bit 3 for COM3.</td></tr>
<tr><td>MPU_DIV[2:0]</td><td>2004[2:0]</td><td>R/W</td><td>The MPU clock divider (from CKCE). These bits may be programmed by the MPU without risk of losing control.<br>000 - CKCE, 001 - CKCE/2, …, 111 - CKCE/$2^7$<br>MPU_DIV is 000 on power-up.</td></tr>
<tr><td>MUX_ALT</td><td>2005[2]</td><td>R/W</td><td>The MPU asserts this bit when it wishes the MUX to perform ADC conversions on an alternate set of inputs.</td></tr>
<tr><td>MUX_DIV[1:0]</td><td>2002[7:6]</td><td>R/W</td><td>The number of states in the input multiplexer.<br>00 - 6 states 01 - 4 states 10 - 3 states 11 - 2 states</td></tr>
<tr><td>MUX_E</td><td>2005[0]</td><td>R/W</td><td>MUX_SYNC enable. When high, converts SEG7 into a MUX_SYNC output.</td></tr>
<tr><td>OPT_TXDIS</td><td>2008[5]</td><td>R/W</td><td>Tristates the OPT_TX output.</td></tr>
</table>

| | | | |
|---|---|---|---|
| *PREBOOT* | SFR B2[7] | R | Indicates that the preboot sequence is active. |
| *PRE_SAMPS[1:0]* | 2001[7:6] | R/W | Together w/ *SUM_CYCLES,* this value determines the number of samples in one sum cycle between XFER interrupts for the CE. Number of samples = *PRE_SAMPS*SUM_CYCLES*.<br>00-42, 01-50, 10-84, 11-100 |
| *RTC_SEC[5:0]*<br>*RTC_MINI[5:0]*<br>*RTC_HR[4:0]*<br>*RTC_DAY[2:0]*<br>*RTC_DATE[4:0]*<br>*RTC_MO[3:0]*<br>*RTC_YR[7:0]* | 2015<br>2016<br>2017<br>2018<br>2019<br>201A<br>201B | R/W | The RTC interface. These are the 'year', 'month', 'day', 'hour', 'minute' and 'second' parameters for the RTC. The RTC is set by writing to these registers. Year 00 is defined as a leap year.<br>SEC 00 to 59<br>MIN 00 to 59<br>HR 00 to 23 (00=Midnight)<br>DAY 01 to 07 (01=Sunday)<br>DATE 01 to 31<br>MO 01 to 12<br>YR 00 to 256 |
| *RTC_DEC_SEC*<br>*RTC_INC_SEC* | 201C[1]<br>201C[0] | W | RTC time correction bits. Only one bit may be pulsed at a time. When pulsed, causes the RTC time value to be incremented (or decremented) by an additional second the next time the *RTC_SEC* register is clocked. The pulse width may be any value. If an additional correction is desired, the MPU must wait 2 seconds before pulsing one of the bits again. |
| *RTM_EN* | 2002[3] | R/W | Real Time Monitor enable. When '0', the RTM output is low. This bit enables the two wire version of RTM |
| *RTM0[7:0]*<br>*RTM1[7:0]*<br>*RTM2[7:0]*<br>*RTM3[7:0]* | 2060<br>2061<br>2062<br>2063 | R/W<br>R/W<br>R/W<br>R/W | Four RTM probes. Before each CE code pass, the values of these registers are serially output on the RTM pin. The *RTM* registers are ignored when *RTM_EN*=0. |
| *SECURE* | SFR B2[6] | R/W | Enables security provisions that prevent external reading of flash memory and CE program RAM. This bit is reset on chip reset and may only be set. Attempts to write zero are ignored. |
| *SSI_EN* | 2070[7] | R/W | Enables the Synchronous Serial Interface (SSI) on SEG3, SEG4, and SEG5 pins. If *SSI_RDYEN* is set, SEG6 is enabled also. The pins take on the new functions SCLK, SSDATA, SFR, and SRDY, respectively. When *SSI_EN* is high and *LCD_EN* is low, these pins are converted to the SSI function, regardless of *LCDEN* and *LCD_NUM*. For proper LCD operation, *SSI_EN* must not be high when *LCD_EN* is high. |
| *SSI_10M* | 2070[6] | R/W | SSI clock speed: 0: 5MHz, 1: 10MHz |
| *SSI_CKGATE* | 2070[5] | R/W | SSI gated clock enable. When low, the SCLK is continuous. When high, the clock is held low when data is not being transferred. |
| *SSI_FSIZE[1:0]* | 2070[4:3] | R/W | SSI frame pulse format:<br>0: once at beginning of SSI sequence (whole block of data),<br>1: every 8 bits, 2: every 16 bits, 3: every 32 bits. |
| *SSI_FPOL* | 2070[2] | R/W | SFR pulse polarity: 0: positive, 1: negative |
| *SSI_RDYEN* | 2070[1] | R/W | SRDY enable. If *SSI_RDYEN* and *SSI_EN* are high, the SEG6 pin is configured as SRDY. Otherwise, it is an LCD driver. |
| *SSI_RDYPOL* | 2070[0] | R/W | SRDY polarity: 0: positive, 1: negative |

| | | | |
|---|---|---|---|
| *SSI_BEG[7:0]*<br>*SSI_END[7:0]* | 2071[7:0]<br>2072[7:0] | R/W | The beginning and ending address of the transfer region of the CE data memory. If the SSI is enabled, a block of words starting with *SSI_BEG* and ending with *SSI_END* will be sent. *SSI_END* must be larger than *SSI_BEG*. The maximum number of output words is limited by the number of SSI clocks in a CE code pass—see *FIR_LEN, MUX_DIV,* and *SSI_10M*. |
| *SUM_CYCLES [5:0]* | 2001[5:0] | R/W | Together w/ *PRE_SAMPS,* this value determines (for the CE) the number of samples in one sum cycle between XFER interrupts. Number of samples = *PRE_SAMPS*SUM_CYCLES*. |
| *TMUX[3:0]* | 2000[3:0] | R/W | Selects one of 16 inputs for TMUXOUT.<br>0 – DGND (analog)<br>1 – IBIAS (analog)<br>2 – PLL_2.5V (analog)<br>3 – VBIAS (analog)<br>4 – RTM (Real time output from CE)<br>5 – WDTR_EN (Comparator 1 Output AND V1LT3)<br>6 – reserved<br>7 – reserved<br>8 – RXD (from Optical interface)<br>9 – MUX_SYNC (from MUX_CTRL)<br>A – CK_10M<br>B – CK_MPU<br>C – reserved for production test<br>D – RTCLK<br>E – CE_BUSY<br>F – XFER_BUSY |
| *RESERVED* | 2005[7] | R/W | Must be zero. |
| *TRIMSEL* | 20FD | W | Selects the temperature trim fuse to be read with the *TRIM* register (*TRIMM[2:0]*: 4, *TRIMBGA*: 5, *TRIMBGB*: 6) |
| *TRIM* | 20FF | R | Contains *TRIMBGA*, *TRIMBGB*, or *TRIMM[2:0]* depending on the value written to *TRIMSEL*. If *TRIMBGB* = 0 then the IC is a 6511 else the IC is a 6511H. |
| *VERSION[7:0]* | 2006 | R | The silicon revision number. This data sheet does not apply to revisions < 000 0100. |
| *VREF_CAL* | 2004[7] | R/W | Brings VREF out to the VREF pin. This feature is disabled when *VREF_DIS*=1. |
| *VREF_DIS* | 2004[3] | R/W | Disables the internal voltage reference. |
| *WD_RST* | SFR E8[7] | W | Resets the WD timer. The WDT is reset when a 1 is written to this bit. Only byte operations on the whole WDI register should be used. |
| *WD_OVF* | 2002[2] | R/W | The WD overflow status bit. This bit is set when the WD timer overflows. It is powered by the VBAT pin and at boot-up will indicate if the part is recovering from a WD overflow or a power fault. This bit should be cleared by the MPU on boot-up. It is also automatically cleared when RESETZ is low. |

## CE Program and Environment

### CE Program

The CE program is supplied by TERIDIAN as a data image that can be merged with the MPU operational code for meter applications. Typically, the CE program covers most applications and does not need to be modified. The description in this section applies to CE code revision CE11B05.

### Formats

All CE words are 4 bytes. Unless specified otherwise, they are in 32-bit two's complement (-1 = 0xFFFFFFFF). 'Calibration' parameters are defined in flash memory (or external EEPROM) and must be copied to CE memory by the MPU before enabling the CE. 'Internal' variables are used in internal CE calculations. 'Input' variables allow the MPU to control the behavior of the CE code. 'Output' variables are outputs of the CE calculations. The corresponding MPU address for the most significant byte is given by 0x1000 + 4 x CE_address and 0x1003 + 4 x CE_address for the least significant byte.

### Constants

Constants used in the CE Data Memory tables are:

- Sampling frequency: $F_S$ = 32768Hz/13 = 2520.62Hz (*MUX_DIV* = 1) or 32786/10 = 3276.8Hz (*MUX_DIV* = 2)
- $F_0$ is the fundamental signal frequency, typically 50 or 60Hz.
- *IMAX* is the external rms current corresponding to 250mV peak at the inputs IA or IB.
- *VMAX* is the external rms voltage corresponding to 250mV peak at the input VA.
- NACC, the accumulation count for energy measurements is *PRE_SAMPS*SUM_CYCLES*. This value resides in *SUM_PRE* (CE address 36).
- Accumulation count time for energy measurements is *PRE_SAMPS*SUM_CYCLES*/$F_S$.
- In_8 is a gain constant of current channel n. Its value is 8 or 1 and is controlled by *In_SHUNT*.
- X is a gain constant of the pulse generators. Its value is determined by *PULSE_FAST* and *PULSE_SLOW*.
- Voltage LSB = *VMAX* * $3.3243*10^{-9}$ V (peak).

The system constants *IMAX* and *VMAX* are used by the MPU to convert internal digital quantities (as used by the CE) to external, i.e. metering quantities. Their values are determined by the scaling of the voltage and current sensors used in an actual meter. The LSB values used in this document relate digital quantities at the CE or MPU interface to external meter input quantities. For example, if a SAG threshold of 80V peak is desired at the meter input, the digital value that should be programmed into *SAG_THR* would be 80V/*SAG_THR*LSB, where *SAG_THR*LSB is the LSB value in the description of *SAG_THR*.

The parameters *EQU*, *CE_EN*, *PRE_SAMPS,* and *SUM_CYCLES* are essential to the function of the CE and are stored in I/O RAM (see I/O RAM section).

### Environment

Before starting the CE using the *CE_EN* bit, the MPU has to establish the proper environment for the CE by implementing the following steps:

- Loading the image for the CE code into CE PRAM.
- Loading the CE data into CE DRAM.
- Establishing the equation to be applied in *EQU*.
- Establishing the accumulation period and number of samples in *PRE_SAMPS* and *SUM_CYCLES.*
- Establishing the number of cycles per ADC mux cycle.

The default configuration is *FIR_LEN* = 1 (three cycles per conversion) and *MUX_DIV* = 1 (4 conversions per mux cycle). There must be thirteen CK32 cycles (see System Timing Diagram, Figure 13). This means that the product of the number of cycles per ADC conversion and the number of conversions per cycle must be 12 (allowing for one settling cycle).

Alternatively, the 71M6511 can be operated at ten CK32 cycles per ADC mux cycle (*MUX_DIV* = 2). CE quantities are stated in this section for *MUX_DIV* = 2, if they differ from those associated with the default setting.

During operation, the MPU is in charge of controlling the multiplexer cycles, for example by inserting an alternate multiplexer sequence at regular intervals using *MUX_ALT*. This enables temperature measurement. The polarity of CHOP must be altered for each sample. It must also alternate for each alternate multiplexer reading.

The MPU must program *CHOP_EN* alternately between 01 and 10 on every CE_BUSY interrupt except for the first CE_BUSY after an XFER_BUSY interrupt. Note that when XFER_BUSY occurs, it will always be at the same time as a CE_BUSY interrupt.

### CE Calculations

The CE performs the precision computations necessary to accurately measure power. These computations include offset cancellation, phase compensation, product smoothing, product summation, frequency detection, VAR calculation, sag detection, peak detection, and voltage phase measurement. All data computed by the CE is dependent on the selected meter equation as given by *EQU (*in I/O RAM*)*. As a function of *EQU*, the element components V0 through I2 take on different meanings.

| ***EQU*** | **Watt & VAR Formula** (WSUM/VARSUM) | **Element Input Mapping** | | | |
|---|---|---|---|---|---|
| | | *W0SUM/ VAR0SUM* | *W1SUM/ VAR1SUM* | *I0SQSUM* | *I1SQSUM* |
| 0 | VA IA (1 element, 2W 1$\phi$) | VA*IA | VA*IB | IA | IB |
| 1 | VA*(IA-IB)/2 (1 element, 3W 1$\phi$) | VA*(IA-IB)/2 | VA*IB | IA-IB | IB |

## CE RAM Locations

### CE Front End Data (Raw Data)

Access to the raw data provided by the AFE is possible by reading addresses 0 through 7, as listed below.

| Address (HEX) | Name | Description |
|---|---|---|
| 00 | IA | Phase A current |
| 01 | VA | Phase A voltage |
| 02 | IB | Phase B current |
| 03 | - | Reserved |
| 04 | - | Reserved |
| 05 | - | Reserved |
| 06 | TEMP | Temperature |
| 07 | -- | Reserved |

### CE Status Word

Since the CE_BUSY interrupt occurs at 2520.6Hz (or at 3276.8Hz when *MUX_DIV* = 2), it is desirable to minimize the computation required in the interrupt handler of the MPU. The MPU can read *CESTATUS* at every CE_BUSY interrupt.

| CE Address | Name | Description |
|---|---|---|
| 0x51 | *CESTATUS* | See description of CE status word below |

The CE Status Word is useful for generating early warnings to the MPU. It contains sag warnings for phase A, as well as F0, the derived clock operating at the fundamental input frequency. *CESTATUS* provides information about the status of voltage and input AC signal frequency, which are useful for generating an early power fail warning to initiate necessary data storage. *CESTATUS* represents the status flags for the preceding CE code pass (CE_BUSY interrupt).

**Note: The CE does not store sag alarms from one code pass to the next. *CESTATUS* is refreshed at every CE_BUSY interrupt and remains valid for up to 100µs after the CE_BUSY interrupt occurs. Unsynchronized read operations of CESTATUS will yield unreliable results.**

The significance of the bits in *CESTATUS* is shown in the table below:

| *CESTATUS [bit]* | Name | Description |
|---|---|---|
| 31-29 | Not Used | These unused bits will always be zero. |
| 28 | *F0* | *F0* is a square wave at the exact fundamental input frequency. |
| 27 | *RESERVED* | |
| 26 | *RESERVED* | |
| 25 | *SAG_A* | Normally zero. Becomes one when VA remains below *SAG_THR* for *SAG_CNT* samples. Will not return to zero until VA rises above *SAG_THR*. |
| 24-0 | Not Used | These unused bits will always be zero. |

For generating proper status information, the CE is initialized by the MPU using *SAG_THR* (default of 80V RMS at the meter input if *VMAX*=600V) and *SAG_CNT* (default 80 samples). Using the default value for *SAG_CNT*, the peak-to-peak signal has to be below *SAG_THR* value for 32 milliseconds to activate the *SAG_X* status bits.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x31 | *SAG_THR* | +56,722,300 (0x361837C) | Meter voltage inputs must be above this threshold to prevent sag alarms. LSB = *VMAX* * $3.3243*10^{-9}$ V peak.<br>For example, if a sag threshold of 80V RMS is desired,<br>$SAG\_THR = \frac{80\sqrt{2}}{VMAX \cdot 3.3243 \cdot 10^{-9}}$ |
| 0x32 | *SAG_CNT* | 80 | Number of consecutive voltage samples below *SAG_THR* before a sag alarm is declared. 80*397µs = 31.8ms (for MUX_DIV = 1). |

## CE Transfer Variables

When the MPU receives the XFER_BUSY interrupt, it knows that fresh data is available in the transfer variables. CE transfer variables are modified during the CE code pass that ends with an XFER_BUSY interrupt. They remain constant throughout each accumulation interval. In this data sheet, the names of CE transfer variables always end with _X.

### Fundamental Power Measurement Variables

The table below describes each transfer variable for fundamental power measurement. All variables are signed 32 bit integers. Accumulated variables such as WSUM are internally scaled so they have at least 2x margin before overflow when the integration time is 1 second. Additionally, the hardware will not permit output values to 'fold back' upon overflow.

| CE Address | Name | Description |
|---|---|---|
| 42 | *RESERVED* | |
| 43 | *W0SUM_X* | The sum of Watt samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*).<br>LSB = $6.6952*10^{-13}$ *VMAX IMAX / In_8* Wh (for *MUX_DIV* = 1)<br>LSB = $5.1501*10^{-13}$ *VMAX IMAX / In_8* Wh (for *MUX_DIV* = 2) |
| 44 | *W1SUM_X* | |
| 45 | *RESERVED* | |
| 46 | *RESERVED* | |
| 47 | *VAR0SUM_X* | The sum of VAR samples from each wattmeter element (*In_8* is the gain configured by *IA_SHUNT* or *IB_SHUNT*).<br>LSB = $6.6952*10^{-13}$ *VMAX IMAX / In_8* Wh (for *MUX_DIV* = 1)<br>LSB = $5.1501*10^{-13}$ *VMAX IMAX / In_8* Wh (for *MUX_DIV* = 2) |
| 48 | *VAR1SUM_X* | |
| 49 | *RESERVED* | |

*WxSUM_X* is the Wh value accumulated for element 'X' in the last accumulation interval and can be computed based on the specified LSB value.

For example with *VMAX* = 600V and *IMAX* = 208A, LSB (for *WxSUM_X* ) is 0.08356 µWh (*MUX_DIV* = 1).

**Instantaneous Power Measurement Variables**

The *FREQSEL* Register selects the input phase used for frequency measurement and for the *MAIN_EDGE* counter. The frequency measurement is implemented using the frequency locked loop of the CE for the selected phase.

*IxSQSUM_X* and *VxSQSUM* are the squared current and voltage samples acquired during the last accumulation interval. *INSQSUM_X* can be used for computing the neutral current.

| CE Address | Name | Description |
|---|---|---|
| 33 | *RESERVED* | |
| 41 | *FREQ_X* | Fundamental frequency.<br>LSB $\equiv \frac{F_S}{2^{32}} \approx 0.587 \cdot 10^{-6}$ Hz for *MUX_DIV* = 1<br>*or* $\frac{F_S}{2^{32}} \approx 0.763 \cdot 10^{-6}$ Hz for *MUX_DIV* = 2 |
| 4A | *I0SQSUM_X* | The sum of squared current samples from each element.<br>LSB = 6.6952*10$^{-13}$ *IMAX*$^2$ / *In_8*$^2$ A$^2$h (for *MUX_DIV* = 1)<br>LSB = 5.1501*10$^{-13}$ *IMAX*$^2$ / *In_8*$^2$ *A*$^2$h *(*for *MUX_DIV* = 2) |
| 4B | *I1SQSUM_X* | |
| 4C | *RESERVED* | |
| 4D | *RESERVED* | |
| 4E | *V0SQSUM_X* | The sum of squared voltage samples from each element.<br>LSB= 6.6952*10$^{-13}$ *VMAX*$^2$ V$^2$h (for *MUX_DIV* = 1)<br>LSB = 5.1501*10$^{-13}$ *VMAX*$^2$V$^2$h *(*for *MUX_DIV* = 2) |
| 4F | *RESERVED* | |
| 50 | *RESERVED* | |

The RMS values can be computed by the MPU from the squared current and voltage samples as per the formulae:

$$Ix_{RMS} = \sqrt{\frac{IxSQSUM \cdot LSB \cdot 3600 \cdot F_S}{N_{ACC}}} \qquad Vx_{RMS} = \sqrt{\frac{VxSQSUM \cdot LSB \cdot 3600 \cdot F_S}{N_{ACC}}}$$

Note: FS = 2520.6Hz (*MUX_DIV* = 1) or 3276.8Hz (*MUX_DIV* = 2)

**Other Measurement Parameters**

*MAINEDGE_X* is useful for implementing a real-time clock based on the input AC signal. *MAINEDGE_X* is the number of half-cycles accounted for in the last accumulated interval for the AC signal of the phase specified in the *FREQSEL* register.

| CE Address | Name | Description |
|---|---|---|
| 52 | *RESERVED* | |
| 53 | *RESERVED* | |
| 55 | *MAINEDGE_X* | The number of edge crossings of the selected voltage in the previous accumulation interval. Edge crossings are either direction and are de-bounced. |

**Temperature Measurement and Temperature Compensation**

**Input variables:** *TEMP_NOM* is the reference value for temperature measurement, i.e. when this value is set with *TEMP_RAW_X* at known temperature. The 71M6511/6511H measures temperature with reference to this value.

*DEGSCALE* is the slope or rate of temperature increase or decrease from the *TEMP_NOM* for *TEMP_X* measurement.

*PPMC* and *PPMC2* are temperature compensation coefficients. Their values should reflect the characteristics of the band gap voltage reference of the chip. *PPMC* and *PPMC2* follow the square law characteristics to compensate for nonlinear temperature behaviors, when the 71M6511/6511H is in internal temperature compensation mode.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x11 | *TEMP_NOM* | 0 | During calibration, the value of *TEMP_RAW_X* should be placed in *TEMP_NOM*. |
| 0x30 | *DEGSCALE* | 9585 | Scale factor for *TEMP_X*.<br>*TEMP_X* = -*DEGSCALE**$2^{-22}$*(*TEMP_RAW_X*-*TEMP_NOM*). |
| 0x38 | *EXT_TEMP* | 0 | Should be 15 or 0. When 15, causes the CE to ignore internal temperature compensation and permits the MPU to control *GAIN_ADJ*. When internal temperature compensation is selected, *GAIN_ADJ* will be:<br>$GAIN\_ADJ = 16384 + floor\left(1 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}\right)$<br>Default is 0 (internal compensation). |
| 0x39 | *PPMC* | 0 | Linear temperature compensation factor. Equals the linear temperature coefficient (PPM/°C) of VREF multiplied by 26.84, or TC1 (expressed in µV/°C, see Electrical Specifications) multiplied by 22.46. A positive value will cause the meter to run faster when hot. The compensation factor affects both V and I and will therefore have a double effect on products. |
| 0x3A | *PPMC2* | 0 | Square-law temperature compensation factor. Equals the square-law temperature coefficient (PPM/°$C^2$) of VREF multiplied by 1374, or TC2 (expressed in µV/°$C^2$, see Electrical Specifications) multiplied by 1150.1. A positive value will cause the meter to run faster when hot. The compensation factor affects both V and I and will therefore have a double effect on products. |

*EXT_TEMP* allows the MPU to select between direct control of *GAIN_ADJ* or management of GAIN_ADJ by the CE, based on *TEMP_X* and the temperature correction coefficients *PPMC* and *PPMC2*.

**Output variables:** *TEMP_X* is the temperature measurement from reference temperature of *TEMP_NOM*. *TEMP_X* is computed using *TEMP_RAW_X* and *DEGSCALE*. This quantity is positive when the temperature is above the reference and is negative for cold temperatures.

*TEMP_RAW_X* is the raw processed value from ADC output and is the fundamental quantity for temperature measurement. *TEMP_RAW_X* is less than *TEMP_NOM* at higher temperatures. *TEMP_RAW_X* is more than *TEMP_NOM* for cooler temperatures than reference temperature.

*GAIN_ADJ* is a scaling factor for power measurements based on temperature (when in internal temperature compensation mode). In general, for higher temperatures it is lower than 16384 and higher than 16384 for lower temperatures. *GAIN_ADJ* is mainly dependent on the *PPMC*, *PPMC2* and *TEMP_X* register values. This parameter is automatically computed by the CE and is used by the CE for temperature compensation.

| CE Address | Name | Description |
|---|---|---|
| 0x40 | *TEMP_X* | Deviation from Calibration temperature. LSB = 0.1 $^0$C. |
| 0x54 | *TEMP_RAW_X* | Filtered, unscaled reading from temperature sensor. This value should be written to *TEMP_NOM* during meter calibration. |
| 0x2E | *GAIN_ADJ* | Scales all voltage and current inputs. 16384 provides unity gain. **Default is 16384**. If *EXT_TMP* = 0, *GAIN_ADJ* is updated by the CE. |

**Pulse Generation**

**Input variables:** The combination of the *PULSE_SLOW* and *PULSE_FAST* parameters control the speed of the pulse rate. The default values of 1 and 1 will maintain the original pulse rate given by the Kh equation.

*WRATE* controls the number of pulses that are generated per measured Wh and VARh quantities. The lower *WRATE* it is the slower is the pulse rate for measured power quantity. The metering constant Kh is derived from *WRATE* as the amount of energy measured for each pulse. That is, if Kh = 1Wh/pulse, a power applied to the meter of 120V and 30A results in one pulse per second. If the load is 240V at 150A, ten pulses per second will be generated.

Control is transferred to the MPU for pulse generation if *EXT_PULSE* > 0. In this case, the pulse rate is determined by *APULSEW* and *APULSER*. The MPU has to load the source for pulse generation in *APULSEW* and *APULSER* to generate pulses. Irrespective of the *EXT_PULSE,* status the output pulse rate controlled by *APULSEW* and *APULSER* is implemented by the CE only. By setting *EXT_PULSE* > 0, the MPU is providing the source for pulse generation. If *EXT_PULSE* is negative, *W0SUM_X* and *VAR0SUM_X* are the default pulse generation sources. In this case, creep cannot be controlled since it is an MPU function.

The maximum pulse rate is $F_S$ /2= 1260.3Hz (*MUX_DIV* = 1).

*PULSE_WIDTH* allows adjustment of the pulse width for compatibility with calibration and other external equipment. When *MUX_DIV* = 1, the minimum pulse width possible is 397µs.

The maximum time jitter is 397µs (for *MUX_DIV* = 1) and is independent of the number of pulses measured. Thus, if the pulse generator is monitored for 1 second, the peak jitter is 397PPM. After 10 seconds, the peak jitter is 39.7PPM. The average jitter is always zero. If it is attempted to drive either pulse generator faster than its maximum rate, it will simply output at its maximum rate without exhibiting any roll-over characteristics. The actual pulse rate, using *WSUM* as an example, is:

$$RATE = \frac{X \cdot WRATE \cdot WSUM \cdot F_S}{2^{46}} Hz$$

Where $F_S$ = 2520.6Hz (sampling frequency for *MUX_DIV* = 1) or 3276.8Hz (sampling frequency for *MUX_DIV* = 2) and X is the pulse gain factor derived from CE variables *PULSE_SLOW* and *PULSE_FAST* (see table below).

| CE Address | Name | Default | Description |
|---|---|---|---|
| 0x28 | *PULSE_SLOW* | 1 | When *PULSE_SLOW* > 0, the pulse generator input is reduced 64x.<br>When *PULSE_FAST* > 0, the pulse generator input is increased 16x.<br>These two parameters control the pulse gain factor X (see table below). Allowed values are either 1 or –1. |
| 0x29 | *PULSE_FAST* | 1 | |
| 0x2D | *WRATE* | 1556 | Kh =<br>*VMAX***IMAX**47.1132 / (*In_8***WRATE**$N_{ACC}$*X) Wh/pulse (for *MUX_DIV* = 1).<br>*VMAX***IMAX**36.2409 / (*In_8***WRATE**$N_{ACC}$*X) Wh/pulse (for *MUX_DIV* = 2). |
| 0x36 | *SUM_PRE* | 2520 | *PRE_SAMPS* * *SUM_CYCLES*. This variable is also called $N_{ACC}$. |
| 0x37 | *EXT_PULSE* | 15 | Should be 15 or 0. When zero, causes the pulse generators to respond to *WSUM_X* and *VARSUM_X*. Otherwise, the generators respond to values the MPU places in *APULSEW* and *APULSER*. |
| 0x3C | *PULSE_WIDTH* | 50 | The maximum pulse width (low-going pulse) is:<br>(2 * *PULSE_WIDTH* + 1) * 397µs (for *MUX_DIV* = 1)<br>(2 * *PULSE_WIDTH* + 1) * 305µs (for *MUX_DIV* = 2)<br>0 is a legitimate value. |
| 0x26 | *APULSEW* | 0 | Wh pulse generator input, to be updated by the MPU when using external pulse generation (see *DIO_PW* bit). The output pulse rate is:<br>*APULSEW* * $F_S$ * $2^{-32}$ * *WRATE* * $2^{-14}$<br>This input is buffered and can be updated by the MPU during a computation interval. The change will take effect at the beginning of the next interval. |
| 0x27 | *APULSER* | 0 | VARh pulse generator input to be updated by the MPU when using external pulse generation (see *DIO_PV* bit). The output pulse rate is:<br>*APULSER* * $F_S$*$2^{-32}$ * *WRATE* * $2^{-14}$<br>This input is buffered and can be updated by the MPU during a computation interval. The change will take effect at the beginning of the next interval. |

| X | *PULSE_SLOW* | *PULSE_FAST* |
|---|---|---|
| 1.5 * $2^2$ = 6 | -1 | -1 |
| 1.5 * $2^6$ = 96 | -1 | 1 |
| 1.5 * $2^{-4}$ = 0.09375 | 1 | -1 |
| 1.5 | 1 (default) | 1 (default) |

### Current Shunt Variables

**Input variables**: *IA_SHUNT* and *IB_SHUNT* can configure the current inputs to accept shunt resistor sensors. In this case the CE provides an additional gain of 8 to the current inputs. This will enable the pulse rate to change by 8 times. In order to maintain a normal pulse rate *WRATE* may have to be decreased by 8 times. Whenever *IA_SHUNT* or *IB_SHUNT* are set to 1 or a positive number, *In_8* is assigned a value of 8 in the equation for Kh.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 2A | *IA_SHUNT* | -1 | When +1, these variables increase the respective current gain by 8. The gain factor controlled by *In_SHUNT* is referred to as *In_8* throughout this document. Allowed values are 1 or –1. For example, if *IB_SHUNT*=-1, *IB_8 = 1, if IB_SHUNT* = 1, *IB_8* = 8.<br>*IA_SHUNT* corresponds to *IA_8*, *IB_SHUNT* corresponds to *IB_8*. |
| 2B | *IB_SHUNT* | -1 | |
| 2C | *RESERVED* | | |

### CE Calibration Parameters

The table below lists the parameters that are typically entered to affect calibration of meter accuracy.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 8 | *CAL_IA* | 16384 | These constants control the gain of their respective channels. The nominal value for each parameters is $2^{14}$ = 16384. The gain of each channel is directly proportional to its CAL parameter. Thus, if the gain of a channel is 1% slow, CAL should be scaled by 1/(1 – 0.01). |
| 9 | *CAL_VA* | 16384 | |
| A | *CAL_IB* | 16384 | |
| B | *RESERVED* | | |
| C | *RESERVED* | | |
| D | *RESERVED* | | |
| E | *PHADJ_A* | 0 | These two constants control the CT phase compensation. No compensation occurs when *PHADJ_X* = 0. As *PHADJ_X* is increased, more compensation (lag) is introduced. Range: $\pm 2^{15} - 1$. If it is desired to delay the current by the angle Φ:<br>$PHADJ\_X = 2^{20}\frac{a \cdot TAN\Phi}{b - c \cdot TAN\Phi}$<br>$a = 1 + (1-2^{-9})^2 - 2(1-2^{-9})\cos(2\pi F_0 T)$<br>$b = (1-2^{-9})\sin(2\pi F_0 T)$<br>$c = 1 - (1-2^{-9})\cos(2\pi F_0 T)$<br>$F_0 T = \frac{F_0}{F_S}$ |
| F | *PHADJ_B* | 0 | |
| 10 | *RESERVED* | 0 | |

**Other CE Parameters**

The table below shows CE parameters used for suppression of noise due to scaling and truncation effects as well as scaling factors.

| CE Address | Name | Default | Description |
|---|---|---|---|
| 2F<br>22 | *QUANTA*<br>*QUANTB* | 0<br>0 | These parameters are added to the Watt calculation to compensate for input noise and truncation.<br>LSB=(*VMAX***IMAX* / *IA_8*) *7.4162*$10^{-10}$ W for phase A, and<br>LSB=(*VMAX***IMAX* / *IB_8*) *7.4162*$10^{-10}$ W for phase B |
| 34<br>24 | *QUANT_VARA*<br>*QUANT_VARB* | 0<br>0 | These parameters are added to the VAR calculation to compensate for input noise and truncation.<br>LSB = (*VMAX***IMAX* / *IA_8*) * 7.4162*$10^{-10}$ W for phase A, and<br>LSB = (*VMAX***IMAX* / *IB_8*) * 7.4162*$10^{-10}$ W for phase B |
| 35<br>23 | *QUANT_IA*<br>*QUANT_IB* | 0<br>0 | These parameters are added to compensate for input noise and truncation in the squaring calculations for $I^2$ and $V^2$.<br>LSB=$VMAX^2$*7.4162*$10^{-10}$ $V^2$,<br>LSB= ($IMAX^2$/$IA\_8^2$)*7.4162*$10^{-10}$ $A^2$ for phase A and<br>LSB= ($IMAX^2$/$IB\_8^2$)*7.4162*$10^{-10}$ $A^2$ for phase B. |
| 3B | *KVAR* | 6448<br>12880 | Scale factor for the VAR calculation. The default value of *KVAR* should never need to be changed.<br>for *MUX_DIV* = 1<br>for *MUX_DIV* = 2 |

## TYPICAL PERFORMANCE DATA

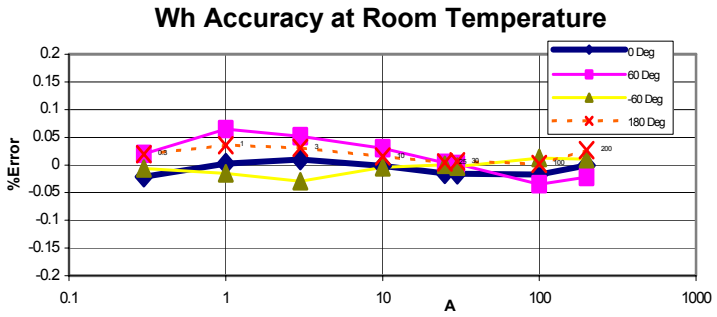



**Figure 24: Wh Accuracy, 0.3A - 200A/240V**

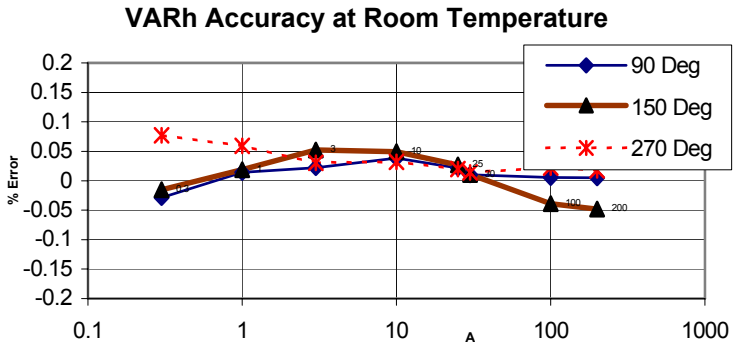



**Figure 25: VARh Accuracy for 0.3A to 200A/240V Performance**

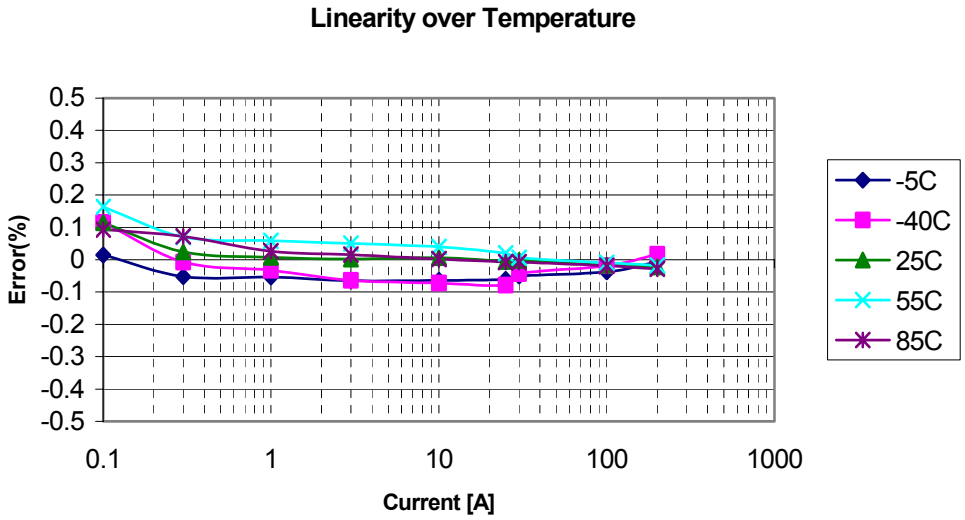
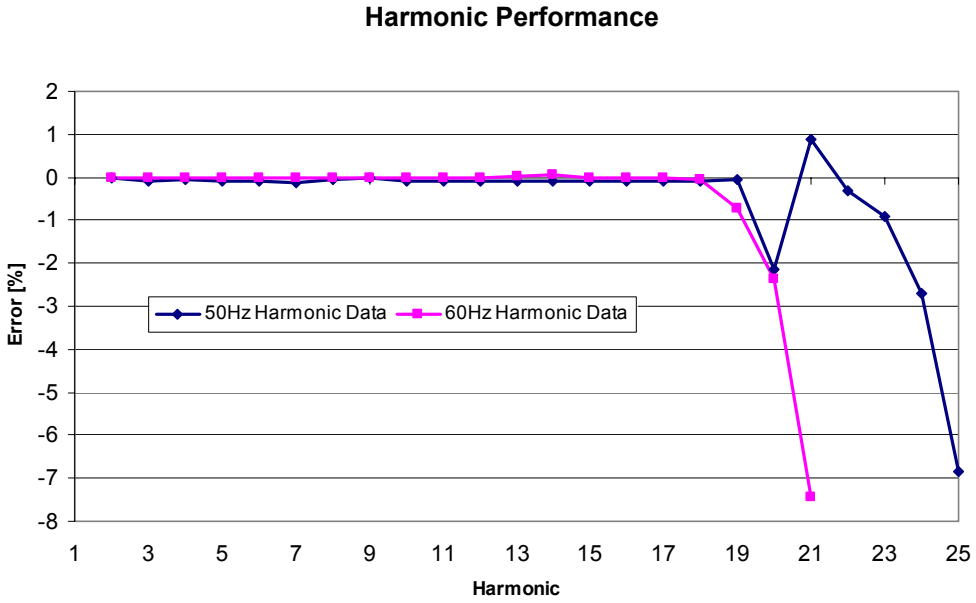



**Figure 26: 71M6511H Wh Accuracy over Current at Various Temperatures**




Test performed at current distortion amplitude of 40% and voltage distortion amplitude of 10% as per IEC 62053, part 22.

**Figure 27: Meter Accuracy over Harmonics at 240V, 30A**

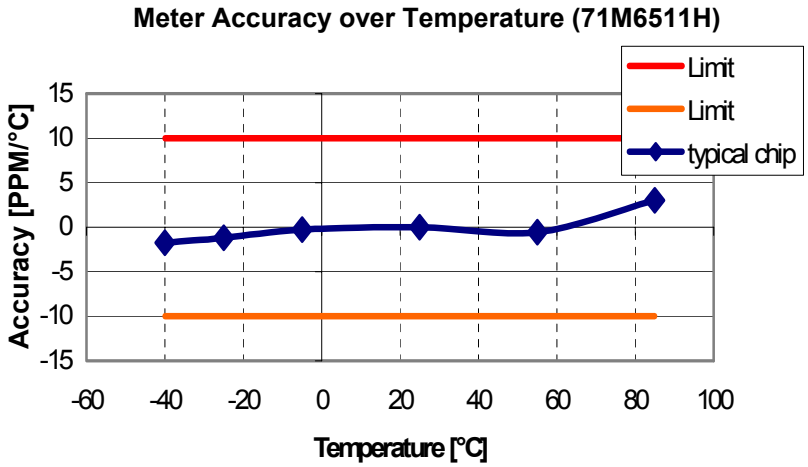



**Figure 28: Typical Meter Accuracy over Temperature Relative to 25°C (w/ Temperature Compensation)**

## APPLICATION INFORMATION

### Connection of Sensors (CT, Resistive Shunt, Rogowski Coil)

Figure 29 and Figure 30 show how resistive dividers, current transformers, restive shunts, and Rogowski coils are connected to the voltage and current inputs of the 71M6511.

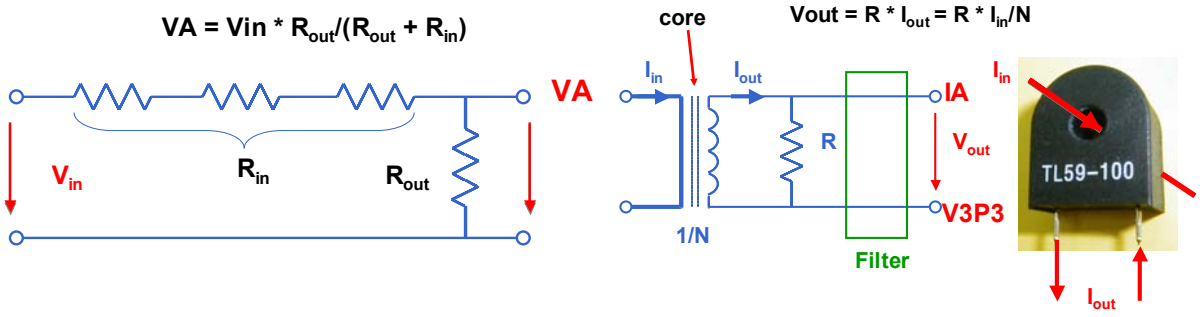



**Figure 29: Resistive Voltage Divider (left), Current Transformer (right)**

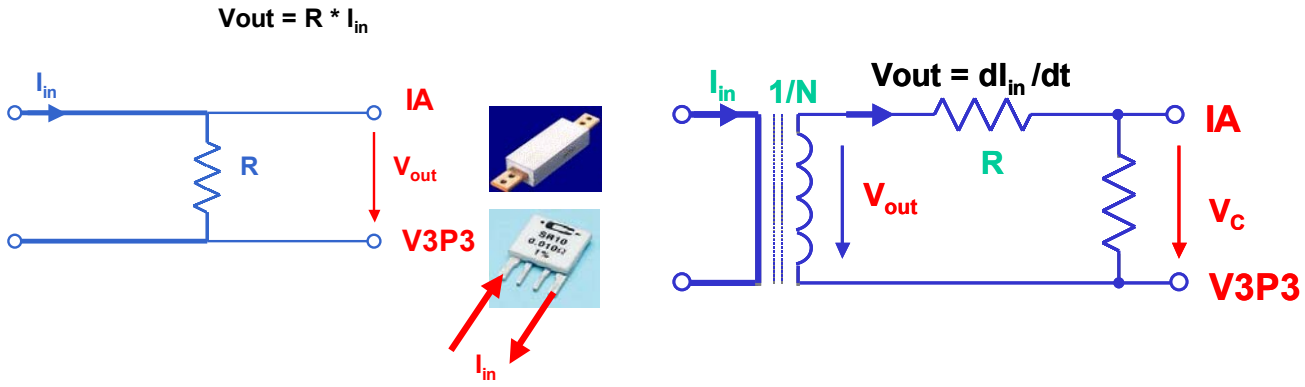



**Figure 30: Resistive Shunt (left), Rogowski Coil (right)**

### Distinction between 71M6511 and 71M6511H Parts

71M6511H parts go through a process of trimming and characterization during production that make them suitable to high-accuracy applications.

The first process applied to the 71M6511H is the trimming of the reference voltage, which is guaranteed to have accuracy over temperature of better that ±10PPM/°C.

The second process applied to the 71M6511H is the characterization of the reference voltage over temperature. The coefficients for the reference voltage are stored in so-called trim fuses (I/O RAM registers *TRIMBGA*, *TRIMBGB*, *TRIMM[2:0]*. The MPU program can read these trim fuses and calculate the correction coefficients PPM1 and PPM2 per the formulae given in the Performance Specifications section (VREF, VBIAS). See the Temperature Compensation section for details.

The fuse *TRIMBGB* is non-zero for the 71M6511H part and zero for the 71M6511 part.

Trim fuse information is not available for non-H parts. Thus, the standard are to be applied. These settings are:

- *PPMC* = TC1 * 22.46 = –149
- *PPMC2* = TC2 * 1150.1 = –392

### Temperature Compensation and Mains Frequency Stabilization for the RTC

The accuracy of the RTC depends on the stability of the external crystal. Crystals vary in terms of initial accuracy as well as in terms of behavior over temperature. The flexibility provided by the MPU allows for compensation of the RTC using the substrate temperature. To achieve this, the crystal has to be characterized over temperature and the three coefficients *Y_CAL*, *Y_CALC*, and *Y_CAL_C2* have to be calculated. Provided the IC substrate temperatures tracks the crystal temperature, the coefficients can be used in the MPU firmware to trigger occasional corrections of the RTC seconds count, using the *RTC_DEC_SEC* or *RTC_INC_SEC* registers in I/O RAM.

It is not recommended to measure crystal frequency directly due to the error introduced by the measurement probes. A practical method to measure the crystal frequency (when installed on the PCB with the 71M6511) is to have a DIO pin toggle every second, based on the RTC interrupt, with all other interrupts disabled. When this signal is measured with a precision timer, the crystal frequency can be obtained from the measured time period t (in µs):

$$f = 32768 \frac{10^6 \mu s}{t}$$

**Example:** Let us assume a crystal characterized by the measurements shown in Table 62. The values show that even at nominal temperature (the temperature at which the chip was calibrated for energy), the deviation from the ideal crystal frequency is 11.6 PPM, resulting in about one second inaccuracy per day, i.e. more than some standards allow.

| Deviation from Nominal Temperature [°C] | Measured Frequency [Hz] | Deviation from Nominal Frequency [PPM] |
|---|---|---|
| +50 | 32767.98 | -0.61 |
| +25 | 32768.28 | 8.545 |
| 0 | 32768.38 | 11.597 |
| -25 | 32768.08 | 2.441 |
| -50 | 32767.58 | -12.817 |

**Table 62: Frequency over Temperature**

As Figure 31 shows, even a constant compensation would not bring much improvement, since the temperature characteristics of the crystal are a mix of constant, linear, and quadratic effects (in commercially available crystals, the constant and quadratic effects are dominant).

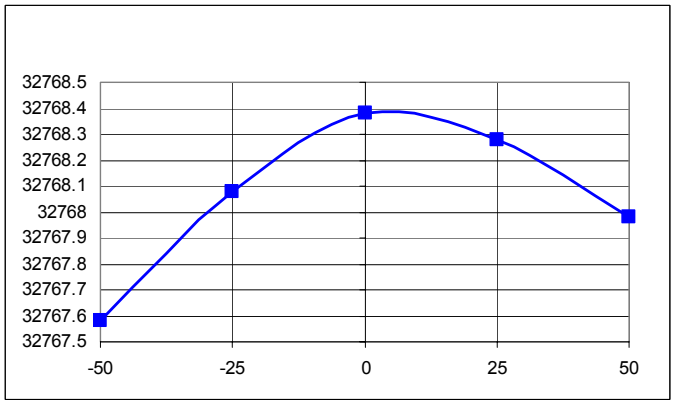



**Figure 31: Crystal Frequency over Temperature**

The temperature characteristics of the crystal are obtained from the curve in Figure 31 by curve-fitting the PPM deviations. A fairly close curve fit is achieved with the coefficients a = 10.89, b = 0.122, and c = –0.00714 (see Figure 32).

When applying the inverted coefficients, a curve (see Figure 32) will result that effectively neutralizes the original crystal characteristics. The frequencies were calculated using the fit coefficients as follows:

$$f = f_{nom} \cdot \left\{1 + \frac{a}{10^6} + T\frac{b}{10^6} + T^2\frac{c}{10^6}\right\}$$

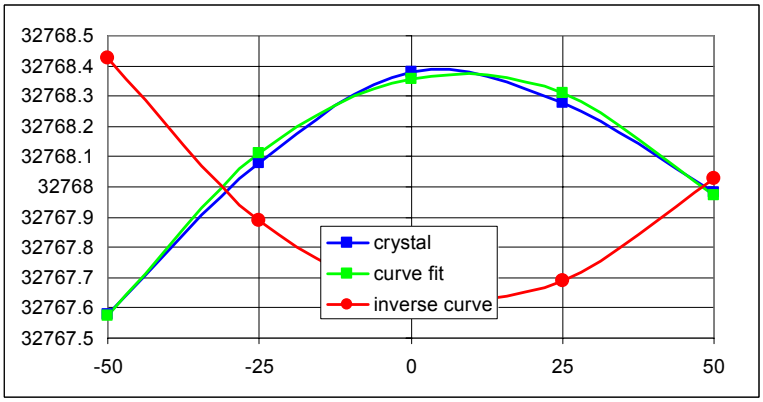



**Figure 32: Crystal Compensation**

The MPU Demo Code supplied with the TERIDIAN Demo Kits has a direct interface for these coefficients and it directly controls the *RTC_DEC_SEC* or *RTC_INC_SEC* registers. The Demo Code uses the coefficients in the following form:

$$CORRECTION(ppm) = \frac{Y\_CAL}{10} + T \cdot \frac{Y\_CALC}{100} + T^2 \cdot \frac{Y\_CALC2}{1000}$$

Note that the coefficients are scaled by 10, 100, and 1000 to provide more resolution. For our example case, the coefficients would then become (after rounding, since the Demo Code accepts only integers):

Y_CAL = 109, Y_CALC = 12, Y_CALC2 = 7

Alternatively, the mains frequency may be used to stabilize or check the function of the RTC. For this purpose, the CE provides a count of the zero crossings detected for the selected line voltage in the *MAIN_EDGE_X* address. This count is equivalent to twice the line frequency, and can be used to synchronize and/or correct the RTC.

## External Temperature Compensation

In a production electricity meter, the 71M6511 or 71M6511H is not the only component contributing to temperature dependency. In fact, a whole range of components (e.g. current transformers, resistor dividers, power sources, filter capacitors) will exhibit slight or pronounced temperature effects. Since the output of the on-chip temperature sensor is accessible to the MPU, temperature-compensation mechanisms with great flexibility, i.e. beyond the capabilities implemented in the CE, are possible.

## Temperature Measurement

Temperature measurement can be implemented with the following steps:

1) At a known temperature $T_N$, read the *TEMP_RAW* register of the CE and write the value into *TEMP_NOM*.
2) Read the *TEMP_X* register at the known temperature. The obtained value should be <±0.1°C.
3) The temperature T (in °C) at any environment can be obtained by reading TEMP_X and applying the following formula:

$$T = T_N + \frac{TEMP\_X}{10}$$

### Connecting LCDs

The 71M6511 has a LCD controller on-chip capable of controlling static or multiplexed LCDs. Figure 33 shows the basic connection for a LCD.

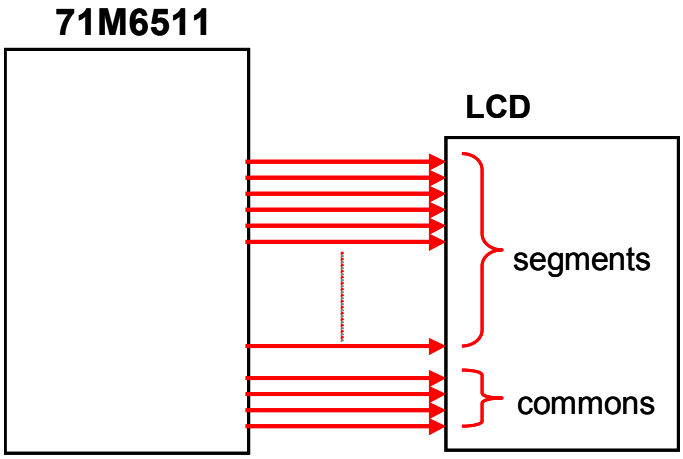



**Figure 33: Connecting LCDs**

Figure 34 shows how 5V LCDs can be operated even when a 5V supply is not available. Setting the I/O RAM register *LCD_BSTEN* to 1 starts the on-chip boost circuitry that will output an AC frequency on the VDRV pin. Using a small coupling capacitor, two general-purpose diodes and a reservoir capacitor, a 5VDC voltage is generated which can be fed back into the VLCD pin of the 71M6511. The LCD drivers are enabled with the I/O register *LCD_ON*; I/O register *LCD_FS* is used to adjust contrast, and *LCD_MODE* selects the operation mode (LCD type).

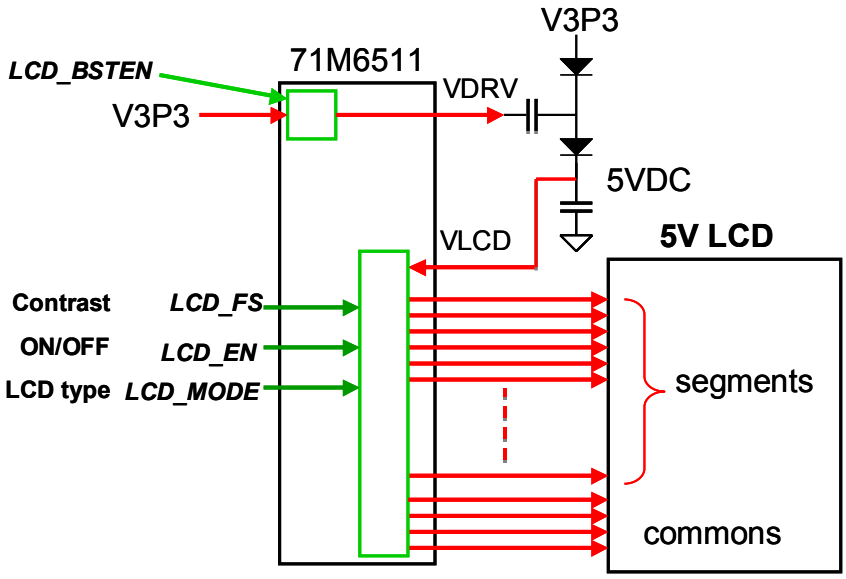



**Figure 34: LCD Boost Circuit**

### Connecting I2C EEPROMs

I2C EEPROMs or other I2C compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 35. Pull-up resistors of roughly 3kΩ to V3P3 should be used for both SCL and SDA signals. The *DIO_EEX* register in I/O RAM must be set to 1 in order to convert the DIO pins DIO4 and DIO5 to I2C pins SCL and SDA.

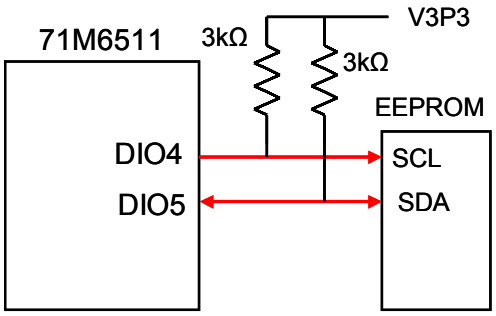



**Figure 35: EEPROM Connection**

### Connecting 5V Devices

In general, all pins of the 71M6511 are compatible with external 5V devices. The exceptions are the power supply pins and the RX pin of the UART (see section Electrical Specifications).

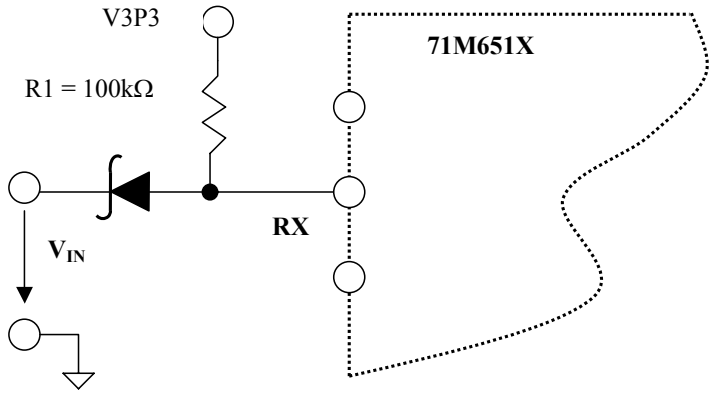



**Figure 36: Interfacing RX to a 0-5V Signal**

Figure 36 shows how a 5V signal from an external device can be safely interfaced to the RX pin.

### Optical Interface

The pins OPT_TX and OPT_RX can be used for a regular serial interface, e.g. by connecting a RS_232 transceiver, or they can be used to directly operate optical components, e.g. an infrared diode and phototransistor implementing a FLAG interface. Figure 37 shows the basic connections. The OPT_TX pin becomes active when the I/O RAM register *OPT_TXDIS* is set to 0.

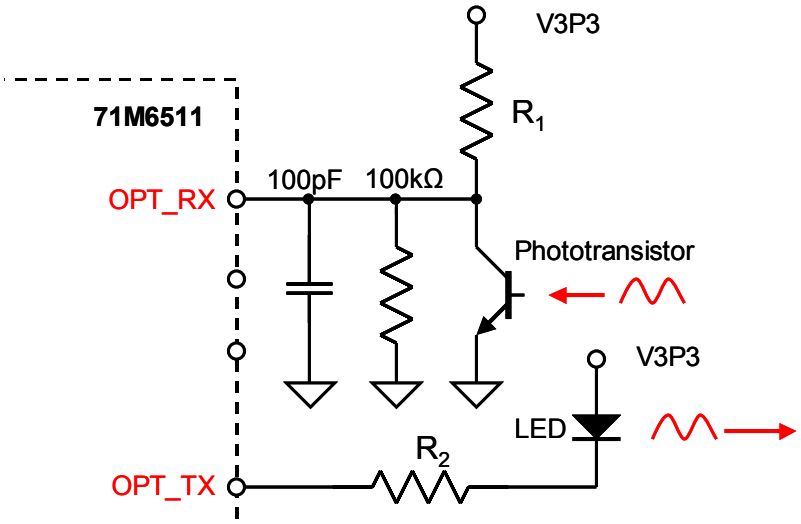



**Figure 37: Connection for Optical Components**

### Connecting V1 and Reset Pins

A voltage divider should be used to establish a safe range for V1 when the meter is in mission mode (V1 must be lower than 2.9V in all cases in order to keep the hardware watchdog timer enabled). For proper debugging or loading code into the 71M6511 mounted on a PCB, it is necessary to have a provision like the header shown above R1 in Figure 38. A shorting jumper on this header pulls V1 up to V3P3, disabling the hardware watchdog timer. C1 helps suppressing ESD.

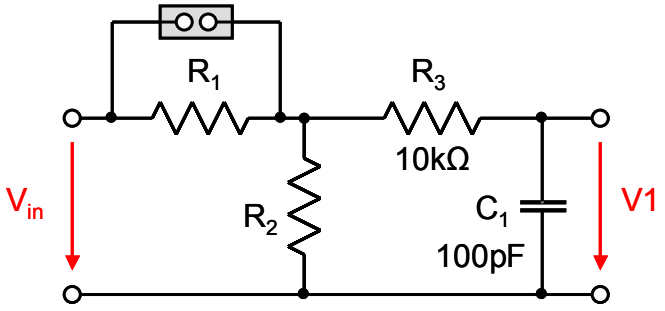



**Figure 38: Voltage Divider for V1**

Even though a functional meter will not necessarily need a reset switch, it is useful to have a reset pushbutton for prototyping. When a circuit is used in an EMI environment, the RESETZ pin should be supported by the external components shown in Figure 39. $R_1$ should be in the range of 200Ω, $R_2$ should be around 10Ω. The capacitor $C_1$ should be 1nF. R1 and C1 should be mounted as close as possible to the IC. In cases where the trace from the pushbutton switch to the RESETZ pin poses a problem, $R_2$ can be removed.

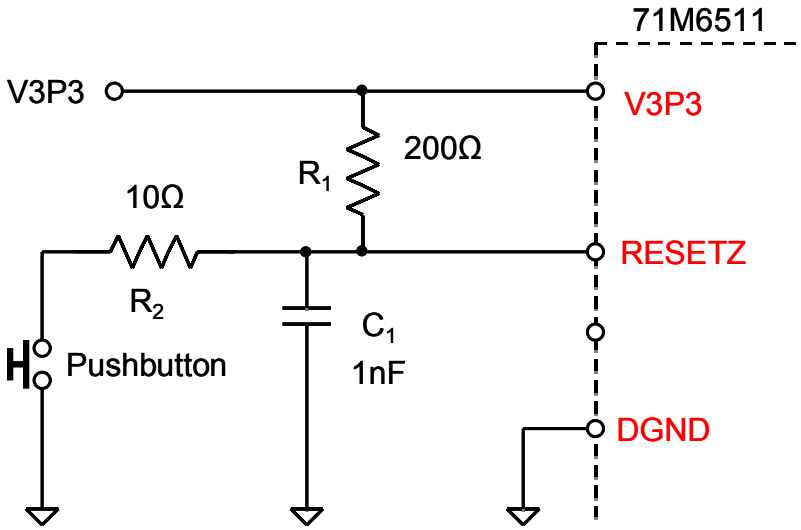



**Figure 39: External Components for RESETZ**

### Flash Programming

Operational or test code can be programmed into the flash memory using either an in-circuit emulator or the Flash Download Board Module (FDBM) available from TERIDIAN. The flash programming procedure uses the E_RTS, E_RXTX, and E_TCLK pins.

### MPU Firmware Library

All application-specific MPU functions mentioned above under “Application Information” are available from TERIDIAN as a standard ANSI C library and as ANSI “C” source code. The code is available as part of the Demonstration Kit for the 71M6511 and 71M6511H ICs. The Demonstration Kits come with the 71M6511 or 71M6511H IC preprogrammed with demo firmware mounted on a functional sample meter PCB (Demo Board). The Demo Boards allow for quick and efficient evaluation of the IC without having to write firmware or having to supply an in-circuit emulator (ICE).

A reference guide for firmware development on the 71M6511 and 71M6511H is available as a separate document (Software User’s Guide, “SUG”). The User’s Manuals supplied with the Demo Kits contain MPU address maps for the demo code as well as other useful information, such as sample calibration procedures.

## SPECIFICATIONS

### Electrical Specifications

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| **Supplies and Ground Pins:** | |
| V3P3D, V3P3A | –0.5V to 4.6V |
| \| V3P3D - V3P3A \| | 0V to 0.5V |
| VLCD | -0.5V to 7V |
| VBAT | -0.5V to 4.6V |
| GNDD | -0.5V to +0.5V |
| **Analog Output Pins:** | |
| VREF, VBIAS | -1mA to 1mA,<br>-0.5 to V3P3A+0.5V |
| V2P5 | -1mA to 1mA,<br>-0.5V to 3.0V |
| **Analog Input Pins:** | |
| IA, VA, IB | -0.5V to V3P3A+0.5V |
| XIN, XOUT | -0.5V to 3.0V |
| RX | -0.5V to 3.6V |
| OPT_RX | -1mA to 1mA<br>-0.5 to V3P3A+0.5V |
| **Digital Input Pins:** | |
| DIO4-11, DIO14-17, E_RXTX, E_RST | -0.5 to 6V |
| TEST, RESETZ | -0.5 to V3P3D+0.5V |
| **All Other Pins:** | |
| Input pins | -5mA to 5mA<br>-0.5V to V3P3D+0.5V |
| Output pins | -30mA to 30mA<br>-0.5 to V3P3D+0.5V |
| **Temperature:** | |
| Operating junction temperature (peak, 100ms) | 140 °C |
| Operating junction temperature (continuous) | 125 °C |
| Storage temperature | –45 °C to 165 °C |
| Solder temperature – 10 second duration | 250 °C |
| **ESD Stress:** | |
| Pins IA, VA, IB, RX, TX, E_RST, E_TCLK, E_RXTX | 6kV |
| All other pins | 2kV |

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| 3.3V Supply Voltage (**V3P3A, V3P3D**) † | Normal Operation | 3.0 | 3.3 | 3.6 | V |
| | Battery Backup | 0 | | 3.45 | V |
| **VLCD** | | 2.9 | | 5.5 | V |
| **VBAT** | No Battery | Externally Connect to V3P3D | | | |
| | Battery Backup | 2.0 | | 3.8 | V |
| Operating Temperature | | -40 | | 85 | ºC |

†V3P3A and V3P3D should be shorted together on the circuit board. GNDA and GNDD should also be shorted on the circuit board.

### LOGIC LEVELS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Digital high-level input voltage, $V_{IH}$ | | 2 | | V3P3D | V |
| Digital low-level input voltage, $V_{IL}$ | | –0.3 | | 0.8 | V |
| Digital high-level output voltage $V_{OH}$ | $I_{LOAD}$ = 1mA | V3P3D –0.4 | | V3P3D | V |
| | $I_{LOAD}$ = 15mA | V3P3D-0.6 | | | V |
| Digital low-level output voltage $V_{OL}$ | $I_{LOAD}$ = 1mA | 0 | | 0.4 | V |
| | $I_{LOAD}$ = 15mA | | | 0.8 | V |
| Input pull-up current, $I_{IL}$ | VIN=0V | | | | |
| RESETZ | | 10 | | 100 | µA |
| E_RXTX, E_RST | | 10 | | 100 | µA |
| Other digital inputs | | -1 | | 1 | µA |
| Input pull down current, $I_{IH}$ | VIN=V3P3D | | | | |
| TEST | | 10 | | 100 | µA |
| Other digital inputs | | -1 | | 1 | µA |

### SUPPLY CURRENT

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **V3P3A + V3P3D + VLCD** current | Normal Operation, **V3P3A=V3P3D=VLCD**=3.3V<br>CKMPU=614kHz<br>VBAT=3.6V<br>No Flash memory write | | 6.4 | 9.5 | mA |
| **V3P3A** current | | | 3.7 | 4.3 | mA |
| **V3P3D** current | | | 2.5 | 4.8 | mA |
| **VLCD** current | | | 0.2 | 0.4 | mA |
| **VBAT** current | | -300 | | 300 | nA |
| **V3P3D** current | Normal Operation, **V3P3A=V3P3D=VLCD**=3.3V<br>VBAT=3.6V, no Flash memory write<br>CKMPU=1,228kHz<br>CKMPU=2,456kHz<br>CKMPU=4,912kHz | | <br><br><br>2.9<br>3.6<br>5.1 | | <br><br><br>mA<br>mA<br>mA |
| **V3P3A + V3P3D** current | Power save/sleep mode<br>**V3P3A=V3P3D=VLCD**=3.3V, CE, ADC, E_TCLK, VREF disabled<br>CKMPU=153.5kHz<br>CKMPU=38.4kHz | | <br><br><br>6<br>4.9 | <br><br><br>7 | <br><br><br>mA<br>mA |
| **V3P3D** current, Write Flash | Normal Operation as above, except write Flash at maximum rate. | | 7 | | mA |
| **VBAT** current, VBAT=3.6V | Battery backup, **≤25°C**<br>**V3P3A=V3P3D=VLCD**=0V<br>$f_{OSC}$ = 32kHz **85°C** | | 2<br>4 | 4<br>12 | µA<br>µA |

### 2.5V VOLTAGE REGULATOR

Unless otherwise specified, load = 5mA

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage overhead **V3P3-V2P5** | Reduce V3P3 until V2P5 drops 200mV | | | 440 | mV |
| PSSR **ΔV2P5/ΔV3P3** | RESETZ=*1,* iload=*0* | -3 | | +3 | mV/V |

### VREF, VBIAS

Unless otherwise specified, *VREF_DIS*=0

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **VREF** output voltage, VNOM(25) | Ta = 22ºC | 1.193 | 1.195 | 1.197 | V |
| **VREF** chop step | | | | 40 | mV |
| **VREF** output impedance | *VREF_CAL* = 1, ILOAD = 10µA, -10µA | | | 2.5 | kΩ |
| **VNOM** definition[A] | VNOM(T) = VREF(22) + (T–22)TC1 + (T–22)$^2$TC2 | | | | V |
| -- If TRIMBGA and TRIMBGB available (**6511H**) -- | | | | | |
| **VREF** temperature coefficients<br>TC1 (linear)<br>TC2 (quadratic)<br>TRIMBGA, TRIMBGB, TRIMM[2:0]: See *TRIMSEL*, *TRIM* registers | x(33-0.28y) + 0.33y + 7.9<br>x(0.02-0.0002y) – 0.46<br>where x = 0.1TRIMBGB - 0.14(TRIMM[2:0]+0.5),<br>$y = \frac{\frac{TEMP\_NOM}{4.7404} - 500TRIM\_BGA - 370000}{900}$ | | | | µV/°C<br>µV/°C$^2$ |
| **VREF(T)** deviation from VNOM(T)<br>$\frac{VREF(T) - VNOM(T)}{VNOM} \frac{10^6}{\max(\lvert T-22\rvert, 40)}$ | | -10 | | 10 | ppm/ºC |
| -- If TRIMBGA and TRIMBGB not available (**6511**) -- | | | | | |
| **VREF** temperature coefficients<br>TC1 (linear)<br>TC2 (quadratic) | | | 7.0<br>-0.341 | | µV/ºC<br>µV/°C$^2$ |
| **VREF(T)** deviation from VNOM(T)<br>$\frac{VREF(T) - VNOM(T)}{VNOM} \frac{10^6}{\max(\lvert T-22\rvert, 40)}$ | Ta = -40ºC to +85ºC | -40 | | +40 | ppm/ºC |
| **VREF** aging | Ta = 25ºC | | ±25 | | ppm/<br>year |
| **VBIAS** output voltage | Ta = 25ºC<br>Ta = -40ºC to 85ºC | (-1%)<br>(-2%) | 1.5<br>1.5 | (+1%)<br>(+2%) | V<br>V |
| **VBIAS** output impedance | ILOAD = 1mA, -1mA | | 240 | 500 | Ω |

[A] This relationship describes the nominal behavior of VREF at different temperatures.

### CRYSTAL OSCILLATOR

Crystal is disconnected. Test load is series 200pF, 100kΩ connected between DGND and XOUT.

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Maximum Output Power to Crystal[4] | Crystal connected | | | 1 | µW |
| XIN to XOUT Capacitance[1] | | | | 3 | pF |
| Capacitance to DGND[1]<br>XIN<br>XOUT | | | | <br>5<br>5 | <br>pF<br>pF |
| Watchdog RTC_OK threshold | | | | 25 | kHz |

### ADC CONVERTER, VDD REFERENCED

*FIR_LEN*=0, *VREF_DIS*=0, *VDDREFZ*=0

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Recommended Input Range (Vin-**V3P3A**) | | -250 | | 250 | mV peak |
| Voltage to Current Crosstalk: $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$ | *Vin* = 200mV peak, 65Hz, on VA<br>*Vcrosstalk* = largest measurement on IA or IB | -10 | | 10 | µV/V |
| THD (First 10 harmonics)<br>250mV- peak<br>20mV- peak | Vin=65Hz, 64kpts FFT, Blackman-Harris window | | | <br>-75<br>-90 | <br>dB<br>dB |
| Input Impedance | Vin=65Hz | 40 | | 90 | kΩ |
| Temperature coefficient of Input Impedance | Vin=65Hz | | 1.7 | | Ω/°C |
| LSB size | *FIR_LEN*=1 | | 150 | | nV/LSB |
| Digital Full Scale | | | ±2097152 | | LSB |
| ADC Gain Error versus %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$ | Vin=200mV peak, 65Hz V3P3A=3.0v, 3.6V | | | 50 | ppm/% |
| Input Offset (Vin-**V3P3A**) | | -10 | | 10 | mV |

### OPTICAL INTERFACE

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **OPT_TX** VOH (**V3P3D-OPT_TX**) | ISOURCE=1mA | | | 0.4 | V |
| **OPT_TX** VOL | ISINK=20mA | | | 0.7 | V |
| **OPT_RX** Vin Threshold (VinRISING+VinFALLING)/2 | | 200 | 250 | 300 | mV |
| **OPT_RX** Vin Hysteresis (VinRISING-VinFALLING) | | 5 | | 30 | mV |
| **OPT_RX** input impedance | \|Vin\|≤300mV | 1 | | | MΩ |

### TEMPERATURE SENSOR

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Nominal Sensitivity ($S_n$)[4] | TA=25ºC, TA=75ºC | | -900 | | LSB/ºC |
| Nominal Offset ($N_n$)[4] | Nominal relationship: $N(T)= S_n*T+N_n$ | | 400000 | | LSB |
| Temperature Error[1] $ERR = (T-25) - \frac{(N(T)-N(25))}{S_n}$ | TA = -40ºC to +85ºC | -3 | | 3 | ºC |

### LCD BOOST

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDRV Frequency | | | OSC/2 | | Hz |
| VDRV Sink Current | Vol=1.5V | 1.2 | | 2.75 | mA |
| VDRV Source Current | Voh=1.5V | 1.2 | | 2.6 | mA |
| VLCD Target Voltage | | 4.5 | | 5.5 | V |
| VLCD Input Current | VLCD=5.0V, *LCD_FS*=1F, *LCD_MODE*=0,1,2,3 *LCD_BSTEN*=1 | | | 450 | µA |

### LCD DRIVERS

Applies to all COM and SEG pins. Unless otherwise stated, VLCD=5.0V, *LCD_FS*=1F

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VLC0 Max Voltage (*LCD_FS* =1F) | With respect to VLCD | -0.2 | | 0 | V |
| VLC0 Min Voltage (*LCD_FS* =00) | With respect to VLCD*0.7 | -0.2 | | 0.2 | V |
| VLC1 Voltage,<br>1/3 bias<br>½ bias | <br>With respect to 2*VLCD/3<br>With respect to VLCD/2 | <br>-10<br>-10 | | <br>+10<br>+10 | <br>%<br>% |
| VLC0 Voltage,<br>1/3 bias<br>½ bias | <br>With respect to VLCD/3<br>With respect to VLCD/2 | <br>-15<br>-10 | | <br>+15<br>+10 | <br>%<br>% |
| Output Impedance | $\Delta I_{LOAD}$=10µA | | | 30 | kΩ |

### RTC

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Range for date | | 2000 | - | 2255 | year |

### RESETZ

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Reset pulse width | | 5 | | | µs |
| Reset pulse fall time | | | | 1 | µs |

### COMPARATORS

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Offset Voltage<br>**V1-VBIAS** | | <br>-20 | | <br>15 | <br>mV |
| Hysteresis Current<br>**V1** | <br>Vin = VBIAS - 100mV | <br>0.8 | | <br>1.2 | <br>µA |
| Response Time<br>**V1** | <br>±100mV overdrive | <br>2 | | <br>15 | <br>µs |
| WD Disable Threshold (**V1**-**V3P3A**) | | -400 | | -10 | mV |

### RAM AND FLASH MEMORY

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| CE RAM wait states | CKMPU = 4.9MHz | 5 | | | Cycles |
| | CKMPU = 1.25MHz | 2 | | | Cycles |
| Flash write cycles | -40°C to +85°C | 20,000 | | | Cycles |
| Flash data retention | 85°C | 10 | | | Years |
| Flash data retention | 25°C | 100 | | | Years |
| Flash byte writes between page or mass erase operations | | | | 2 | Cycles |

### FLASH MEMORY TIMING

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Write Time per Byte | | | | 42 | µs |
| Page Erase (512 bytes) | | | | 20 | ms |
| Mass Erase | | | | 200 | ms |
| Flash byte writes between page or mass erase operations | | | | 2 | Cycles |

### EEPROM INTERFACE

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Write Clock frequency | CKMPU=4.9MHz, Using interrupts | | 78 | | kHz |
| | CKMPU=4.9MHz, "bit-banging" DIO4/5 | | 150 | | kHz |

FOOTNOTES

[1]This parameter is has been verified in production samples, but is not measured in production.
[2]This parameter is has been verified in production samples, but is measured in production only at DC.
[3]This parameter is measured in production at the limits of the specified operating temperature.
[4]This parameter defines a nominal relationship rather than a measured parameter. Correct circuit operation is verified with other specs that use this nominal relationship as a reference.

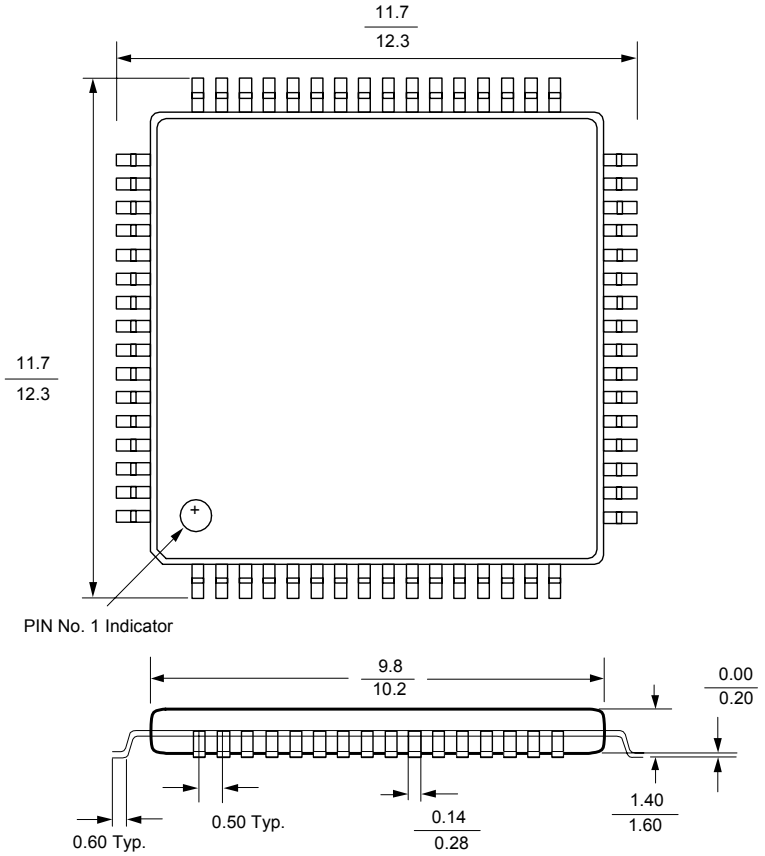
**Recommended External Components**

| NAME | FROM | TO | FUNCTION | VALUE | UNIT |
|---|---|---|---|---|---|
| C1 | **V3P3A** | **AGND** | Bypass capacitor for 3.3V supply | ≥0.1±20% | µF |
| C2 | **V3P3D** | **DGND** | Bypass capacitor for 3.3V supply | ≥0.1±20% | µF |
| XTAL | **XIN** | **XOUT** | 32.768kHz crystal. Electrically similar to ECS ECX-3TA series | 32.768 | kHz |
| CXS | **XIN** | **AGND** | Load capacitor for crystal (depends on crystal specs and board parasitics). | 22±10% | pF |
| CXL | **XOUT** | **AGND** | | 22±10% | pF |
| CBIAS | **VBIAS** | **AGND** | Bypass capacitor for VBIAS | ≥1000±20% | pF |
| CBST1 | **VDRV** | **External** | Boost charging capacitor | 33±20% | nF |
| C2P5 | **V2P5** | **DGND** | Bypass capacitor for V2P5 | ≥0.1±20% | µF |
| CBST2 | **VLCD** | **DGND** | Boost bypass capacitor | ≥0.22±20% | µF |

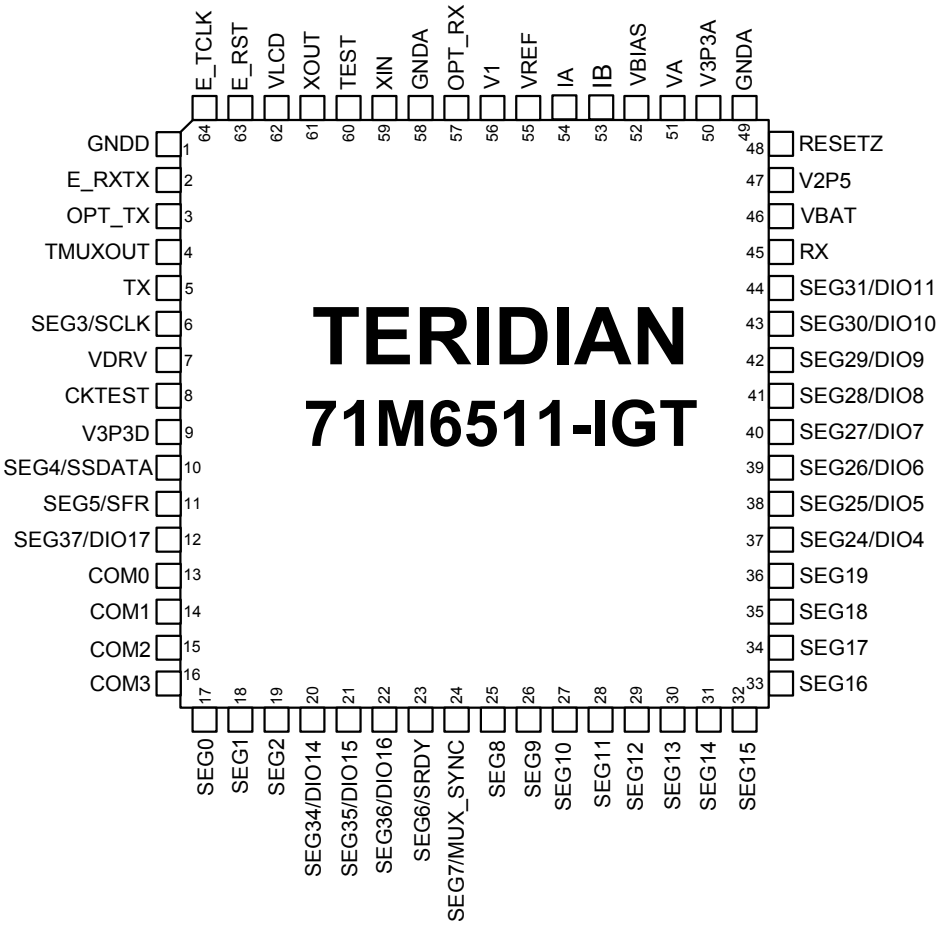
## Packaging Information

**64-Pin LQFP PACKAGE OUTLINE (Bottom View).**

NOTE: Controlling dimensions are in mm.



**Pinout (Top View)**



## Pin Descriptions

### Power/Ground Pins

| Name | Pin # | Type | Description |
|---|---|---|---|
| GNDA | 49, 58 | P | Analog ground: This pin should be connected directly to the ground plane. |
| GNDD | 1 | P | Digital ground: This pin should be connected directly to the ground plane. |
| V3P3A | 50 | P | Analog power supply: A 3.3V power supply should be connected to this pin. |
| V3P3D | 9 | P | Digital power supply: A 3.3V power supply should be connected to this pin. |
| VBAT | 46 | P | Battery backup power supply. A battery or super-capacitor should be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3D. |
| V2P5 | 47 | O | Output of the internal 2.5V regulator. A 0.1µF capacitor to GNDA should be connected to this pin. |
| VLCD | 62 | P | LCD power supply. A DC source of 3.3V to 5.0V should be connected to this pin. |

### Analog Pins

| Name | Pin # | Type | Circuit | Description |
|---|---|---|---|---|
| IA | 54 | I | 6 | Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer or shunt resistor. **If the pin is unused it must be connected to V3P3A or tied to the IB pin.** |
| VA | 51 | I | 6 | Line Voltage Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a resistor divider. **If the pin is unused it must be tied to V3P3A.** |
| IB | 53 | I | 6 | Line Current Sense Input: This pin is a voltage input to the internal A/D converter. Typically, it is connected to the output of a current transformer or shunt resistor. **If the pin is unused it must be connected to V3P3A or tied to the IA pin.** |
| V1 | 56 | I | 7 | Comparator Input: This pin is a voltage input to the internal comparator. The voltage applied to the pin is compared to an internal reference voltage of 1.5V. If the input voltage is above the reference, the comparator output will be high (1). If the comparator output is low, a voltage fault will occur. **See the precautions in the Applications Section for terminating this pin.** |
| VREF | 55 | O | 9 | Voltage Reference for the ADC. A 0.1µF capacitor to GNDA should be connected to this pin. |
| VBIAS | 52 | O | 9 | This pin outputs the reference voltage used by the power fault detection circuit. A 1,000pF capacitor to GND should be connected to this pin. |
| XIN<br>XOUT | 59<br>61 | I | 8 | Crystal Inputs: A 32kHz style crystal should be connected across these pins. Typically, a 20pF capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details. |
| VDRV | 7 | O | 4 | Voltage boost output. |

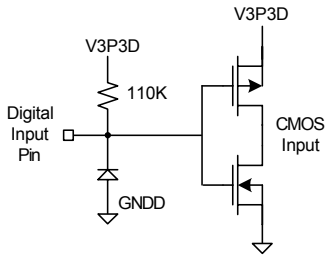
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified under “I/O Equivalent Circuits”.

**Digital Pins:**

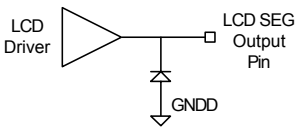
| Name | Pin # | Type | Circuit | Description |
|---|---|---|---|---|
| COM3,<br>COM2,<br>COM1,<br>COM0 | 16<br>15<br>14<br>13 | O | 5 | LCD Common Outputs: These 4 pins provide the select signals for the LCD display. |
| SEG19…SEG8,<br>SEG2…SEG0 | See pinout | O | 5 | Dedicated LCD Segment Output pins. |
| SEG24/DIO4…<br>SEG31/DIO11,<br>SEG34/DIO14…<br>SEG37/DIO17 | See pinout | O | 3, 4, 5 | Multi-use pins, configurable as either LCD SEG driver or DIO (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **If unused, these pins must be configured as outputs.** |
| SEG7/<br>MUX_SYNC | 24 | O | 4, 5 | Multi-use-pin LCD Segment Output/ MUX_SYNC is output for Synchronous serial interface |
| SEG6/SRDY | 23 | I/O | 2, 5 | Multi-use-pin, LCD Segment Outputs/ SRDY input for Synchronous serial interface. **When configured as SRDY, this pin must be pulled down to GNDD.** |
| SEG5/SFR | 11 | O | 4, 5 | Multi-use-pin, LCD Segment Output/ SFR output for Synchronous serial interface. |
| SEG4/SDATA | 10 | O | 4, 5 | Multi-use-pin, LCD Segment Output/ SDATA output for Synchronous serial interface. |
| SEG3/SCLK | 6 | O | 4, 5 | Multi-use-pin, LCD Segment Output/ SCLK output for Synchronous serial interface. |
| CKTEST | 8 | O | 4 | Clock PLL output. Can be enabled and disabled by *CKOUT_DIS*. |
| TMUXOUT | 4 | O | 4 | Digital output test multiplexer. Controlled by *DMUX[3:0]*. |
| OPT_RX | 57 | I | 7 | Optical Receive Input: This pin may receive a signal from an external photo-detector used in an IR serial interface. **If this pin is unused it must be terminated to V3P3D or GNDD.** |
| OPT_TX | 3 | O | 4 | Optical LED Transmit Output: This pin is designed to directly drive an LED for transmitting data in an IR serial interface. Can be tristated with *OPT_TXDIS* to be multiplexed with other DIO pins. |
| RESETZ | 48 | I | 1 | This input pin resets the chip into a known state. For normal operation, this pin is set to 1. To reset the chip, this pin is driven to 0. This pin has an internal 30µA (nominal) current source pull up. A 0.1µF capacitor to GNDD should be connected to this pin. **See the precautions in the Applications Section for terminating this pin.** |
| RX | 45 | I | 3 | UART input. **The voltage applied at this input must be below 3.6V. If this pin is unused it must be terminated to V3P3D or GNDD.** |
| TX | 5 | O | 4 | UART output. |
| E_RXTX | 2 | I/O | 1, 4 | Emulator serial data. This pin has an internal pull-up resistor. |
| E_TCLK | 64 | O | 4 | Emulator clock. |
| E_RST | 63 | I/O | 1, 4 | Emulator reset. This pin has an internal pull-up resistor. **See the precautions in the Applications Section for terminating this pin.** |
| TEST | 60 | I | 7 | Enables Production Test. **This pin must be grounded in normal operation.** |

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified on the following page.

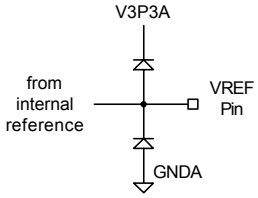
## I/O Equivalent Circuits:



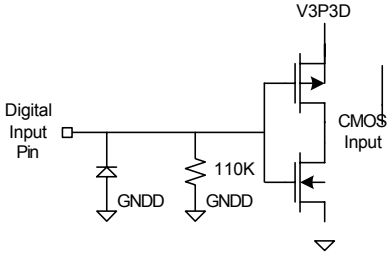

**Digital Input Equivalent Circuit**
**Type 1:**
Standard Digital Input or
pin configured as DIO Input
with Internal Pull-Up



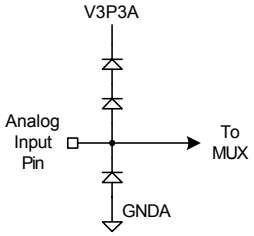

**LCD Output Equivalent Circuit**
**Type 5:**
LCD SEG or
pin configured as LCD SEG



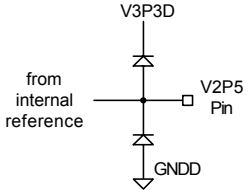

**VREF Equivalent Circuit**
**Type 9:**
VREF



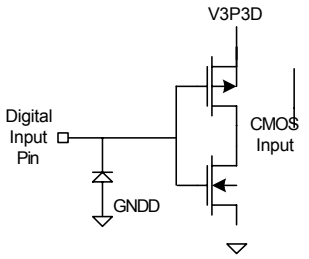

**Digital Input**
**Type 2:**
Pin configured as DIO Input
with Internal Pull-Down



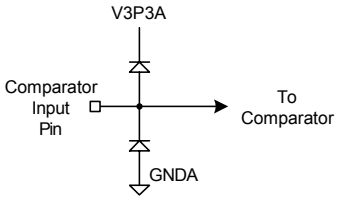

**Analog Input Equivalent Circuit**
**Type 6**:
ADC Input



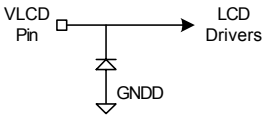

**V2P5 Equivalent Circuit**
**Type 10:**
V2P5



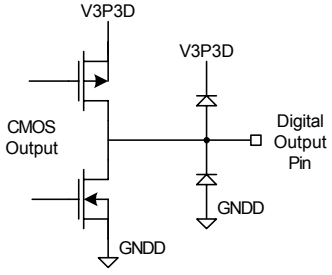

**Digital Input Type 3:**
Standard Digital Input or
pin configured as DIO Input



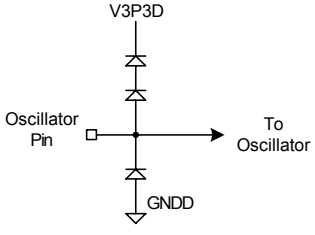

**Comparator Input Equivalent**
**Circuit Type 7:**
Comparator Input



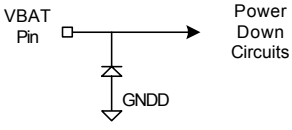

**VLCD Equivalent Circuit**
**Type 11:**
VLCD Power




**Digital Output Equivalent Circuit**
**Type 4:**
Standard Digital Output or
pin configured as DIO Output




**Oscillator Equivalent Circuit**
**Type 8:**
Oscillator I/O




**VBAT Equivalent Circuit**
**Type 12:**
VBAT Power

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARKING |
|---|---|---|
| **71M6511**<br>64-pin LQFP, 0.5% accuracy | 71M6511-IGT | 71M6511-IGT |
| **71M6511**<br>64-pin Lead-Free LQFP, 0.5% accuracy | 71M6511-IGT/F | 71M6511-IGT |
| **71M6511**<br>64-pin LQFP, 0.5% accuracy, T&R | 71M6511-IGTR | 71M6511-IGT |
| **71M6511**<br>64-pin Lead-Free LQFP, 0.5% accuracy, T&R | 71M6511-IGTR/F | 71M6511-IGT |
| **71M6511H**<br>64-pin LQFP, 0.1% accuracy | 71M6511H-IGT | 71M6511H-IGT |
| **71M6511H**<br>64-pin Lead-Free LQFP, 0.1% accuracy | 71M6511H-IGT/F | 71M6511H-IGT |
| **71M6511H**<br>64-pin LQFP, 0.1% accuracy, T&R | 71M6511H-IGTR | 71M6511H-IGT |
| **71M6511H**<br>64-pin Lead-Free LQFP, 0.1% accuracy, T&R | 71M6511H-IGTR/F | 71M6511H-IGT |



TERIDIAN Semiconductor Corp., 6440 Oak Canyon, Irvine, CA 92618

TEL (714) 508-8800, FAX (714) 508-8877, http://www.teridian.com

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