ADVANCED
LINEAR
DEVICES, INC.

ALD1701A/ALD1701B
ALD1701/ALD1701G

MICROPOWER RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD1701A/ALD1701B/ALD1701/ALD1701G is a monolithic CMOS micropower high slew rate operational amplifier intended for a broad range of analog applications using ±1V to ±5V dual power supply systems, as well as +2V to +10V battery operated systems. All device characteristics are specified for +5V single supply or ±2.5V dual supply systems. Supply current is 250μA maximum at 5V supply voltage. It is manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process.

The ALD1701A/ALD1701B/ALD1701/ALD1701G is designed to offer a trade-off of performance parameters providing a wide range of desired specifications. It has been developed specifically for the +5V single supply or ±1V to ±5V dual supply user and offers the popular industry standard pin configuration of μA741 and ICL7611 types.

Several important characteristics of the device make application easier to implement at those voltages. First, the operational amplifier can operate with rail to rail input and output voltages. This means the signal input voltage and output voltage can be equal to the positive and negative supply voltages. This feature allows numerous analog serial stages and flexibility in input signal bias levels. Second, the device was designed to accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Third, the output stage can typically drive up to 50pF capacitive and 10KΩ resistive loads.

These features, combined with extremely low input currents, high open loop voltage gain of 100V/mV, useful bandwidth of 700KHz, a slew rate of 0.7V/μs, low power dissipation of 0.5mW, low offset voltage and temperature drift, make the ALD1701 a versatile, micropower operational amplifier.

The ALD1701A/ALD1701B/ALD1701/ALD1701G, designed and fabricated with silicon gate CMOS technology, offers 1pA typical input bias current. On chip offset voltage trimming allows the device to be used without nulling in most applications. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

FEATURES

- All parameters specified for +5V single supply or ±2.5V dual supply systems
- Rail to rail input and output voltage ranges
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 1.0pA typical (30pA max.)
- Ideal for high source impedance applications
- Dual power supply ±1.0V to ±5.0V operation
- Single power supply +2.0V to +10.0V operation
- High voltage gain -- typically 100V/mV @ ±2.5V(100dB)
- Drive as low as 10KΩ load
- Output short circuit protected
- Unity gain bandwidth of 0.7MHz
- Slew rate of 0.7V/μs
- Low power dissipation
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

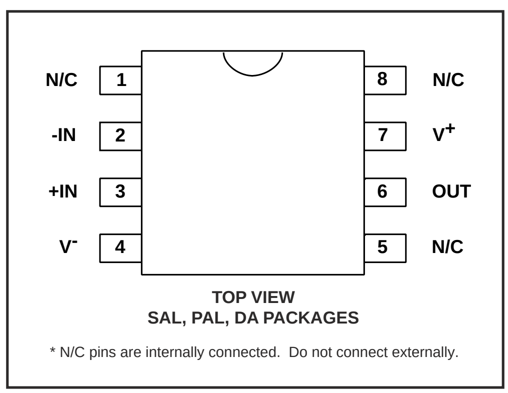
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to 125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1701ASAL	ALD1701APAL	ALD1701ADA
ALD1701BSAL	ALD1701BPAL	ALD1701BDA
ALD1701SAL	ALD1701PAL	ALD1701DA
ALD1701GSAL	ALD1701GPAL	ALD1701GDA

* Contact factory for leaded (non-RoHS) or high temperature versions.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+		10.6V
Differential input voltage range		-0.3V to V^+ +0.3V
Power dissipation		600 mW
Operating temperature range	SAL, PAL packages	0°C to +70°C
	DA package	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature, 10 seconds		+260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS
T_A = 25°C V_S = ±2.5V unless otherwise specified

Parameter	Symbol	1701A Min	1701A Typ	1701A Max	1701B Min	1701B Typ	1701B Max	1701 Min	1701 Typ	1701 Max	1701G Min	1701G Typ	1701G Max	Unit	Test Conditions
Supply Voltage	V_S V^+	±1.0 2.0		±5.0 10.0	±1.0 2.0		±5.0 10.0	±1.0 2.0		±5.0 10.0	±1.0 2.0		±5.0 10.0	 V	Dual Supply Single Supply
Input Offset Voltage	V_{OS}			0.9 1.7			2.0 2.8			4.5 5.3			10.0 11.0	mV mV	$R_S \leq$ 100KΩ 0°C $\leq T_A \leq$ +70°C
Input Offset Current	I_{OS}		1.0	25 240		1.0	25 240		1.0	25 240		1.0	30 450	pA pA	T_A = 25°C 0°C $\leq T_A \leq$ +70°C
Input Bias Current	I_B		1.0	30 300		1.0	30 300		1.0	30 300		1.0	50 600	pA pA	T_A = 25°C 0°C $\leq T_A \leq$ +70°C
Input Voltage Range	V_{IR}	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	V V	V^+ = +5V V_S = ±2.5V
Input Resistance	R_{IN}		10^{12}			10^{12}			10^{12}			10^{12}		Ω	
Input Offset Voltage Drift	TCV_{OS}		7			7			7			7		µV/°C	$R_S \leq$ 100KΩ
Power Supply Rejection Ratio	PSRR	70 70	80 80		65 65	80 80		65 65	80 80		60 60	80 80		dB dB	$R_S \leq$ 100KΩ 0°C $\leq T_A \leq$ +70°C
Common Mode Rejection Ratio	CMRR	70 70	83 83		65 65	83 83		65 65	83 83		60 60	83 83		dB dB	$R_S \leq$ 100KΩ 0°C $\leq T_A \leq$ +70°C
Large Signal Voltage Gain	A_V	40 20	100 1000		32 20	100 1000		32 20	100 1000		20 10	80 1000		V/ mV V/ mV V/ mV	R_L = 100KΩ $R_L \geq$ 1MΩ R_L = 100KΩ 0°C $\leq T_A \leq$ +70°C
Output Voltage Range	V_O low V_O high	 4.99	0.001 4.999	0.01	 4.99	0.001 4.999	0.01	 4.99	0.001 4.999	0.01	 4.99	0.001 4.999	0.01	V V	R_L =1MΩ V^+ = +5V 0°C $\leq T_A \leq$ +70°C
	V_O low V_O high	 2.40	-2.48 2.48	-2.40	 2.40	-2.48 2.48	-2.40	 2.40	-2.48 2.48	-2.40	 2.40	-2.48 2.48	-2.40	V V	R_L =100KΩ 0°C $\leq T_A \leq$ +70°C
Output Short Circuit Current	I_{SC}		1			1			1			1		mA	
Supply Current	I_S		120	250		120	250		120	250		120	300	µA	V_{IN} = 0V No Load
Power Dissipation	P_D			1.25			1.25			1.25			1.50	mW	V_S = ±2.5V

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

$T_A = 25^{\circ}C$ $V_S = \pm 2.5V$ unless otherwise specified

Parameter	Symbol	1701A			1701B			1701			1701G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C_{IN}		1			1			1			1		pF	
Bandwidth	B_W	400	700		400	700		400	700			700		KHz	
Slew Rate	S_R	0.33	0.7		0.33	0.7		0.33	0.7			0.7		V/μs	$A_V = +1$ $R_L = 100K\Omega$
Rise time	t_r		0.2			0.2			0.2			0.2		μs	$R_L = 100K\Omega$
Overshoot Factor			20			20			20			20		%	$R_L = 100K\Omega$ $C_L = 50pF$
Settling Time	t_s		10.0			10.0			10.0			10.0		μs	0.1% $A_V = -R_L = 100K\Omega$ $C_L = 50pF$

$T_A = 25^{\circ}C$ $V_S = \pm 5.0V$ unless otherwise specified

Parameter	Symbol	1701A			1701B			1701			1701G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		83			83			83			83		dB	$R_S \leq 100K\Omega$
Common Mode Rejection Ratio	CMRR		83			83			83			83		dB	$R_S \leq 100K\Omega$
Large Signal Voltage Gain	A_V		250			250			250			250		V/mV	$R_L = 100K\Omega$
Output Voltage Range	V_O low V_O high	 4.90	-4.98 4.98	-4.90	 4.90	-4.98 4.98	-4.90	 4.90	-4.98 4.98	-4.90	 4.90	-4.98 4.98	-4.90	V V	$R_L = 100K\Omega$
Bandwidth	B_W		1.0			1.0			1.0			1.0		MHz	
Slew Rate	S_R		1.0			1.0			1.0			1.0		V/μs	$A_V = +1$ $C_L = 50pF$

$V_S = \pm 2.5V$ $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified

Parameter	Symbol	1701BDA			1701DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			3.0			6.5	mV	$R_S \leq 100K\Omega$
Input Offset Current	I_{OS}			8.0			8.0	nA	
Input Bias Current	I_B			10.0			10.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		dB	$R_S \leq 100K\Omega$
Common Mode Rejection Ratio	CMRR	60	83		60	83		dB	$R_S \leq 100K\Omega$
Large Signal Voltage Gain	A_V	15	50		15	50		V/ mV	$R_L = 100K\Omega$
Output Voltage Range	V_O low V_O high	 2.35	-2.47 2.45	-2.40	 2.35	-2.47 2.45	-2.40	V V	 $R_L = 100K\Omega$

Design & Operating Notes:

1. The ALD1701A/ALD1701B/ALD1701/ALD1701G CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1701A/ALD1701B/ ALD1701/ALD1701G is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency.

2. The ALD1701A/ALD1701B/ALD1701/ALD1701G has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V below the positive supply voltage. Since offset voltage trimming on the ALD1701A/ALD1701B/ALD1701/ALD1701G is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. The user should however, be aware that this switching does take place if the operational amplifier is connected as a unity gain buffer, and should make provision in his design to allow for input offset voltage variations.

3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{12}\Omega$ would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.

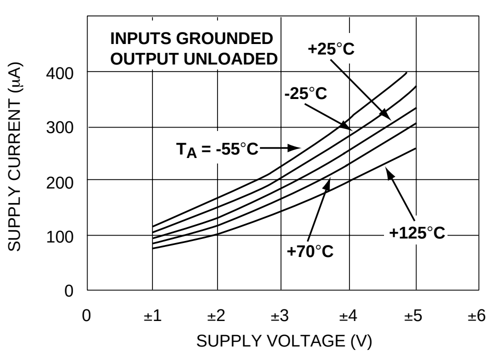
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.

5. The ALD1701A/ALD1701B/ALD1701/ALD1701G operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with any input voltages applied, and to limit input voltages not to exceed 0.3V of the power supply voltage levels.

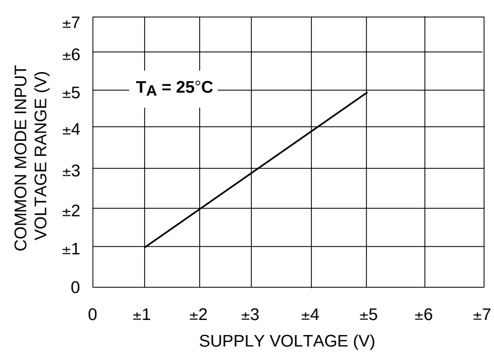
6. The ALD1701A/ALD1701B/ALD1701/ALD1701G, with its micropower operation, offers numerous benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to only 0.1°C above ambient temperature under most operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

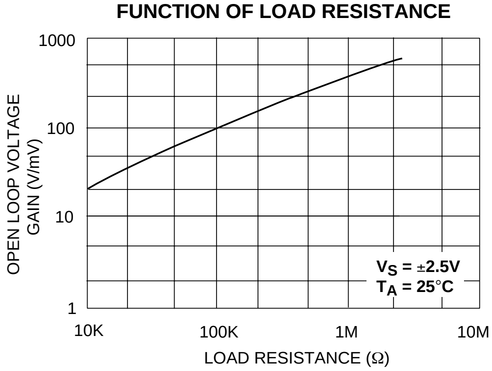
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



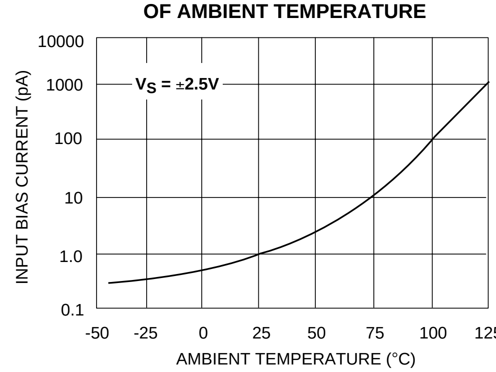
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE

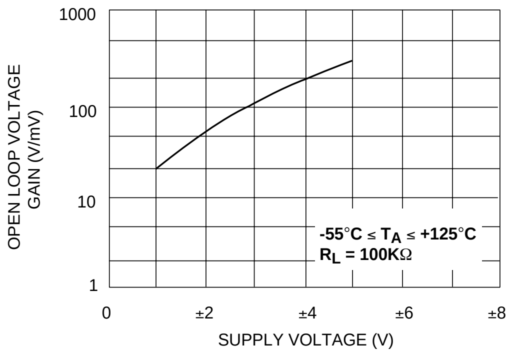


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

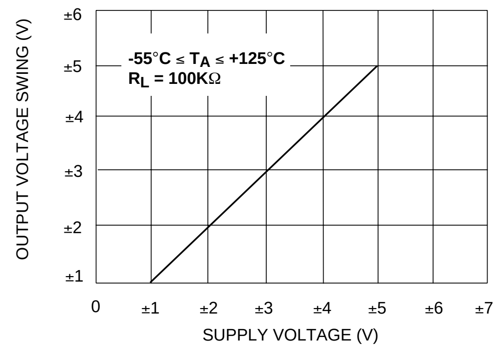


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

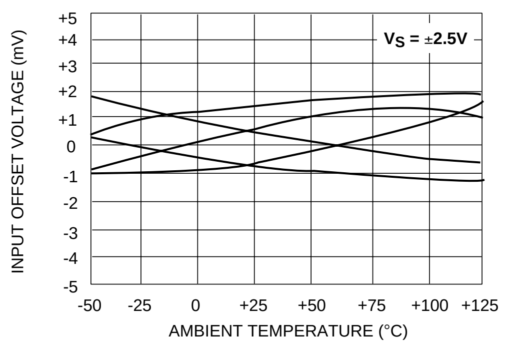
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



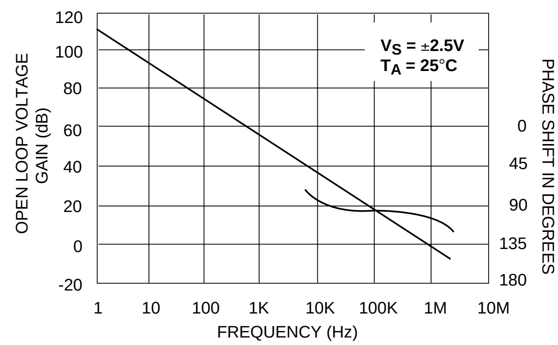
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



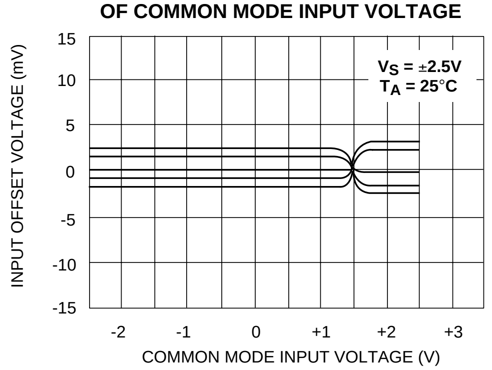
INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS



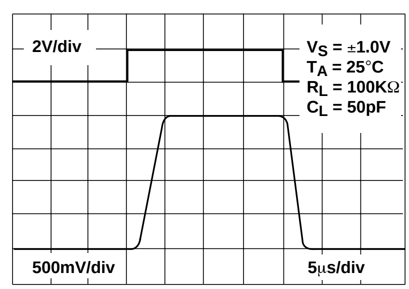
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



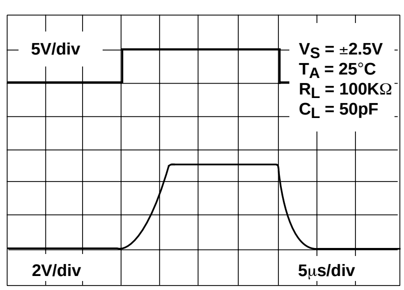
INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE



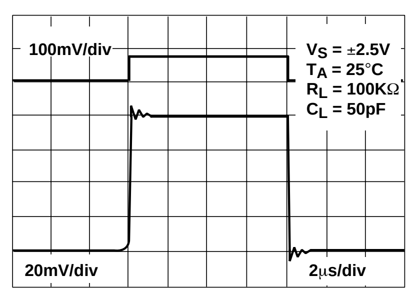
LARGE - SIGNAL TRANSIENT RESPONSE



LARGE - SIGNAL TRANSIENT RESPONSE

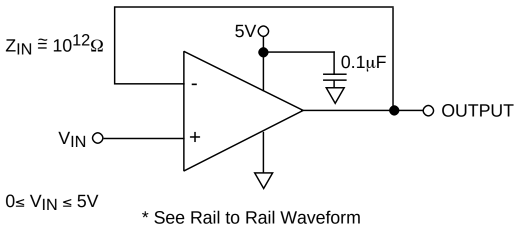


SMALL - SIGNAL TRANSIENT RESPONSE



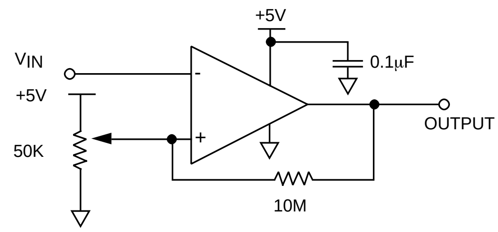
TYPICAL APPLICATIONS

RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER

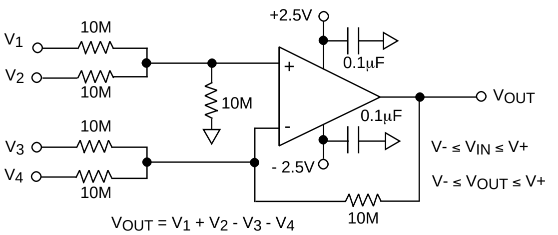


* See Rail to Rail Waveform

RAIL-TO-RAIL VOLTAGE COMPARATOR



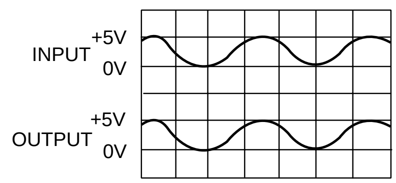
HIGH INPUT IMPEDANCE RAIL-TO-RAIL PRECISION DC SUMMING AMPLIFIER



$V_{OUT} = V_1 + V_2 - V_3 - V_4$

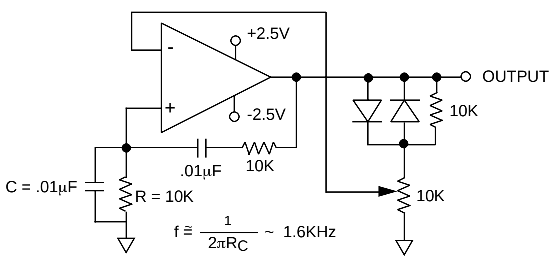
$R_{IN} = 10M\Omega$ Accuracy limited by resistor tolerances and input offset voltage

RAIL-TO-RAIL WAVEFORM



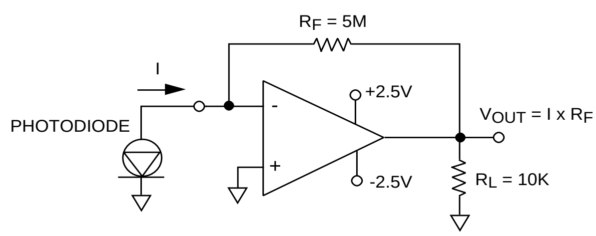
Performance waveforms.
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-rail voltage follower.

WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR

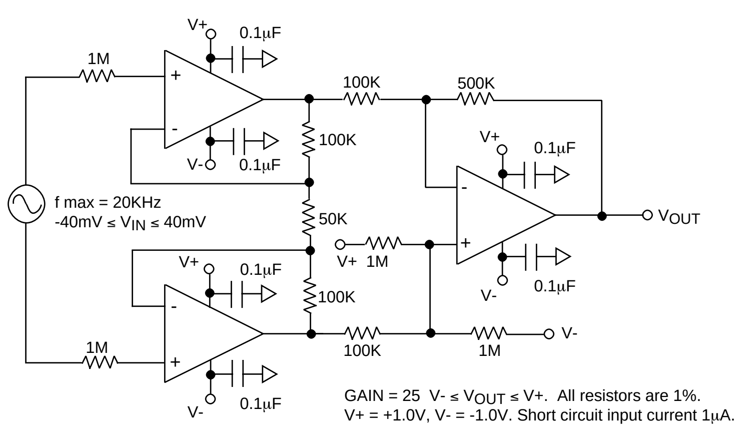


* See Rail to Rail Waveform

PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



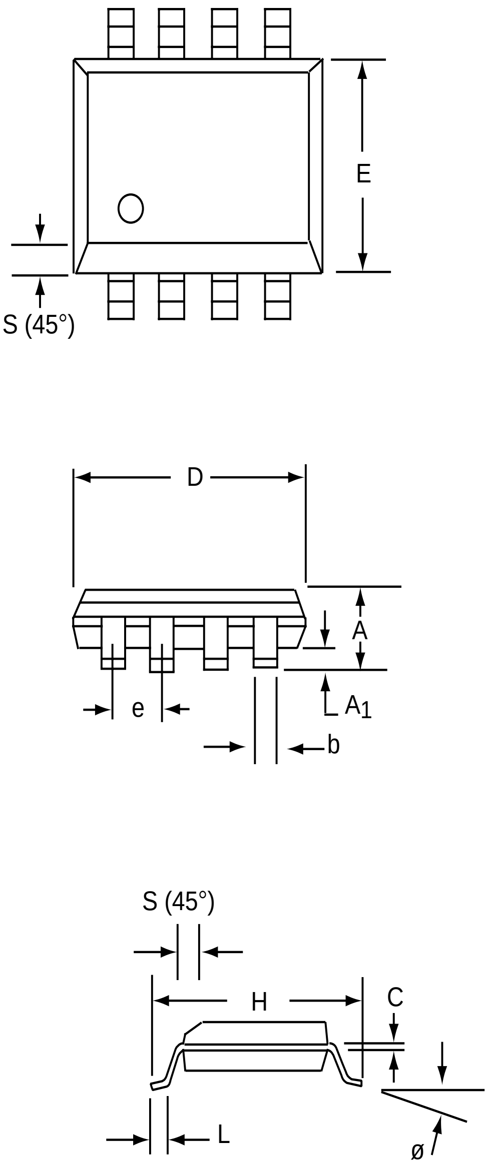
LOW VOLTAGE INSTRUMENTATION AMPLIFIER



GAIN = 25 $V- \leq V_{OUT} \leq V+$. All resistors are 1%.
V+ = +1.0V, V- = -1.0V. Short circuit input current 1μA.

SOIC-8 PACKAGE DRAWING

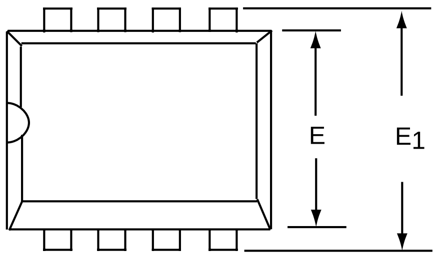
8 Pin Plastic SOIC Package



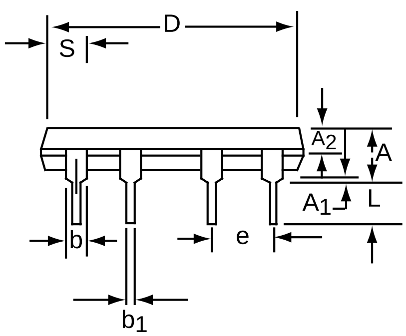
Dim	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A_1	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

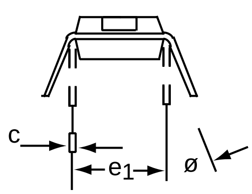
PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package



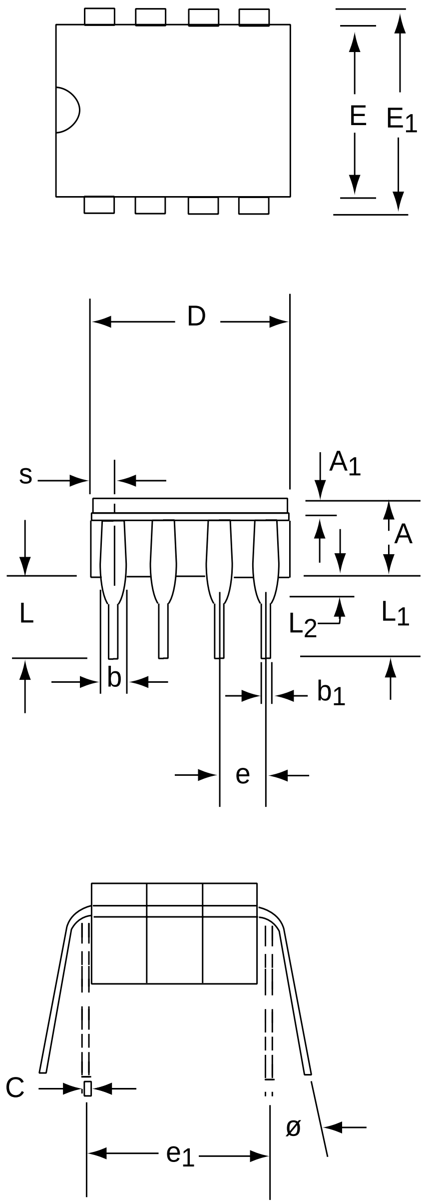
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A_1	0.38	1.27	0.015	0.050
A_2	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b_1	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E_1	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e_1	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
ø	0°	15°	0°	15°





CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A_1	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b_1	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E_1	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e_1	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L_1	3.18	--	0.125	--
L_2	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°