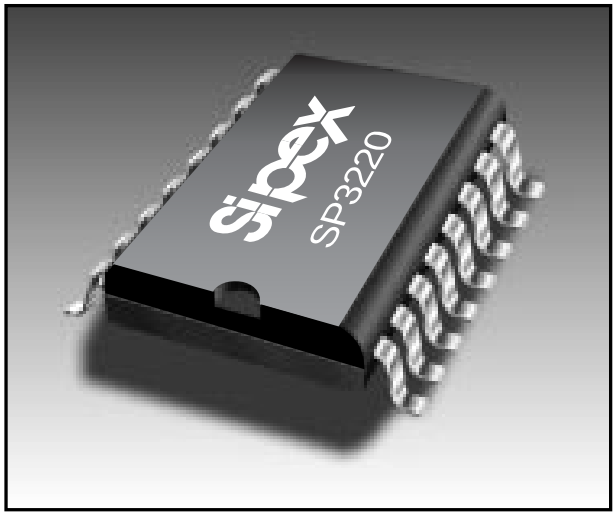
+3.0V to +5.5V RS-232 Driver/Receiver Pair

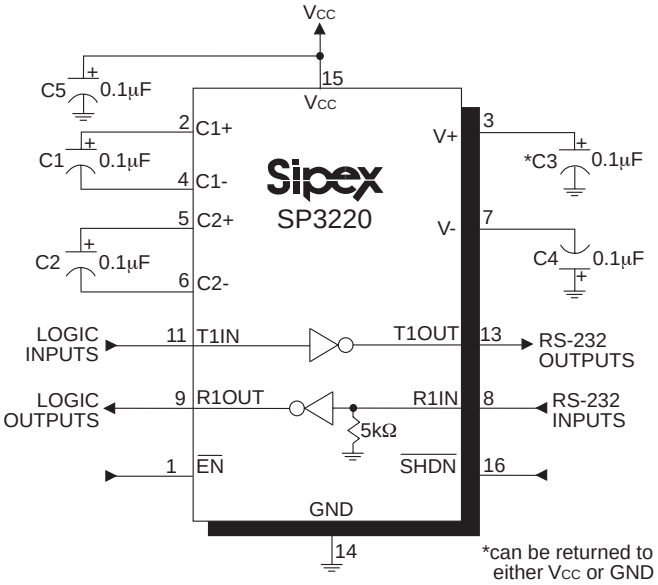
- Meets True RS-232 Protocol Operation From A +3.0V to +5.5V Power Supply
- Minimum 120 Kbps Data Rate Under Full Load
- 1μA Low-Power Shutdown With Receivers Active
- Interoperable With RS-232 Down To +2.7V Power Source
- Pin-Compatible With The **MAX3221E** Device Without The *AUTO ON-LINE®* Feature
- ESD Specifications: ±2kV Human Body Model



DESCRIPTION

The **SP3220** device is an RS-232 driver/receiver solution intended for portable or hand-held applications such as notebook or palmtop computers. The **SP3220** device has a high-efficiency, charge-pump power supply that requires only 0.1μF capacitors in 3.3V operation. This charge pump allows the **SP3220** device to deliver true RS-232 performance from a single power supply ranging from +3.3V to +5.0V.

The **SP3220** device has a low-power shutdown mode where the driver outputs and charge pumps are disabled. During shutdown, the supply current falls to less than 1μA.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC} ..... -0.3V to +6.0V
V+ (NOTE 1) ..... -0.3V to +7.0V
V- (NOTE 1) ..... +0.3V to -7.0V
V+ + |V-| (NOTE 1) ..... +13V

I_{CC} (DC V_{CC} or GND current) ..... ±100mA

Input Voltages
TxIN, EN ..... -0.3V to +6.0V
RxIN ..... ±15V

Output Voltages
TxOUT ..... ±15.0V
RxOUT ..... -0.3V to +6.0V

Short-Circuit Duration
TxOUT ..... Continuous

Storage Temperature ..... -65°C to +150°C

Power Dissipation Per Package
16-pin SSOP (derate 9.69mW/°Cabove+70°C) 775mW
16-pin TSSOP (derate 10.5mW/°C above +70°C) 840mW
16-pin Wide SOIC (derate 11.2mW/°C above+70°C) 900mW

NOTE 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = T_{MIN} to T_{MAX}.
Typical Values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25°C.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current		0.3	1.0	mA	no load, T_{AMB} = +25°C, V_{CC} = 3.3V
Shutdown Supply Current		1.0	10	µA	$\overline{SHDN}$ = GND, T_{AMB} = +25°C, V_{CC} = +3.3V
LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold LOW			0.8	V	TxIN, $\overline{EN}$, $\overline{SHDN}$, Note 2
Input Logic Threshold HIGH	2.0 2.4			V	V_{CC} = 3.3V, Note 2 V_{CC} = 5.0V, Note 2
Input Leakage Current		±0.01	±1.0	µA	TxIN, $\overline{EN}$, $\overline{SHDN}$, T_{AMB} = +25°C
Output Leakage Current		±0.05	±10	µA	receivers disabled
Output Voltage LOW			0.4	V	I_{OUT} = 1.6mA
Output Voltage HIGH	V_{CC}-0.6	V_{CC}-0.1		V	I_{OUT} = -1.0mA
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±5.4		V	3kΩ load to ground at all driver outputs, T_{AMB} = +25°C
Output Resistance	300			Ω	V_{CC} = V+ = V- = 0V, T_{OUT} = ±2V
Output Short-Circuit Current		±35 ±70	±60 ±100	mA mA	V_{OUT} = 0V V_{OUT} = ±15V
Output Leakage Current			±25	µA	V_{OUT} = ±12V, V_{CC} = 0V to 5.5V, drivers disabled

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{CC} = +3.0V to +5.0V with T_{AMB} = T_{MIN} to T_{MAX}.
Typical Values apply at V_{CC} = +3.3V or +5.0V and T_{AMB} = 25ºC.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.6 0.8	1.2 1.5		V	V_{CC}=3.3V V_{CC}=5.0V
Input Threshold HIGH		1.5 1.8	2.4 2.4	V	V_{CC}=3.3V V_{CC}=5.0V
Input Hysteresis		0.3		V	
Input Resistance	3	5	7	kΩ	
TIMING CHARACTERISTICS					
Maximum Data Rate	120	235		kbps	R_L=3kΩ, C_L=1000pF, one driver switching
Driver Propagation Delay		1.0 1.0		µs µs	t_{PHL}, R_L = 3KΩ, C_L = 1000pF t_{PLH}, R_L = 3KΩ, C_L = 1000pF
Receiver Propagation Delay		0.3 0.3		µs	t_{PHL}, RxIN to RxOUT, C_L=150pF t_{PLH}, RxIN to RxOUT, C_L=150pF
Receiver Output Enable Time		200		ns	
Receiver Output Disable Time		200		ns	
Driver Skew		100	500	ns	$\lvert t_{PHL} - t_{PLH} \rvert$, T_{AMB} = 25ºC
Receiver Skew		200	1000	ns	$\lvert t_{PHL} - t_{PLH} \rvert$
Transition-Region Slew Rate			30	V/µs	V_{CC} = 3.3V, R_L = 3KΩ, T_{AMB} = 25ºC, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V

NOTE 2: Driver input hysteresis is typically 250mV.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, the following performance characteristics apply for V_{CC} = +3.3V, 120kbps data rates, all drivers loaded with 3kΩ, 0.1µF charge pump capacitors, and T_{AMB} = +25°C.

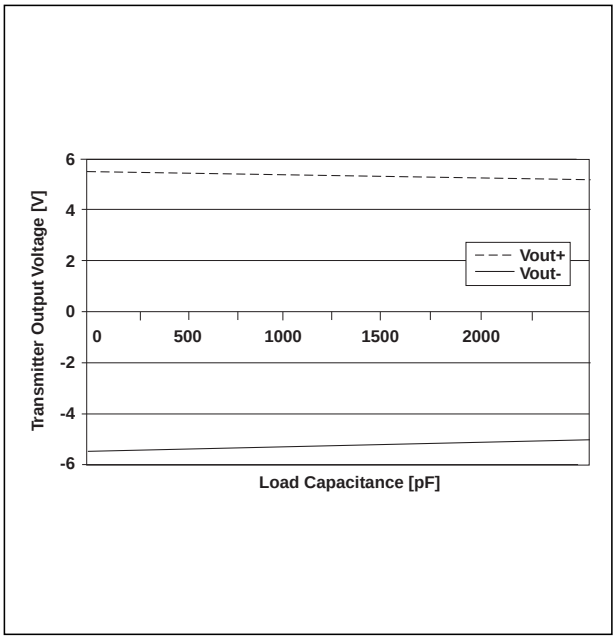


Figure 1. Transmitter Output Voltage VS. Load Capacitance for the SP3220

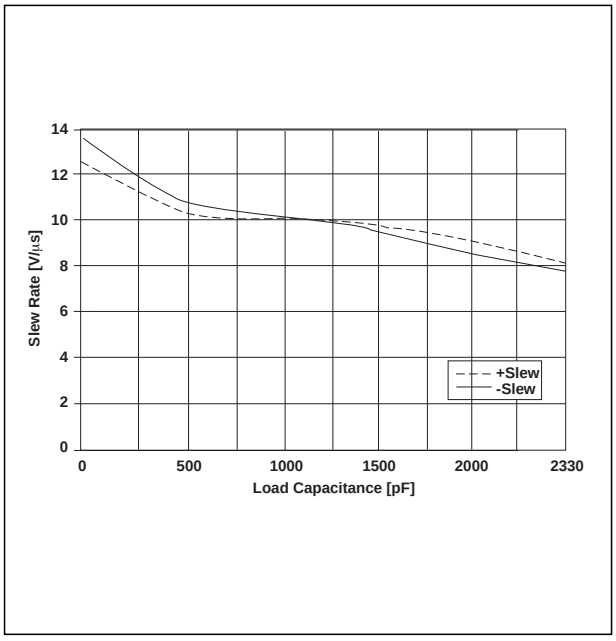


Figure 2. Slew Rate VS. Load Capacitance for the SP3220

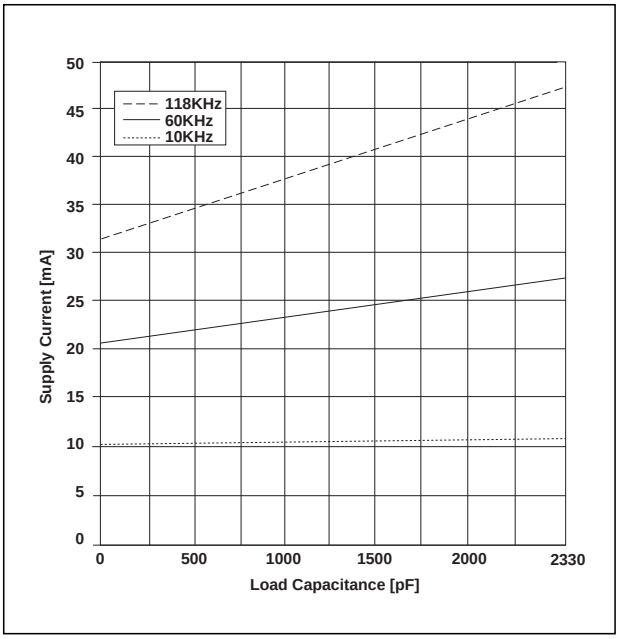


Figure 3. Supply Current VS. Load Capacitance when Transmitting Data for the SP3220

NAME	FUNCTION	PIN NUMBER
$\overline{EN}$	Receiver Enable Control. Drive LOW for normal operation. Drive HIGH to Tri-State the receiver outputs (high-Z state).	1
C1+	Positive terminal of the voltage doubler charge-pump capacitor.	2
V+	+5.5V generated by the charge pump.	3
C1-	Negative terminal of the voltage doubler charge-pump capacitor.	4
C2+	Positive terminal of the inverting charge-pump capacitor.	5
C2-	Negative terminal of the inverting charge-pump capacitor.	6
V-	-5.5V generated by the charge pump.	7
R1IN	RS-232 receiver input.	8
R1OUT	TTL/CMOS reciever output.	9
N.C.	No Connect.	10, 12
T1IN	TTL/CMOS driver input.	11
T1OUT	RS-232 driver output.	13
GND	Ground.	14
V_{CC}	+3.0V to +5.5V supply voltage	15
$\overline{SHDN}$	Shutdown Control Input. Drive HIGH for normal device operation. Drive LOW to shutdown the drivers (high-Z output) and the on-board charge pump power supply.	16

Table 1. Device Pin Description

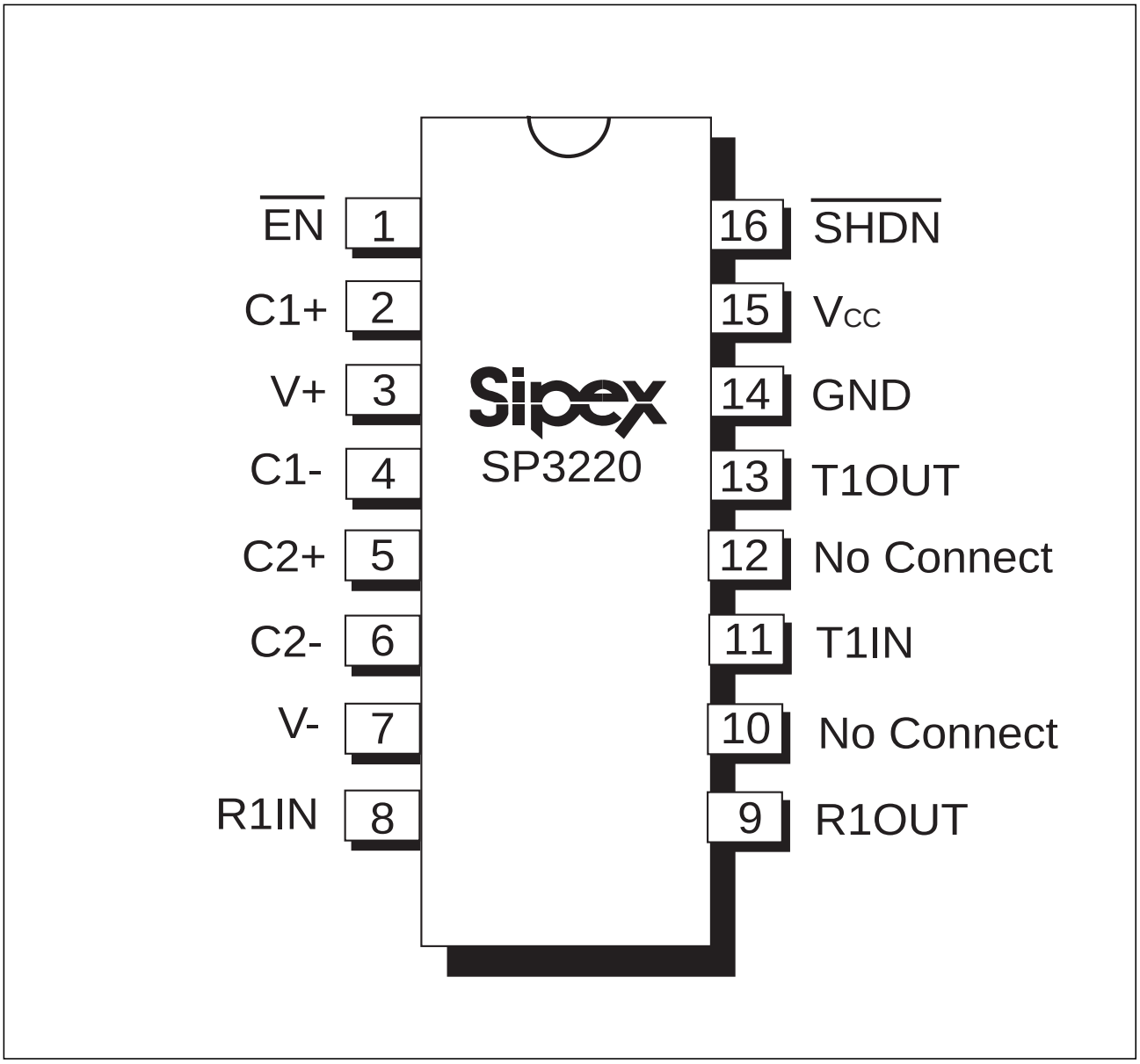


Figure 4. Pinout Configurations for the SP3220

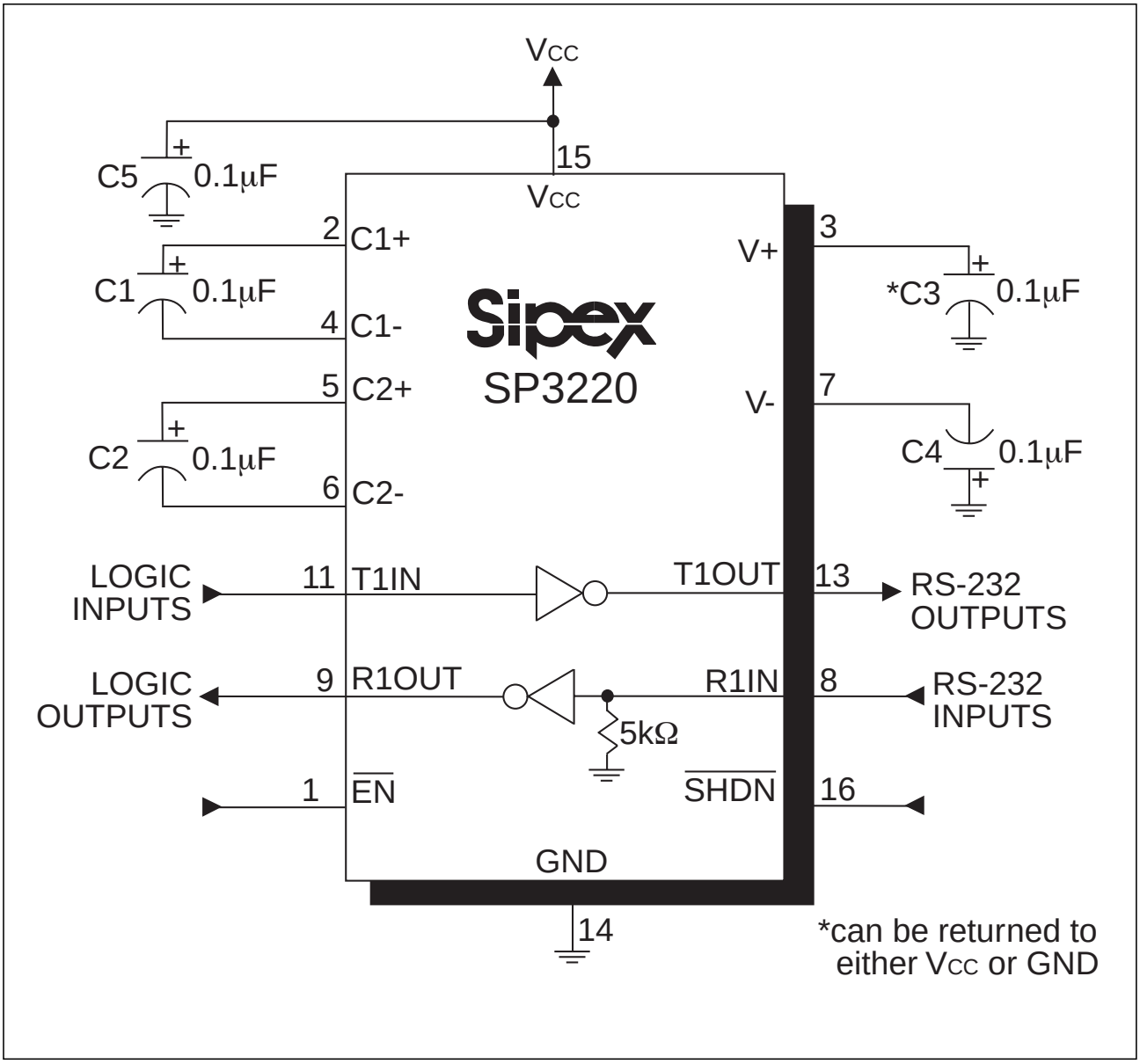


Figure 5. SP3220 Typical Operating Circuits

DESCRIPTION

The **SP3220** device meets the EIA/TIA-232 and V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The **SP3220** device features **Sipex's** proprietary on-board charge pump circuitry that generates 2 x V_{CC} for RS-232 voltage levels from a single +3.0V to +5.5V power supply. This series is ideal for +3.3V-only systems, mixed +3.0V to +5.5V systems, or +5.0V-only systems that require true RS-232 performance. The **SP3220** device has a driver that operates at a typical data rate of 235Kbps fully loaded.

The **SP3220** is a 1-driver/1-receiver device ideal for portable or hand-held applications. The **SP3220** features a 1µA shutdown mode that reduces power consumption and extends battery life in portable systems. Its receivers remain active in shutdown mode, allowing external devices such as modems to be monitored using only 1µA supply current.

THEORY OF OPERATION

The **SP3220** device is made up of three basic circuit blocks: 1. Drivers, 2. Receivers, and 3. the Sipex proprietary charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to ±5.0V EIA/TIA-232 levels inverted relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.5V with no load and at least ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. Driver outputs will meet EIA/TIA-562 levels of ±3.7V with supply voltages as low as 2.7V.

The drivers typically can operate at a data rate of 235Kbps. The drivers can guarantee a data rate of 120Kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software.

The slew rate of the driver output is internally limited to a maximum of 30V/µs in order to meet the EIA standards (EIA RS-232D 2.1.7, Paragraph 5). The transition of the loaded output from HIGH to LOW also meets the monotonicity requirements of the standard.

The **SP3220** driver can maintain high data rates up to 235Kbps fully loaded. *Figure 6* shows a loopback test circuit used to test the RS-232 driver. *Figure 7* shows the test results of the loopback circuit with the driver active at 120Kbps with an RS-232 load in parallel with a 1000pF capacitor. *Figure 8* shows the test results where the driver was active at 235Kbps and loaded with an RS-232 receiver in parallel with a 1000pF capacitor. A solid RS-232 data transmission rate of 120Kbps provides compatibility with many designs in personal computer peripherals and LAN applications.

The **SP3220** driver's output stage is turned off (high-Z) when the device is in shutdown mode. When the power is off, the **SP3220** device permits the outputs to be driven up to ±12V. The driver's input does not have pull-up resistors. Designers should connect an unused input to V_{CC} or GND.

In the shutdown mode, the supply current falls to less than 1µA, where $\overline{SHDN}$ = LOW. When the **SP3220** device is shut down, the device's driver output is disabled (high-Z) and the charge pump is turned off with V+ pulled down to V_{CC} and V- pulled to GND. The time required to exit shutdown is typically 100µs. Connect $\overline{SHDN}$ to V_{CC} if the shutdown mode is not used. $\overline{SHDN}$ has no effect on RxOUT. Note that the driver is enabled only when the magnitude of V- exceeds approximately 3V.

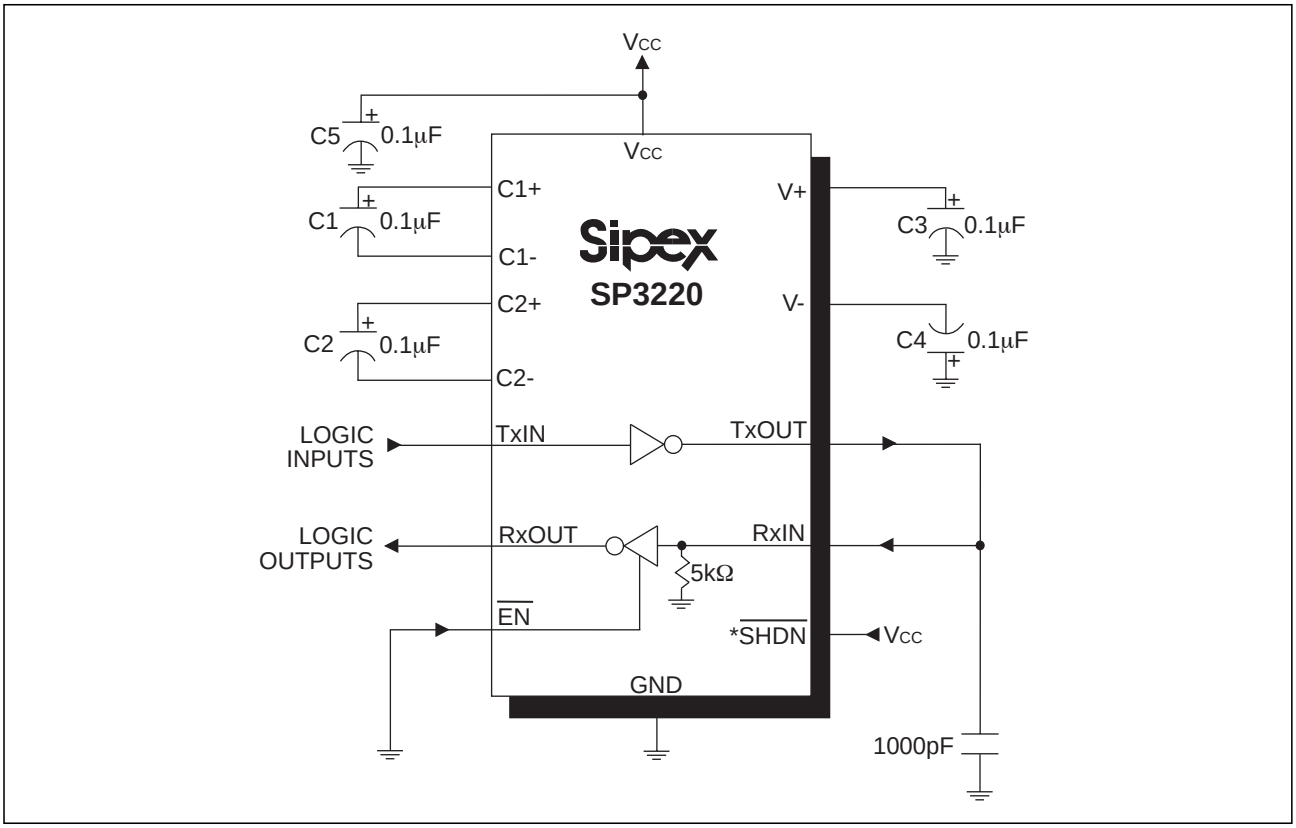


Figure 6. SP3220 Driver Loopback Test Circuit

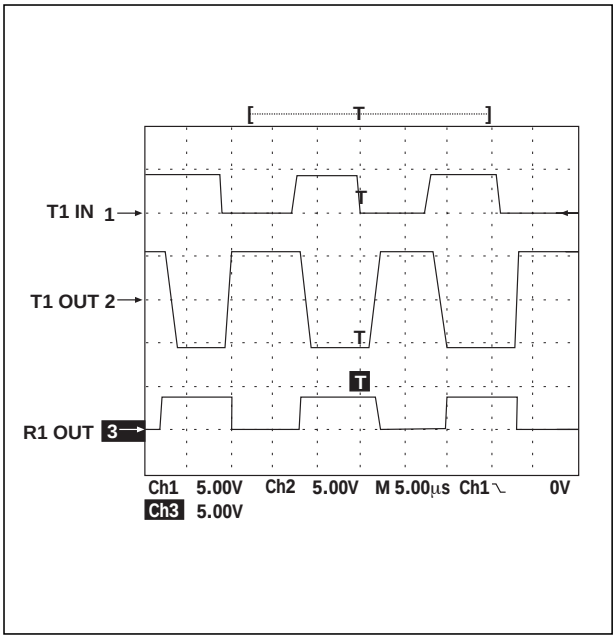


Figure 7. Driver Loopback Test Results at 120kbps

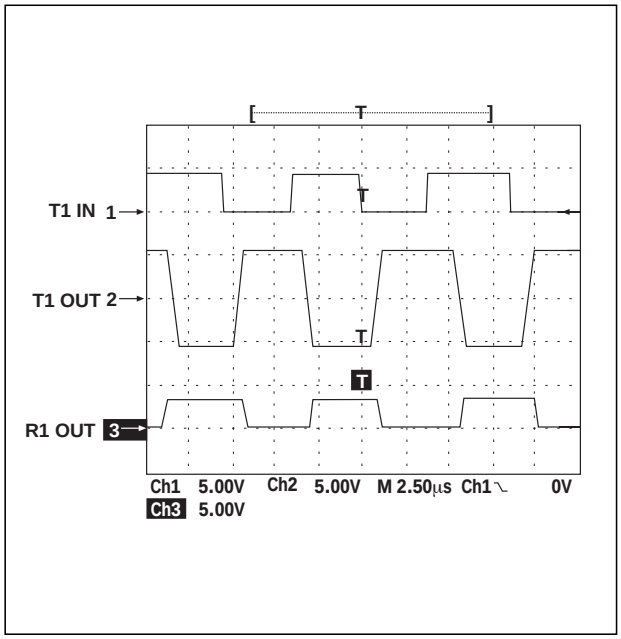


Figure 8. Driver Loopback Test Results at 235kbps

Receivers

The receiver converts EIA/TIA-232 levels to TTL or CMOS logic output levels. The receiver has an inverting high-impedance output. This receiver output (RxOUT) is at high-impedance when the enable control $\overline{EN}$ = HIGH. In the shutdown mode, the receiver can be active or inactive. $\overline{EN}$ has no effect on TxOUT. The truth table logic of the **SP3220** driver and receiver outputs can be found in *Table 2*.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, a 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

Charge Pump

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (V_{CC}) over the +3.0V to +5.5V range.

$\overline{SHDN}$	$\overline{EN}$	TxOUT	RxOUT
0	0	Tri-state	Active
0	1	Tri-state	Tri-state
1	0	Active	Active
1	1	Active	Tri-state

Table 2. Truth Table Logic for Shutdown and Enable Control

In most circumstances, decoupling the power supply can be achieved adequately using a 0.1µF bypass capacitor at C5 (refer to *Figures 5*). In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as charge-pump capacitor C1. Physically connect bypass capacitors as close to the IC as possible.

The charge pumps operate in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pumps are enabled. If the output voltage exceed a magnitude of 5.5V, the charge pumps are disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to V_{CC}. C_1^+ is then switched to GND and the charge in C_1^- is transferred to C_2^-. Since C_2^+ is connected to V_{CC}, the voltage potential across capacitor C_2 is now 2 times V_{CC}.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to GND. This transfers a negative generated voltage to C_3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C_3, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces $-V_{CC}$ in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at V_{CC}, the voltage potential across C_2 is 2 times V_{CC}.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to GND, and transfers this positive generated voltage across C_2 to C_4, the V_{DD} storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C_4, the positive side of capacitor C_1 is switched to V_{CC} and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

Since both V^+ and V^- are separately generated from V_{CC}; in a no–load condition V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 250kHz. The external capacitors can be as low as 0.1µF with a 16V breakdown voltage rating.

ESD Tolerance

The **SP3220** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 14*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively.

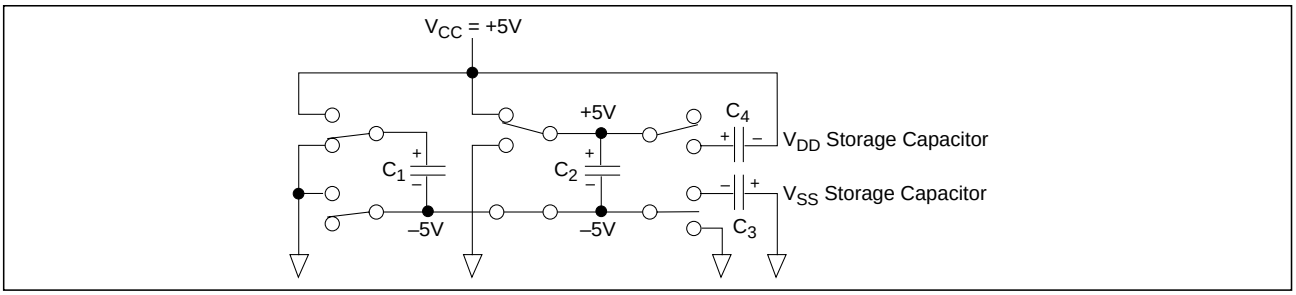


Figure 9. Charge Pump — Phase 1

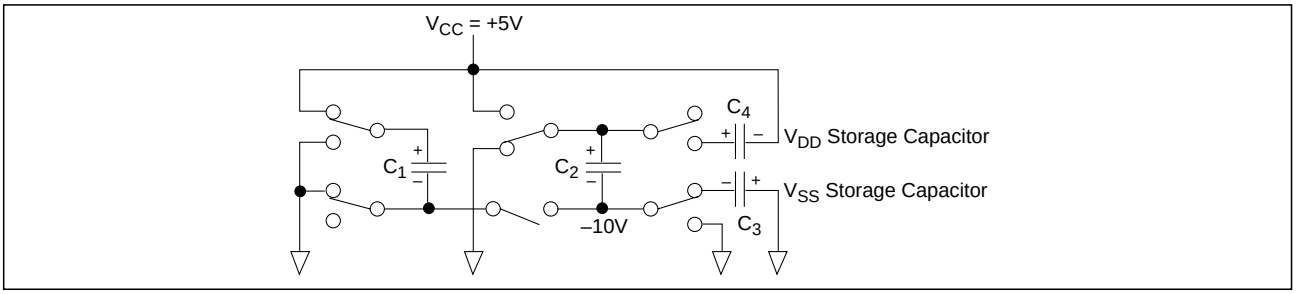


Figure 10. Charge Pump — Phase 2

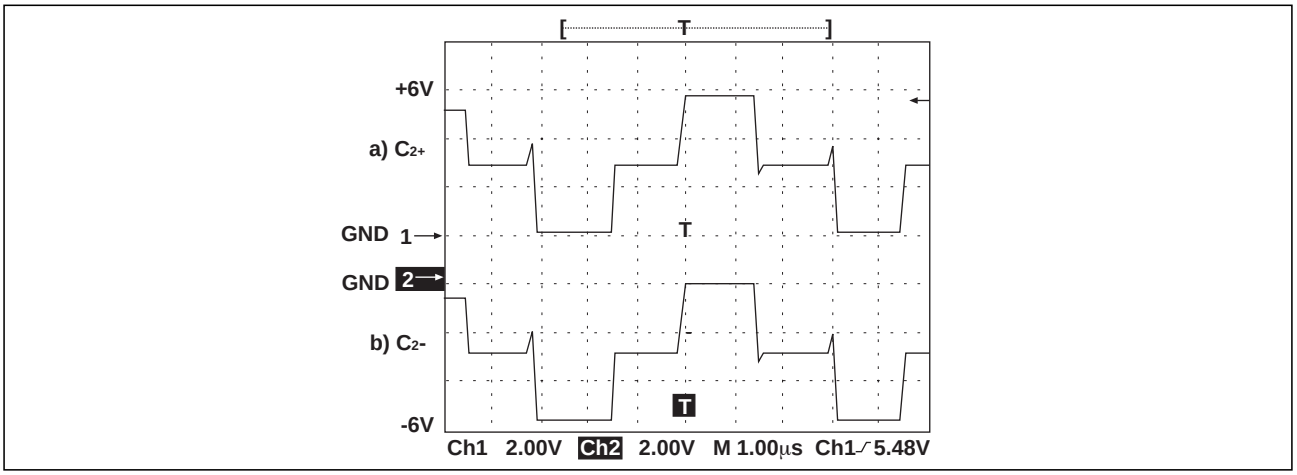


Figure 11. Charge Pump Waveforms

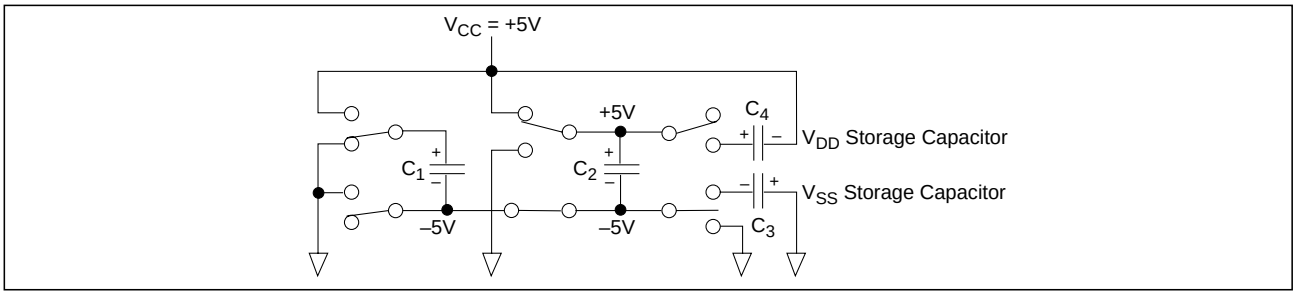


Figure 12. Charge Pump — Phase 3

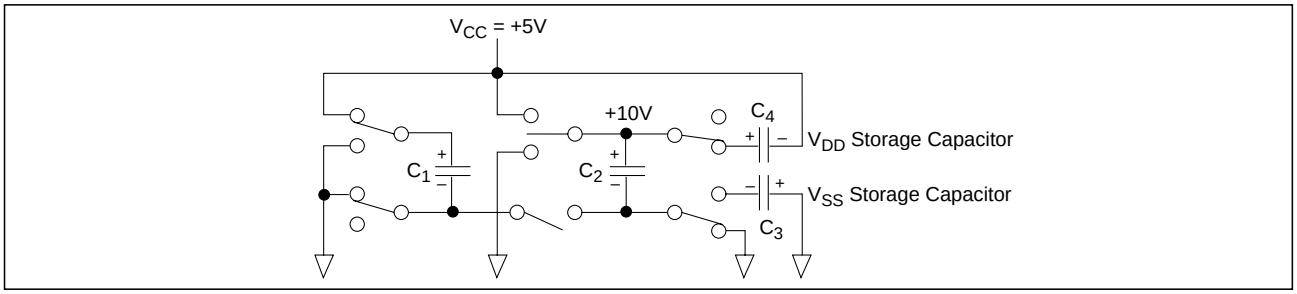


Figure 13. Charge Pump — Phase 4

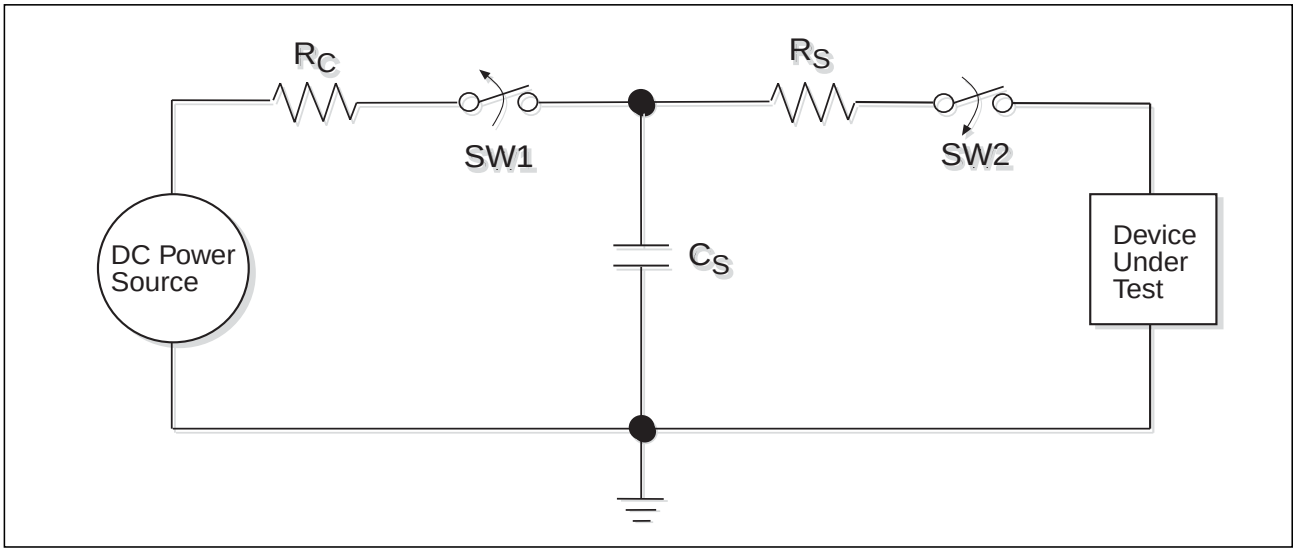
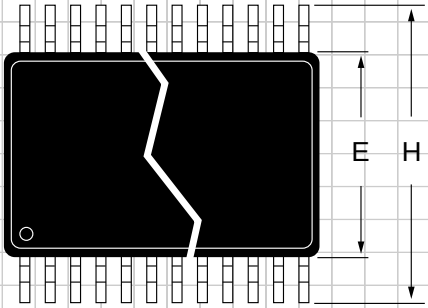
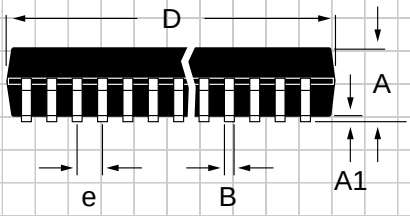
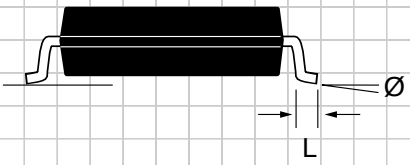


Figure 14. ESD Test Circuit for Human Body Model

PACKAGE: PLASTIC SHRINK SMALL OUTLINE (SSOP)

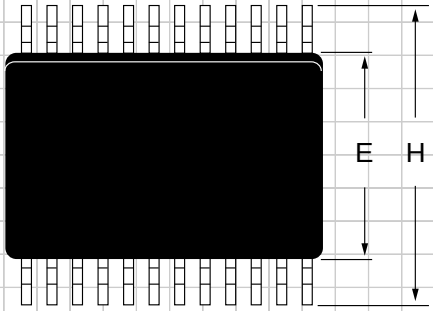


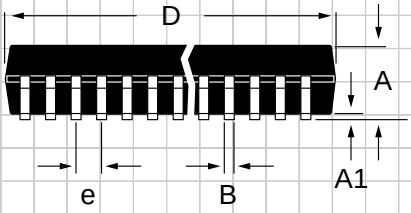


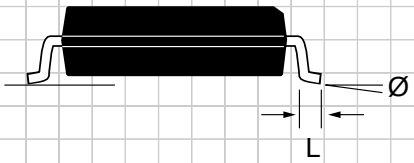


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	20–PIN	24–PIN	28–PIN
A	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)	0.068/0.078 (1.73/1.99)
A1	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)	0.002/0.008 (0.05/0.21)
B	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)	0.010/0.015 (0.25/0.38)
D	0.239/0.249 (6.07/6.33)	0.278/0.289 (7.07/7.33)	0.317/0.328 (8.07/8.33)	0.397/0.407 (10.07/10.33)
E	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)	0.205/0.212 (5.20/5.38)
e	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)	0.0256 BSC (0.65 BSC)
H	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)	0.301/0.311 (7.65/7.90)
L	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)	0.022/0.037 (0.55/0.95)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC SMALL OUTLINE (SOIC)

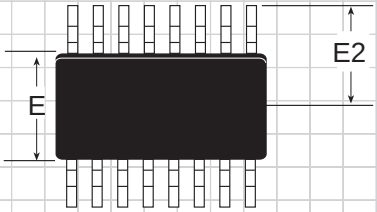


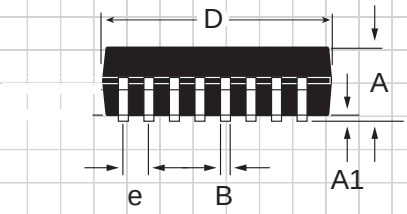


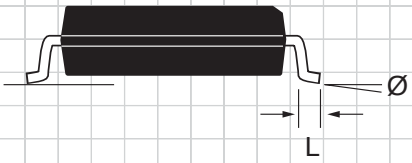


DIMENSIONS (Inches) Minimum/Maximum (mm)	16–PIN	18–PIN
A	0.090/0.104 (2.29/2.649)	0.090/0.104 (2.29/2.649))
A1	0.004/0.012 (0.102/0.300)	0.004/0.012 (0.102/0.300)
B	0.013/0.020 (0.330/0.508)	0.013/0.020 (0.330/0.508)
D	0.398/0.413 (10.10/10.49)	0.447/0.463 (11.35/11.74)
E	0.291/0.299 (7.402/7.600)	0.291/0.299 (7.402/7.600)
e	0.050 BSC (1.270 BSC)	0.050 BSC (1.270 BSC)
H	0.394/0.419 (10.00/10.64)	0.394/0.419 (10.00/10.64)
L	0.016/0.050 (0.406/1.270)	0.016/0.050 (0.406/1.270)
Ø	0°/8° (0°/8°)	0°/8° (0°/8°)

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)







DIMENSIONS in inches (mm) Minimum/Maximum	16–PIN	20–PIN
A	- /0.043 (- /1.10)	- /0.043 (- /1.10)
A1	0.002/0.006 (0.05/0.15)	0.002/0.006 (0.05/0.15)
B	0.007/0.012 (0.19/0.30)	0.007/0.012 (0.19/0.30)
D	0.193/0.201 (4.90/5.10)	0.252/0.260 (6.40/6.60)
E	0.169/0.177 (4.30/4.50)	0.169/0.177 (4.30/4.50)
e	0.026 BSC (0.65 BSC)	0.026 BSC (0.65 BSC)
E2	0.126 BSC (3.20 BSC)	0.126 BSC (3.20 BSC)
L	0.020/0.030 (0.50/0.75)	0.020/0.030 (0.50/0.75)
Ø	0°/8°	0°/8°

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP3220CA	0˚C to +70˚C	16-Pin SSOP
SP3220CT	0˚C to +70˚C	16-Pin Wide SOIC
SP3220CY	0˚C to +70˚C	16-Pin TSSOP
SP3220EA	-40˚C to +85˚C	16-Pin SSOP
SP3220ET	-40˚C to +85˚C	16-Pin Wide SOIC
SP3220EY	-40˚C to +85˚C	16-Pin TSSOP

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