AK5700

16-Bit ΔΣ Mono ADC with PLL & MIC-AMP

GENERAL DESCRIPTION

The AK5700 features a 16-bit mono ADC. Input circuits include a Microphone-Amplifier and an ALC (Auto Level Control) circuit that is suitable for portable application with recording function. On-chip PLL supports base-band clock of mobile phone, therefore it is easy to connect with DSP. The AK5700 is available in a 24pin QFN, utilizing less board space than competitive offerings.

FEATURES

1. **Resolution: 16bits**
2. **Recording Function**
   - **Input Selector**
   - **Full-differential or Single-ended Input**
   - **MIC Amplifier (+30dB/+15dB or 0dB)**
   - **Input Voltage: 1.8Vpp@AVDD=3.0V (= 0.6 x AVDD)**
   - **ADC Performance: S/(N+D): 78dB, DR, S/N: 89dB@MGAIN=0dB**
     S/(N+D): 77dB, DR, S/N: 87dB@MGAIN=+15dB
     S/(N+D): 72dB, DR, S/N: 77dB@MGAIN=+30dB
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
   - **Digital ALC (Automatic Level Control)**
     (+36dB ~ –54dB, 0.375dB Step, Mute)
3. **Sampling Rate:**
   - **PLL Slave Mode (EXLRCK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (EXBCLK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (MCKI pin):**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **PLL Master Mode:**
     8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
   - **EXT Slave Mode:**
     7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)
4. **PLL Input Clock:**
   - **MCKI pin:**
     27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz
   - **EXLRCK pin: 1fs**
   - **EXBCLK pin: 32fs/64fs**
5. **Master/Slave mode**
6. **Audio Interface Format: MSB First, 2's complement**
   - **DSP Mode, 16bit MSB justified, I^2S**
7. **μP I/F: 3-wire Serial**
8. **Power Supply:**
   - **AVDD: 2.4 ~ 3.6V**
   - **DVDD: 1.6 ~ 3.6V**
9. **Power Supply Current: 6mA**
10. **Ta = –30 ~ 85°C**
11. **Package: 24pin QFN (4mm x 4mm)**
12. **Pin and Register compatible with AK5701 Stereo Version**

■ Block Diagram

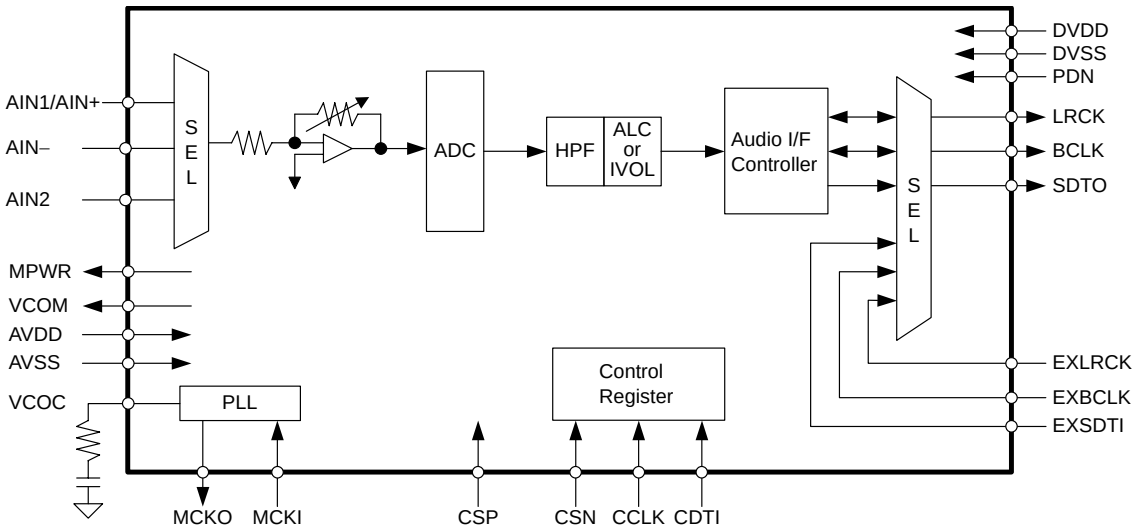
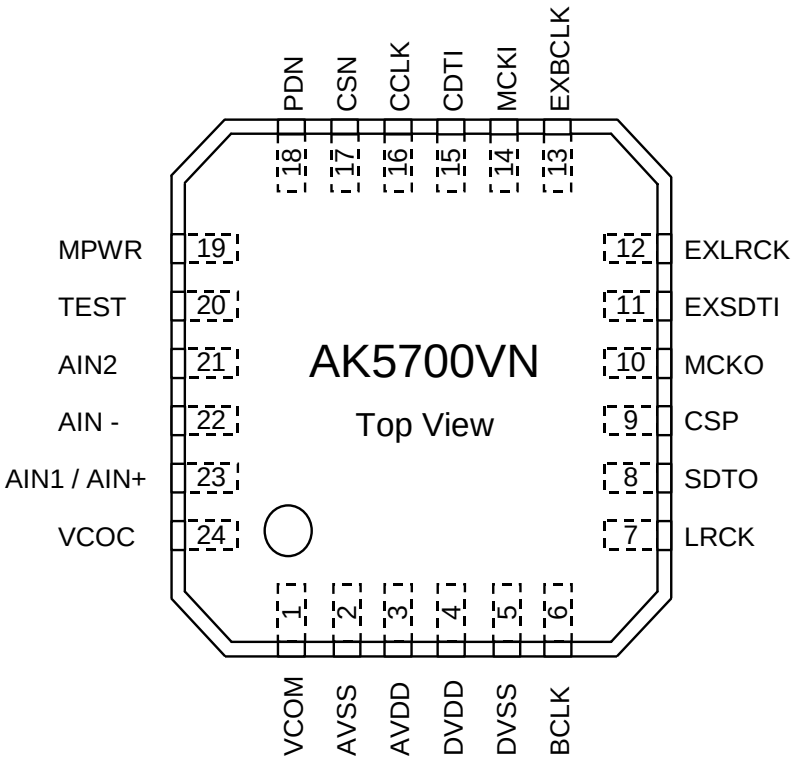


Figure 1. Block Diagram

■ Ordering Guide

AK5700VN	–30 ~ +85°C	24pin QFN (0.5mm pitch)
AKD5700	Evaluation board for AK5700	

■ Pin Layout



■ Comparison with AK5701VN

Function	AK5701VN	AK5700VN
ADC channel Number	2 channel	1channel
Input Selector	2 Stereo Input Selector	2 Mono Input Selector
Audio I/F Format	DSP Mode 0, DSP Mode 1, Left justified, I^2S	DSP Mode 0, Left justified, I^2S

PIN/FUNCTION

No.	Pin Name	I/O	Function
1	VCOM	O	Common Voltage Output Pin, 0.5 x AVDD Bias voltage of ADC inputs.
2	AVSS	-	Analog Ground Pin
3	AVDD	-	Analog Power Supply Pin
4	DVDD	-	Digital Power Supply Pin
5	DVSS	-	Digital Ground Pin
6	BCLK	O	Audio Serial Data Clock Pin
7	LRCK	O	Input / Output Channel Clock Pin
8	SDTO	O	Audio Serial Data Output Pin
9	CSP	I	Chip Select Polarity Pin "H": CSN pin = "H" active, C1-0 = "01" "L": CSN pin = "L" active, C1-0 = "10"
10	MCKO	O	Master Clock Output Pin
11	EXSDTI	I	External Audio Serial Data Input Pin
12	EXLRCK	I	External Input / Output Channel Clock Pin
13	EXBCLK	I	External Audio Serial Data Clock Pin
14	MCKI	I	External Master Clock Input Pin
15	CDTI	I	Control Data Input Pin
16	CCLK	I	Control Data Clock Pin (Internal Pull-down at CSP pin = "H")
17	CSN	I	Chip Select Pin
18	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, reset and initializes the control register.
19	MPWR	O	MIC Power Supply Pin
20	TEST	-	Test Pin This pin should be left floating.
21	AIN2	I	Analog Input 2 Pin
22	AIN–	I	Negative Input Pin
23	AIN1	I	Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input)
	AIN+	I	Positive Input Pin (MDIF1 bit = "1": Full-differential Input)
24	VCOC	O	Output Pin for Loop Filter of PLL Circuit This pin should be connected to AVSS with one resistor and capacitor in series.

Note 1. All input pins except analog input pins (AIN1, AIN1–, AIN2) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MPWR, VCOC, AIN1/AIN+, AIN–, AIN2	These pins should be open.
Digital	BCLK, LRCK, SDTO, MCKO	These pins should be open.
	MCKI, EXBCLK, EXLRCK, EXSDTI	These pins should be connected to DVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
	Digital	DVDD	–0.3	4.6	V
	|AVSS – DVSS| (Note 3)	ΔGND	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA	–0.3	AVDD+0.3	V
Digital Input Voltage (Note 5)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (powered applied)		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 2. All voltages with respect to ground.
Note 3. AVSS and DVSS must be connected to the same analog ground plane.
Note 4. AIN1/AIN+, AIN–, AIN2 pins
Note 5. PDN, CSN, CCLK, CDTI, CSP, MCKI, EXSDTI, EXLRCK, EXBCLK pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 2)

Parameter		Symbol	min	typ	Max	Units
Power Supplies	Analog	AVDD	2.4	3.0	3.6	V
(Note 6)	Digital	DVDD	1.6	3.0	AVDD	V

Note 2. All voltages with respect to ground.
Note 6. The power-up sequence between AVDD and DVDD is not critical. When only AVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD should not be powerd OFF while AVDD is powered ON.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3.0V; AVSS=DVSS=0V; PLL Master Mode; MCKI=12MHz, fs=44.0995kHz, BCLK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

Parameter		Min	Typ	max	Units
MIC Amplifier: AIN1, AIN2 pins; MDIF1 bit = "0" (Single-ended inputs)					
Input Resistance	MGAIN1-0 bits = "00"	40	60	80	kΩ
	MGAIN1-0 bits = "01" or "10"	20	30	40	kΩ
Gain	MGAIN1-0 bits = "00"	-	0	-	dB
	MGAIN1-0 bits = "01"	-	+15	-	dB
	MGAIN1-0 bits = "10"	-	+30	-	dB
MIC Amplifier: AIN+, AIN– pins; MDIF1 bit = "1" (Full-differential input)					
Input Voltage (Note 7)					
	MGAIN1-0 bits = "01"	-	-	0.37	Vpp
	MGAIN1-0 bits = "10"	-	-	0.066	Vpp
MIC Power Supply: MPWR pin					
Output Voltage (Note 8)		2.02	2.25	2.48	V
Load Resistance		1.0	-	-	kΩ
Load Capacitance		-	-	30	pF
ADC Analog Input Characteristics: AIN1/AIN2 pins (Single-ended inputs) → ADC → IVOL, MGAIN=+15dB, IVOL=0dB, ALC=OFF					
Resolution		-	-	16	Bits
Input Voltage (Note 9)	MGAIN=+30dB	-	0.057	-	Vpp
	MGAIN=+15dB	0.27	0.32	0.37	Vpp
	MGAIN=0dB	1.53	1.80	2.07	Vpp
S/(N+D) (–0.5dBFS) (Note 10)		67	77	-	dB
D-Range (–60dBFS, A-weighted) (Note 11)		79	87	-	dB
S/N (A-weighted) (Note 11)		79	87	-	dB
Power Supplies:					
Power Supply Current: AVDD+DVDD					
Power Up (PDN pin = "H") (Note 12)		-	6	12	mA
Power Down (PDN pin = "L") (Note 13)		-	1	20	μA

Note 7. The voltage difference between AIN+ and AIN– pins. AC coupling capacitor should be inserted in series at each input pin. Full-differential input is not available at MGAIN1-0 bits = "00". Maximum input voltage of AIN+, AIN– pins is proportional to AVDD voltage, respectively.
Vin = |(AIN+) – (AIN–)| = 0.123 x AVDD (max)@MGAIN1-0 bits = "01", 0.022 x AVDD (max)@MGAIN1-0 bits = "10".
When the signal larger than above value is input to AIN+, AIN– pin, ADC does not operate normally.

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ).

Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.107 x AVDD (typ)@MGAIN1-0 bits = "01" (+15dB), Vin = 0.6 x AVDD(typ)@MGAIN1-0 bits = "00" (0dB).

Note 10. 80dB(typ)@MGAIN=0dB, 70dB(typ)@MGAIN=+30dB

Note 11. 89dB(typ)@MGAIN=0dB, 75dB(typ)@MGAIN=+30dB

Note 12. PLL Master Mode (MCKI=12MHz), PMADC = PMVCM = PMPLL = PMMP = M/S bits = "1" and MCKO bit = "0". MPWR pin outputs 0mA. AVDD=4.5mA(typ), DVDD=1.5mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=3.8mA(typ), DVDD=1.2mA(typ).
Bypass Mode (THR bit = "1", PMADC = M/S bits = "0"), fs=8kHz: AVDD=1μA(typ), DVDD=150μA(typ).

Note 13. All digital input pins are fixed to DVDD or DVSS.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; fs=44.1kHz)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (Decimation LPF):						
Passband (Note 14)	±0.1dB	PB	0	-	17.4	kHz
	−1.0dB		-	20.0	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband (Note 14)		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	65	-	-	dB
Group Delay (Note 15)		GD	-	18	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
ADC Digital Filter (HPF): HPF1-0 bits = "00"						
Frequency Response (Note 14)	−3.0dB	FR	-	3.4	-	Hz
	−0.5dB		-	10	-	Hz
	−0.1dB		-	22	-	Hz

Note 14. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.454*fs (@−1.0dB). Each response refers to that of 1kHz.

Note 15. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data from the input register to the output register of the ADC. This time includes the group delay of the HPF.

DC CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage					
Except CSP pin; 2.2V≤ DVDD ≤3.6V	VIH	70%DVDD	-	-	V
Except CSP pin; 1.6V≤ DVDD <2.2V	VIH	80%DVDD	-	-	V
CSP pin	VIH	90%DVDD	-	-	V
Low-Level Input Voltage					
Except CSP pin; 2.2V≤ DVDD ≤3.6V	VIL	-	-	30%DVDD	V
Except CSP pin; 1.6V≤ DVDD <2.2V	VIL	-	-	20%DVDD	V
CSP pin	VIL	-	-	10%DVDD	V
High-Level Output Voltage (Iout= −200μA)	VOH	DVDD−0.2	-	-	V
Low-Level Output Voltage (Iout= 200μA)	VOL	-	-	0.2	V
Input Leakage Current (Note 16)	Iin	-	-	±10	μA

Note 16. When CSP pin is "H", CCLK pin has internal pull-down device, normally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Units
PLL Master Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.2352	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
LRCK Output Timing					
Frequency	fs	7.35	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle	Duty	-	50	-	%
BCLK Output Timing					
Period BCKO1-0 bit = "01"	tBCK	-	1/(32fs)	-	ns
Period BCKO1-0 bit = "10"	tBCK	-	1/(64fs)	-	ns
Duty Cycle	dBCK	-	50	-	%
PLL Slave Mode (PLL Reference Clock = MCKI pin)					
MCKI Input Timing					
Frequency	fCLK	11.2896	-	27	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
MCKO Output Timing					
Frequency	fMCK	0.2352	-	12.288	MHz
Duty Cycle					
Except 256fs at fs=32kHz, 29.4kHz	dMCK	40	50	60	%
256fs at fs=32kHz, 29.4kHz	dMCK	-	33	-	%
EXLRCK Input Timing					
Frequency	fs	7.35	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
EXBCLK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns
PLL Slave Mode (PLL Reference Clock = EXLRCK pin)					
EXLRCK Input Timing					
Frequency	fs	7.35	-	48	kHz
DSP Mode: Pulse Width High	tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle	Duty	45	-	55	%
EXBCLK Input Timing					
Period	tBCK	1/(64fs)	-	1/(32fs)	ns
Pulse Width Low	tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High	tBCKH	0.4 x tBCK	-	-	ns

Parameter		Symbol	min	typ	max	Units
PLL Slave Mode (PLL Reference Clock = EXBCLK pin)						
EXLRCK Input Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
EXBCLK Input Timing						
Period	PLL3-0 bits = "0010"	tBCK	-	1/(32fs)	-	ns
	PLL3-0 bits = "0011"	tBCK	-	1/(64fs)	-	ns
Pulse Width Low		tBCKL	0.4 x tBCK	-	-	ns
Pulse Width High		tBCKH	0.4 x tBCK	-	-	ns
External Slave Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
EXLRCK Input Timing						
Frequency	256fs	fs	7.35	-	48	kHz
	512fs	fs	7.35	-	26	kHz
	1024fs	fs	7.35	-	13	kHz
DSP Mode: Pulse Width High		tLRCKH	tBCK–60	-	1/fs – tBCK	ns
Except DSP Mode: Duty Cycle		Duty	45	-	55	%
EXBCLK Input Timing						
Period		tBCK	312.5	-	-	ns
Pulse Width Low		tBCKL	130	-	-	ns
Pulse Width High		tBCKH	130	-	-	ns
External Master Mode						
MCKI Input Timing						
Frequency	256fs	fCLK	1.8816	-	12.288	MHz
	512fs	fCLK	3.7632	-	13.312	MHz
	1024fs	fCLK	7.5264	-	13.312	MHz
Pulse Width Low		tCLKL	0.4/fCLK	-	-	ns
Pulse Width High		tCLKH	0.4/fCLK	-	-	ns
LRCK Output Timing						
Frequency		fs	7.35	-	48	kHz
DSP Mode: Pulse Width High		tLRCKH	-	tBCK	-	ns
Except DSP Mode: Duty Cycle		Duty	-	50	-	%
BCLK Output Timing						
Period	BCKO1-0 bit = "01"	tBCK	-	1/(32fs)	-	ns
	BCKO1-0 bit = "10"	tBCK	-	1/(64fs)	-	ns
Duty Cycle		dBCK	-	50	-	%

Parameter	Symbol	min	typ	Max	Units
Audio Interface Timing (DSP Mode)					
Master Mode					
LRCK "↑" to BCLK "↑" (Note 17)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
LRCK "↑" to BCLK "↓" (Note 18)	tDBF	0.5 x tBCK – 40	0.5 x tBCK	0.5 x tBCK + 40	ns
BCLK "↑" to SDTO (BCKP bit = "0")	tBSD	–70	-	70	ns
BCLK "↓" to SDTO (BCKP bit = "1")	tBSD	–70	-	70	ns
Slave Mode					
EXLRCK "↑" to EXBCLK "↑" (Note 17)	tLRB	0.4 x tBCK	-	-	ns
EXLRCK "↑" to EXBCLK "↓" (Note 18)	tLRB	0.4 x tBCK	-	-	ns
EXBCLK "↑" to EXLRCK "↑" (Note 17)	tBLR	0.4 x tBCK	-	-	ns
EXBCLK "↓" to EXLRCK "↑" (Note 18)	tBLR	0.4 x tBCK	-	-	ns
EXBCLK "↑" to SDTO (BCKP bit = "0")	tBSD	-	-	80	ns
EXBCLK "↓" to SDTO (BCKP bit = "1")	tBSD	-	-	80	ns
Audio Interface Timing (Left justified & I^2S)					
Master Mode					
BCLK "↓" to LRCK Edge (Note 19)	tMBLR	–40	-	40	ns
LRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	–70	-	70	ns
BCLK "↓" to SDTO	tBSD	–70	-	70	ns
Slave Mode					
EXLRCK Edge to EXBCLK "↑" (Note 19)	tLRB	50	-	-	ns
EXBCLK "↑" to EXLRCK Edge (Note 19)	tBLR	50	-	-	ns
EXLRCK Edge to SDTO (MSB) (Except I^2S mode)	tLRD	-	-	80	ns
EXBCLK "↓" to SDTO	tBSD	-	-	80	ns

Note 17. MSBS, BCKP bits = "00" or "11"
Note 18. MSBS, BCKP bits = "01" or "10"
Note 19. EXBCLK rising edge must not occur at the same time as EXLRCK edge.

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (CSP pin = "L")					
CCLK Period	tCCK	142	-	-	ns
CCLK Pulse Width Low	tCCKL	56	-	-	ns
Pulse Width High	tCCKH	56	-	-	ns
CDTI Setup Time	tCDS	28	-	-	ns
CDTI Hold Time	tCDH	28	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Control Interface Timing (CSP pin = "H")					
CCLK Period	tCCK	142	-	-	ns
CCLK Pulse Width Low	tCCKL	56	-	-	ns
Pulse Width High	tCCKH	56	-	-	ns
CDTI Setup Time	tCDS	28	-	-	ns
CDTI Hold Time	tCDH	28	-	-	ns
CSN "L" Time	tCSW	150	-	-	ns
CSN "↑" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↓"	tCSH	50	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 20)	tPD	150	-	-	ns
PMADC "↑" to SDTO valid (Note 21)					
HPF1-0 bits = "00"	tPDV	-	3088	-	1/fs
HPF1-0 bits = "01"	tPDV	-	1552	-	1/fs
HPF1-0 bits = "10"	tPDV	-	784	-	1/fs

Note 20. The AK5700 can be reset by the PDN pin = "L".
Note 21. This is the count of LRCK "↑" from the PMADC bit = "1".

■ Timing Diagram

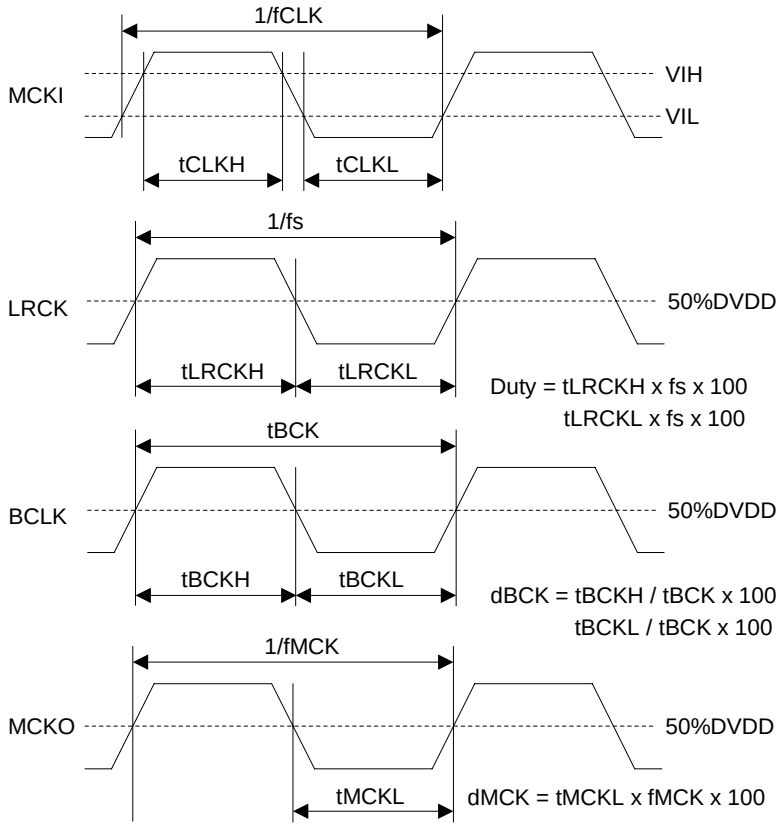


Figure 2. Clock Timing (PLL/EXT Master mode)

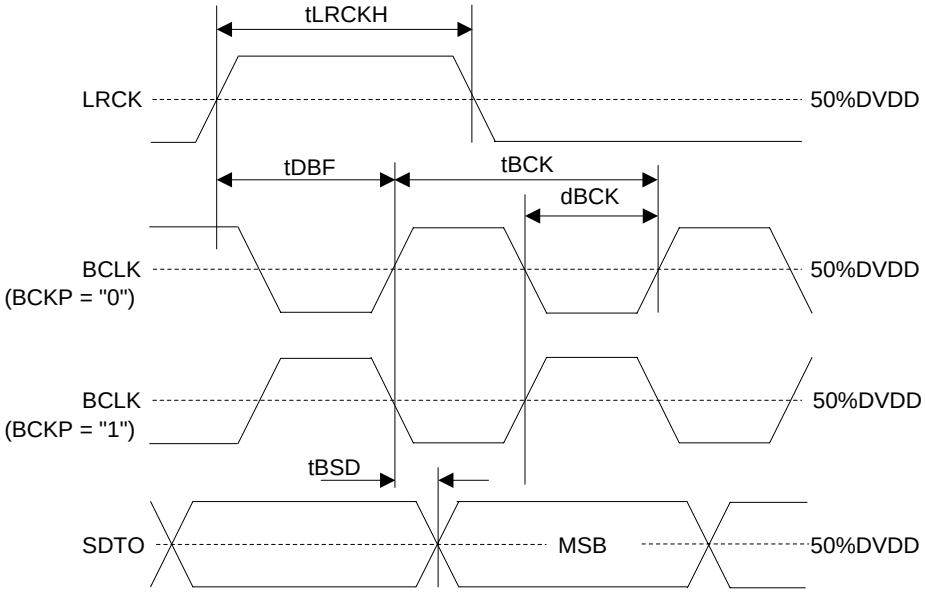


Figure 3. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = “0”)

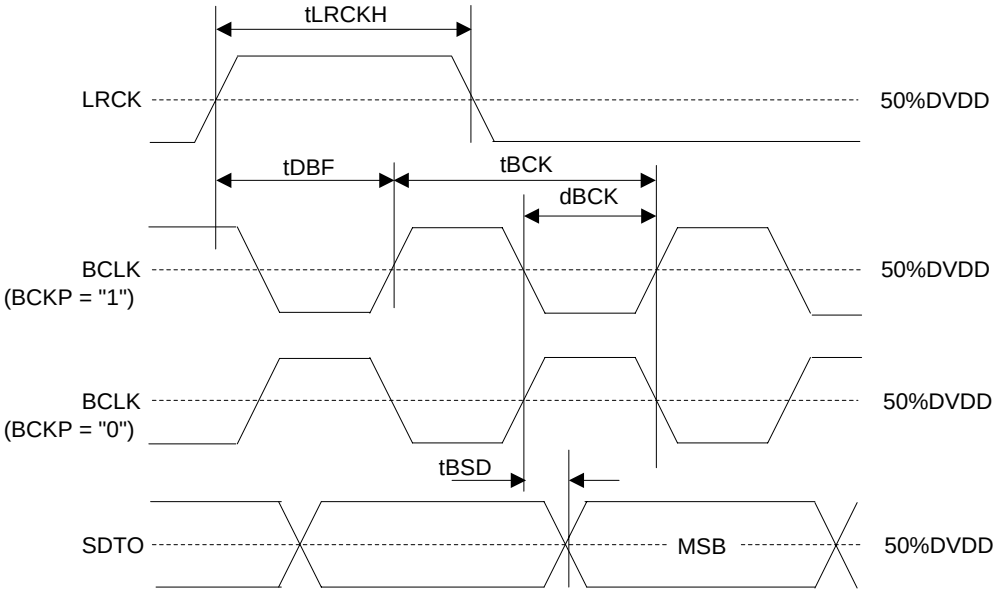


Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = "1")

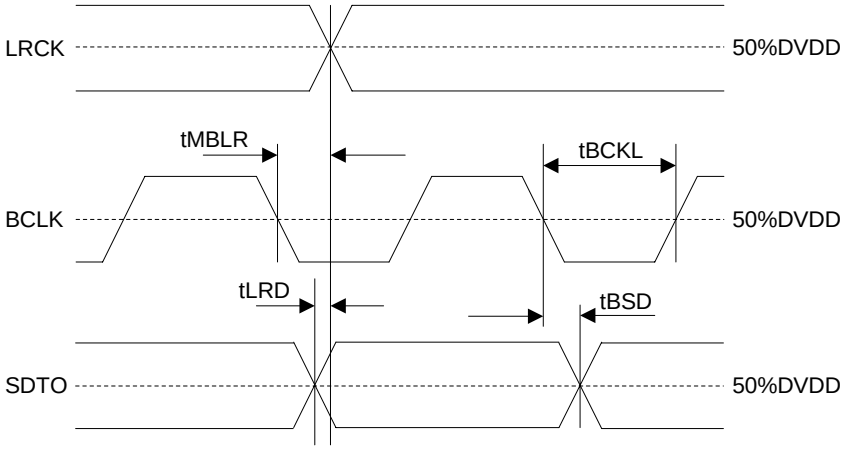


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Except DSP mode)

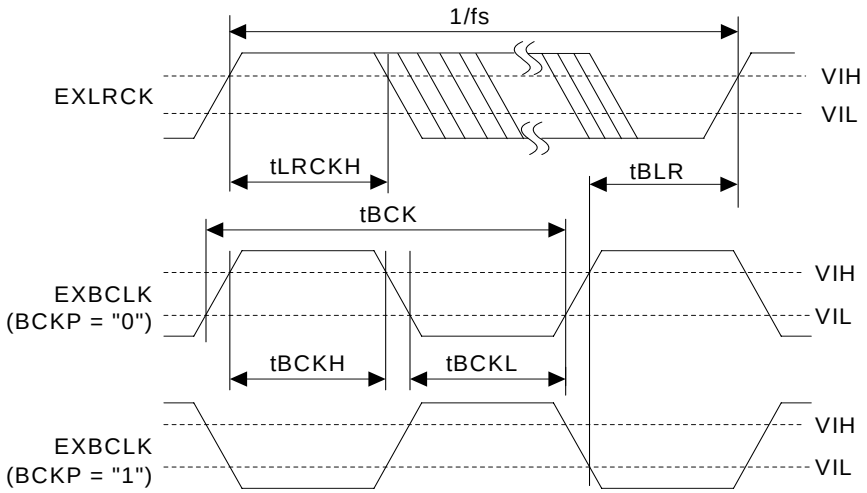


Figure 6. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 0)

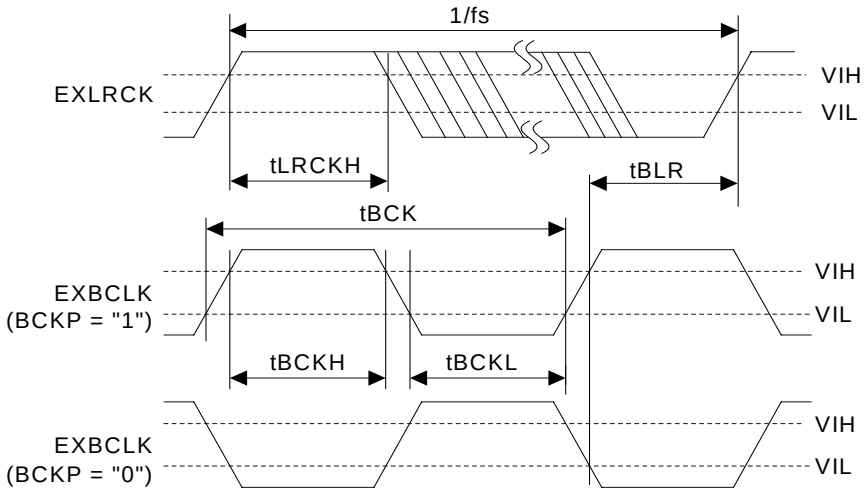


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 1)

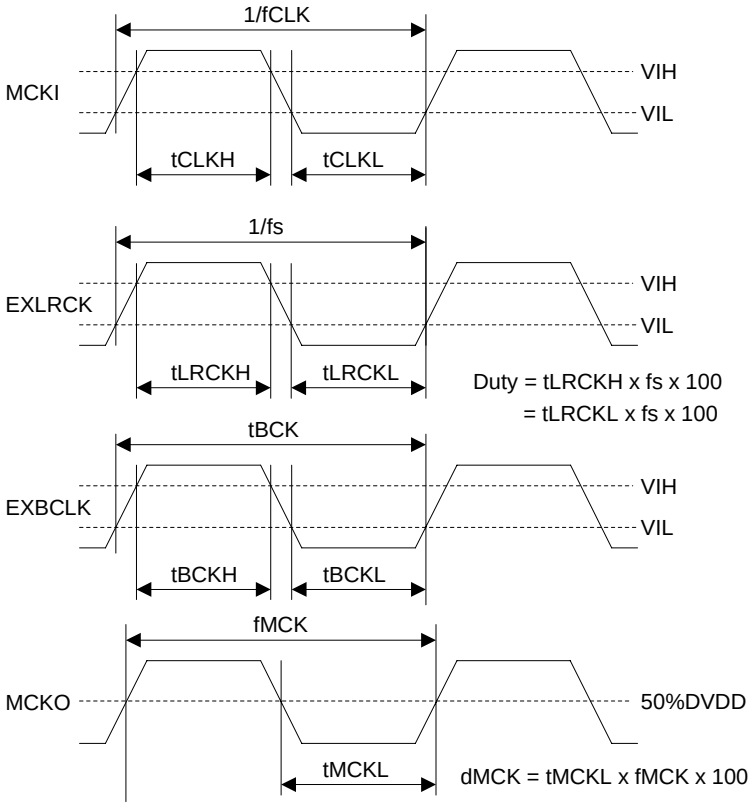


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

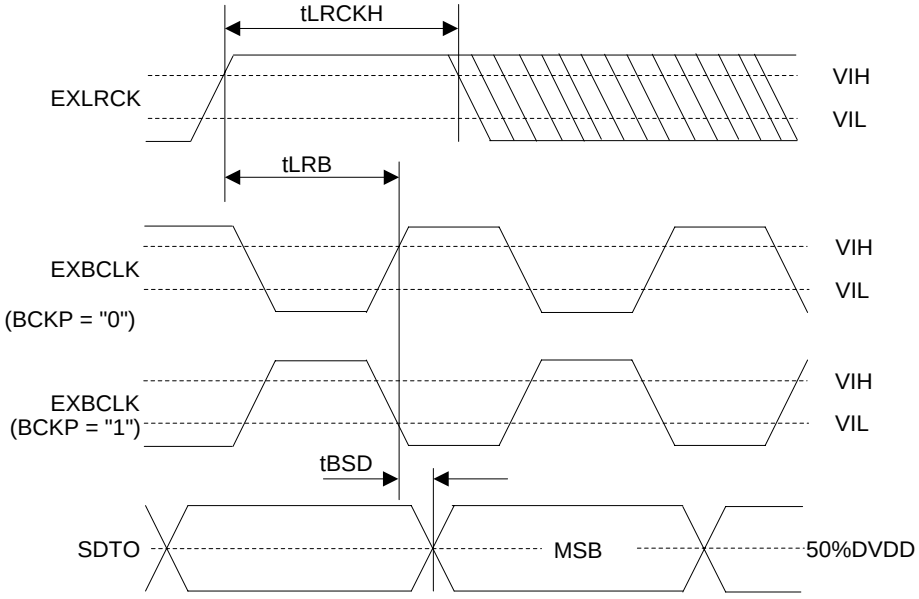


Figure 9. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)

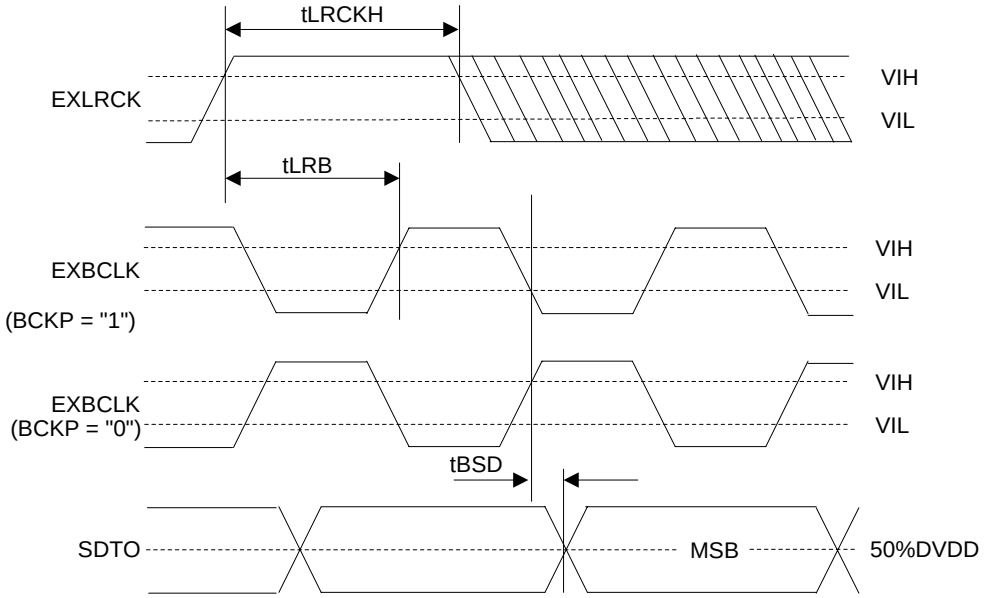


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = 1)

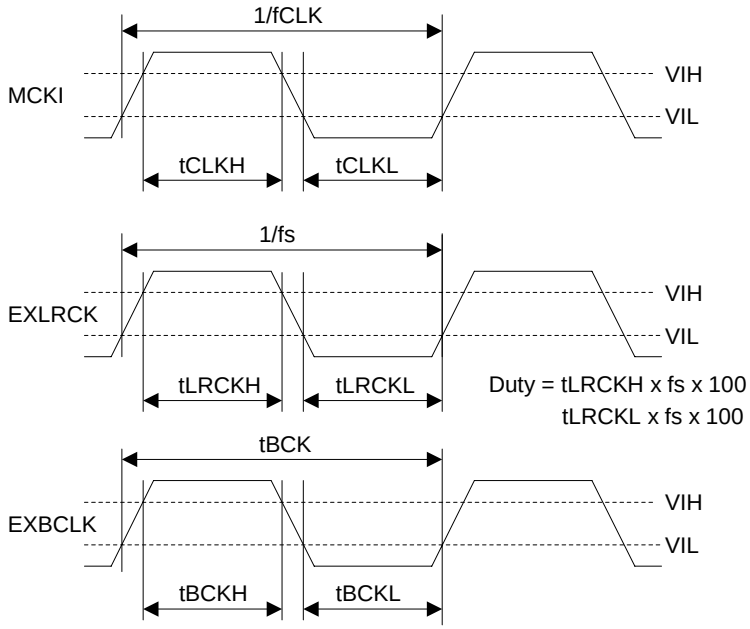


Figure 11. Clock Timing (EXT Slave mode)

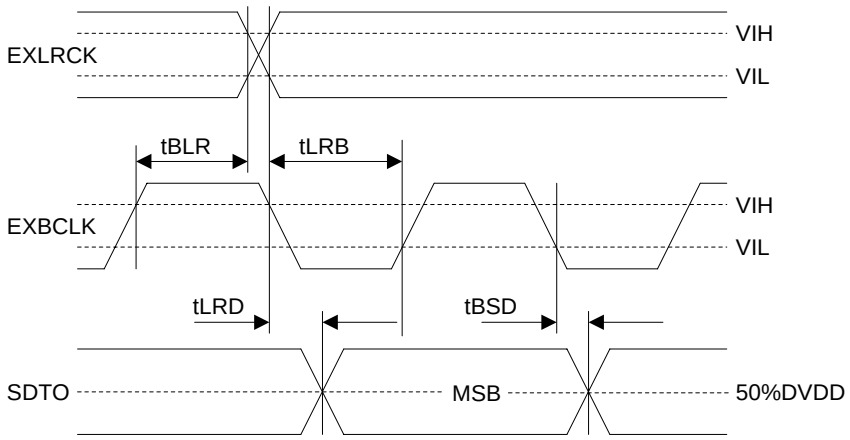


Figure 12. Audio Interface Timing (PLL/EXT Slave mode)

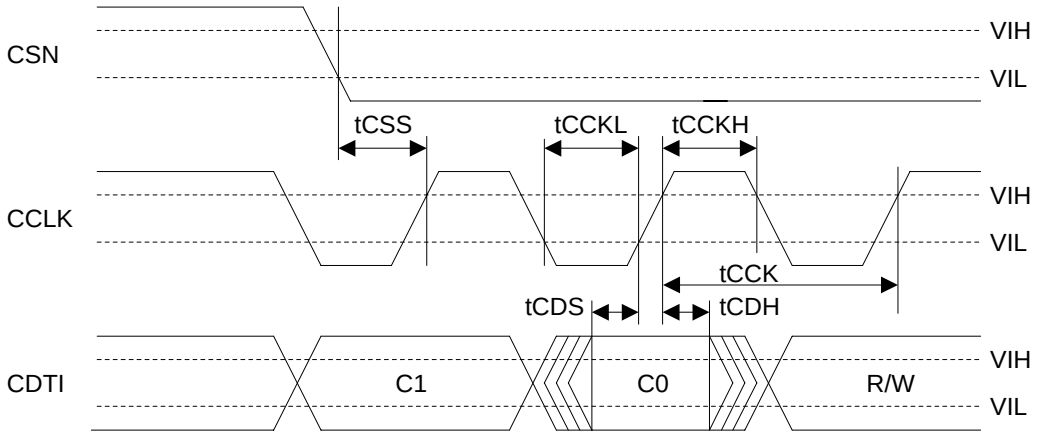


Figure 13. WRITE Command Input Timing (CSP pin = "L")

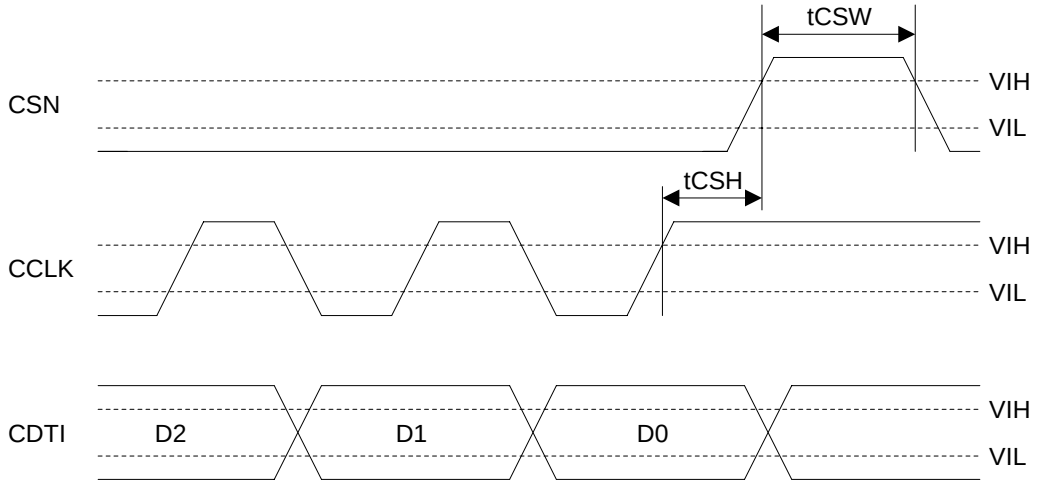


Figure 14. WRITE Data Input Timing (CSP pin = "L")

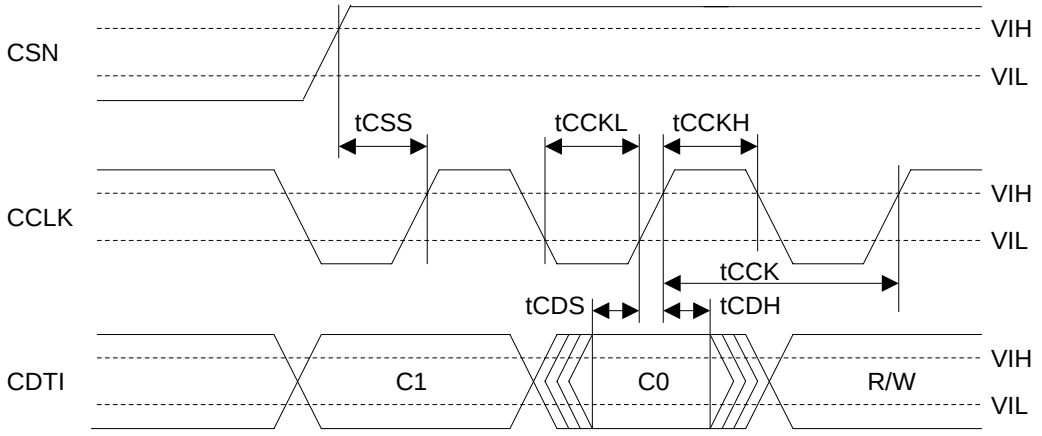


Figure 15. WRITE Command Input Timing (CSP pin = "H")

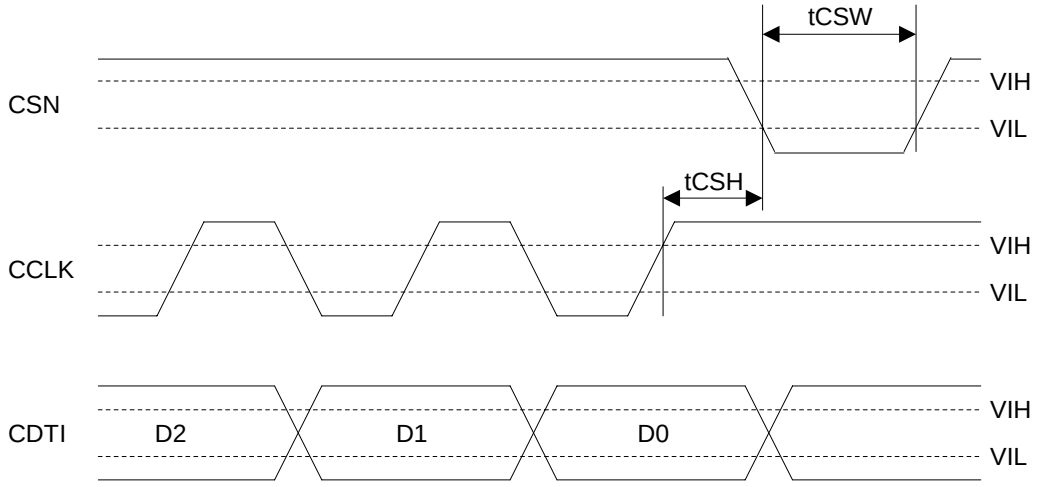


Figure 16. WRITE Data Input Timing (CSP pin = "H")

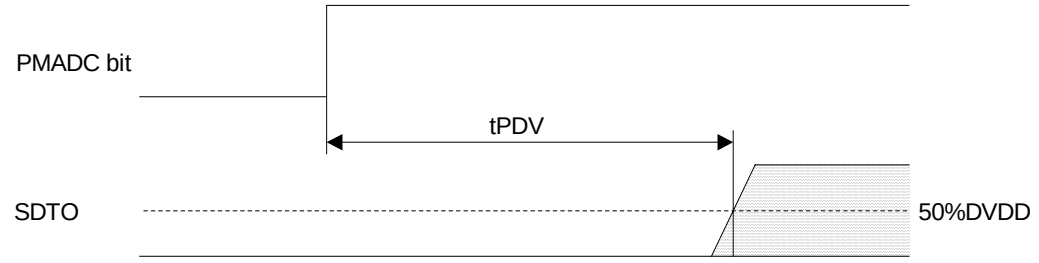


Figure 17. Power Down & Reset Timing 1

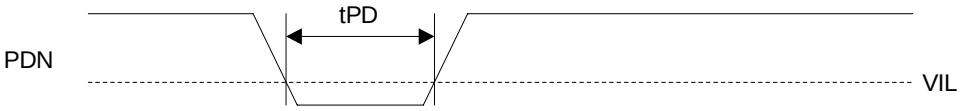


Figure 18. Power Down & Reset Timing 2

OPERATION OVERVIEW

■ System Clock

There are the following five clock modes to interface with external devices (see Table 1 and Table 2.)

Mode	PMPLL bit	M/S bit	PLL3-0 bits	Figure
PLL Master Mode (Note 22)	1	1	See Table 4	Figure 19
PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)	1	0	See Table 4	Figure 20
PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin)	1	0	See Table 4	Figure 21
EXT Slave Mode	0	0	x	Figure 22
EXT Master Mode (Note 23)	0	0	x	Figure 23

Note 22. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is "1".

Note 23. In case of EXT Master Mode, the register should be set as Figure 45.

Table 1. Clock Mode Setting (x: Don't care)

Mode	MCKO bit	MCKO pin	MCKI pin	BCLK pin, EXBCLK pin	LRCK pin, EXLRCK pin
PLL Master Mode	0	"L"	Selected by PLL3-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: MCKI pin)	0	"L"	Selected by PLL3-0 bits	EXBCLK pin (≥ 32fs)	EXLRCK pin (1fs)
	1	Selected by PS1-0 bits			
PLL Slave Mode (PLL Reference Clock: EXLRCK or EXBCLK pin)	0	"L"	GND	EXBCLK pin (Selected by PLL3-0 bits)	EXLRCK pin (1fs)
EXT Slave Mode	0	"L"	Selected by FS1-0 bits	EXBCLK pin (≥ 32fs)	EXLRCK pin (1fs)
EXT Master Mode	0	"L"	Selected by FS1-0 bits	BCLK pin (Selected by BCKO1-0 bits)	LRCK pin (1fs)

Table 2. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5700 is power-down mode (PDN pin = "L") and exits reset state, the AK5700 is slave mode. After exiting reset state, the AK5700 goes to master mode by changing M/S bit = "1".

M/S bit	Mode	Used pins	
0	Slave Mode	EXBCLK, EXLRCK	Default
1	Master Mode	BCLK, LRCK	

Table 3. Select Master/Salve Mode

■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK5700 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

Mode	PLL3 bit	PLL2 Bit	PLL1 bit	PLL0 bit	PLL Reference Clock Input Pin	Input Frequency	R and C of VCOC pin		PLL Lock Time (max)	
							R[Ω]	C[F]		
0	0	0	0	0	EXLRCK pin	1fs	6.8k	220n	80ms	
2	0	0	1	0	EXBCLK pin	32fs	10k	4.7n	2ms	
							10k	10n	4ms	
3	0	0	1	1	EXBCLK pin	64fs	10k	4.7n	2ms	
							10k	10n	4ms	
4	0	1	0	0	MCKI pin	11.2896MHz	10k	4.7n	40ms	
5	0	1	0	1	MCKI pin	12.288MHz	10k	4.7n	40ms	
6	0	1	1	0	MCKI pin	12MHz	10k	4.7n	40ms	
7	0	1	1	1	MCKI pin	24MHz	10k	4.7n	40ms	
8	1	0	0	0	MCKI pin	19.2MHz	10k	4.7n	40ms	
9	1	0	0	1	MCKI pin	12MHz (Note24)	10k	4.7n	40ms	Default
12	1	1	0	0	MCKI pin	13.5MHz	10k	10n	40ms	
13	1	1	0	1	MCKI pin	27MHz	10k	10n	40ms	
14	1	1	1	0	MCKI pin	13MHz	10k	220n	60ms	
15	1	1	1	1	MCKI pin	26MHz	10k	220n	60ms	
Others	Others				N/A					

Note 24. See Table 5 regarding the difference between PLL3-0 bits = "0110"(Mode 6) and "1001"(Mode 9). Clock jitter is lower in Mode9 than Mode6 respectively.

Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	0	8kHz	
1	0	0	0	1	12kHz	
2	0	0	1	0	16kHz	
3	0	0	1	1	24kHz	
4	0	1	0	0	7.35kHz 7.349918kHz (Note25)	
5	0	1	0	1	11.025kHz 11.024877kHz (Note25)	
6	0	1	1	0	14.7kHz 14.69984kHz (Note25)	
7	0	1	1	1	22.05kHz 22.04975kHz (Note25)	
10	1	0	1	0	32kHz	
11	1	0	1	1	48kHz	
14	1	1	1	0	29.4kHz 29.39967kHz (Note25)	
15	1	1	1	1	44.1kHz 44.0995kHz (Note25)	Default
Others	Others				N/A	

Note 25. In case of PLL3-0 bits = "1001"

Table 5. Setting of Sampling Frequency at PMPLL bit = "1" and Reference Clock=MCKI pin

When PLL reference clock input is EXLRCK or EXBCLK pin, the sampling frequency is selected by FS3 and FS2 bits (See Table 6).

Mode	FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency Range	
0	0	0	Don't care	Don't care	7.35kHz ≤ fs ≤ 12kHz	
1	0	1	Don't care	Don't care	12kHz < fs ≤ 24kHz	
2	1	Don't care	Don't care	Don't care	24kHz < fs ≤ 48kHz	Default
Others	Others				N/A	

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" and Reference=EXLRCK/EXBCLK

■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BCLK pins go to "L" and irregular frequency clock is output from MCKO pins at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", MCKO pin goes to "L" (see Table 7).

In DSP Mode 0, BCLK and LRCK start to output corresponding to Ach data after PLL goes to lock state by setting PMPLL bit = "0" → "1". When MSBS and BCKP bits are "01" or "10" in DSP Mode 0, BCLK "H" time of the first pulse becomes shorter by 1/(256fs) than "H" time except for the first pulse.

When sampling frequency is changed, BCLK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

PLL State	MCKO pin		BCLK pin	LRCK pin
	MCKO bit = "0"	MCKO bit = "1"		
After that PMPLL bit "0" → "1"	"L" Output	Invalid	"L" Output	"L" Output
PLL Unlock (except above case)	"L" Output	Invalid	Invalid	Invalid
PLL Lock	"L" Output	See Table 9	See Table 10	1fs Output

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from MCKO pin when PLL is locked. ADC outputs invalid data when the PLL is unlocked.

PLL State	MCKO pin	
	MCKO bit = "0"	MCKO bit = "1"
After that PMPLL bit "0" → "1"	"L" Output	Invalid
PLL Unlock (except above case)	"L" Output	Invalid
PLL Lock	"L" Output	See Table 9

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BCLK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (see Table 9) and the output is enabled by MCKO bit. The BCLK output frequency is selected among 32fs or 64fs, by BCKO1-0 bits (see Table 10).

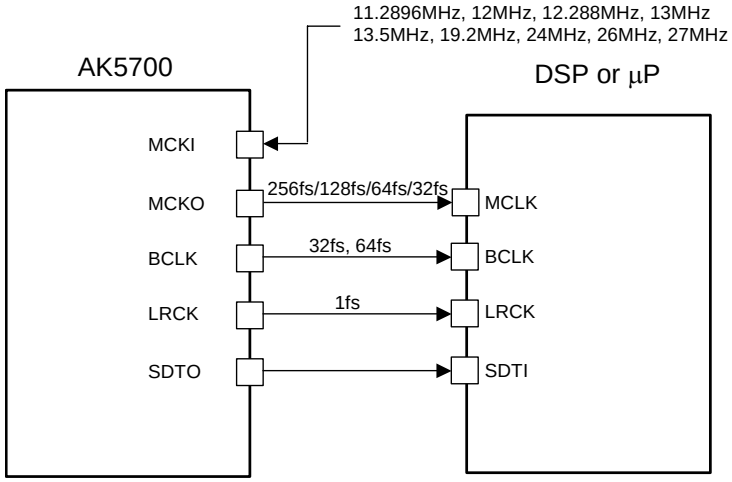


Figure 19. PLL Master Mode

Mode	PS1 bit	PS0 bit	MCKO pin	
0	0	0	256fs	Default
1	0	1	128fs	
2	1	0	64fs	
3	1	1	32fs	

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

BCKO1 bit	BCKO0 bit	BCLK Output Frequency	
0	0	N/A	
0	1	32fs	Default
1	0	64fs	
1	1	N/A	

Table 10. BCLK Output Frequency at Master Mode

■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to MCKI, EXBCLK or EXLRCK pin. The required clock to the AK5700 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (see Table 4).

a) PLL reference clock: MCKI pin

EXBCLK and EXLRCK inputs should be synchronized with MCKO output. The phase between MCKO and EXLRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits (see Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (see Table 5).

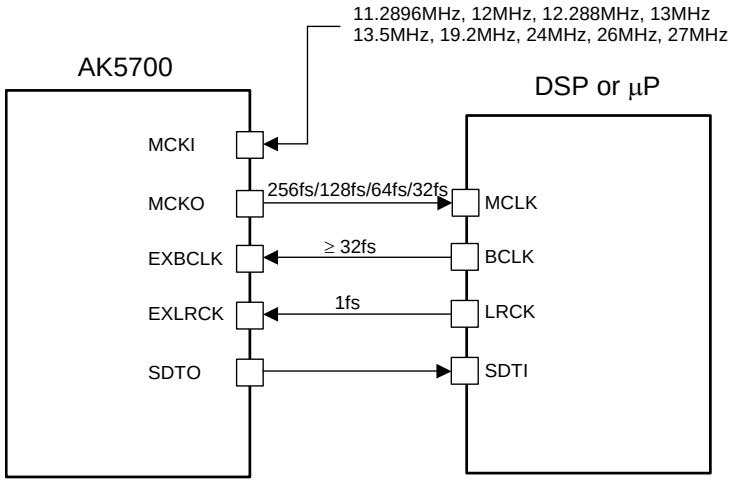


Figure 20. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

The external clocks (MCKI, EXBCLK and EXLRCK) should always be present whenever the ADC is in operation (PMADC bit = "1"). If these clocks are not provided, the AK5700 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADC bit = "0").

b) PLL reference clock: EXBCLK or EXLRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (see Table 6).

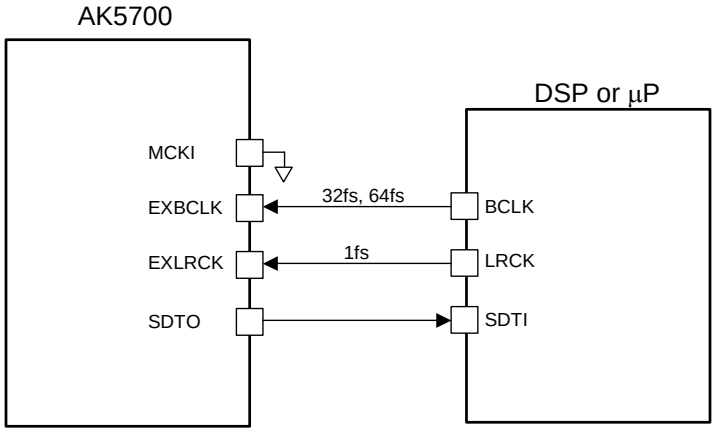


Figure 21. PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin)

■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK5700 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), EXLRCK (fs) and EXBCLK (≥32fs). The master clock (MCKI) should be synchronized with EXLRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (see Table 11).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ~ 48kHz	
1	Don't care	0	1	1024fs	7.35kHz ~ 13kHz	
2	Don't care	1	0	512fs	7.35kHz ~ 26kHz	
3	Don't care	1	1	256fs	7.35kHz ~ 48kHz	Default

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

The external clocks (MCKI, EXBCLK and EXLRCK) should always be present whenever the ADC is in operation (PMADC bit = "1"). If these clocks are not provided, the AK5700 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADC bit = "0").

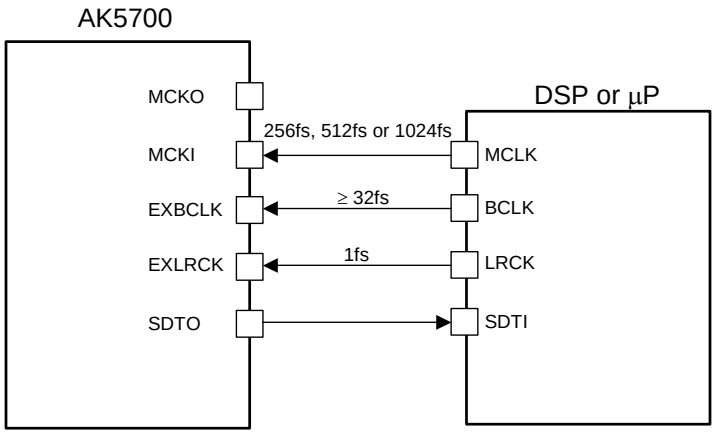


Figure 22. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1", TE3-0 bits = "0101", TMASTER bit = "1")

The AK5700 becomes EXT Master Mode by setting as Figure 45. Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (see Table 12).

Mode	FS3-2 bits	FS1 bit	FS0 bit	MCKI Input Frequency	Sampling Frequency Range	
0	Don't care	0	0	256fs	7.35kHz ~ 48kHz	
1	Don't care	0	1	1024fs	7.35kHz ~ 13kHz	
2	Don't care	1	0	512fs	7.35kHz ~ 26kHz	
3	Don't care	1	1	256fs	7.35kHz ~ 48kHz	Default

Table 12. MCKI Frequency at EXT Master Mode

MCKI should always be present whenever the ADC is in operation (PMADC bit = "1"). If MCKI is not provided, the AK5700 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC should be in the power-down mode (PMADC bits = "0").

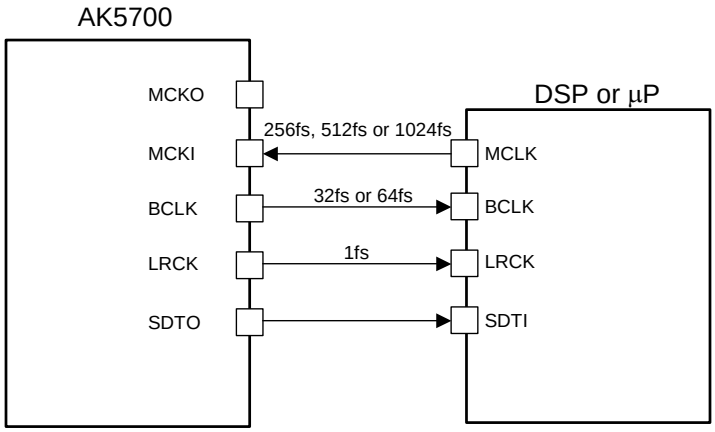


Figure 23. EXT Master Mode

BCKO1 bit	BCKO0 bit	BCLK Output Frequency	
0	0	N/A	
0	1	32fs	Default
1	0	64fs	
1	1	N/A	

Table 13. BCLK Output Frequency at Master Mode

■ Bypass Mode

When THR bit = "1", M/S bit = "0" and PMADC bit = "0" input clocks and data of EXLRCK, EXBCLK and EXSDTI pins are bypassed to LRCK, BCLK and SDTO pins, respectively.

When THR bit = "1", M/S bit = "0" and PMADC bit = "1" input clocks of EXLRCK and EXBCLK pins are bypassed to LRCK and BCLK pins, and ADC data is output from SDTO pin.

THR bit	M/S bit	PMADC bit	BCLK/LRCK	SDTO	Mode	Figure	
0	0	0	"L"	"L"	Power down		Default
		1	"L"	ADC data	Slave mode		
	1	0	Output	"L"	Power down		
		1	Output	ADC data	Master mode		
1	0	0	EXBCLK/EXLRCK	EXSDTI	Bypass mode	Figure 24	
		1	EXBCLK/EXLRCK	ADC data	Slave & Bypass	Figure 25	
	1	0	N/A	N/A	N/A		
		1	Output	ADC data	Master mode		

Table 14. Bypass Mode Select

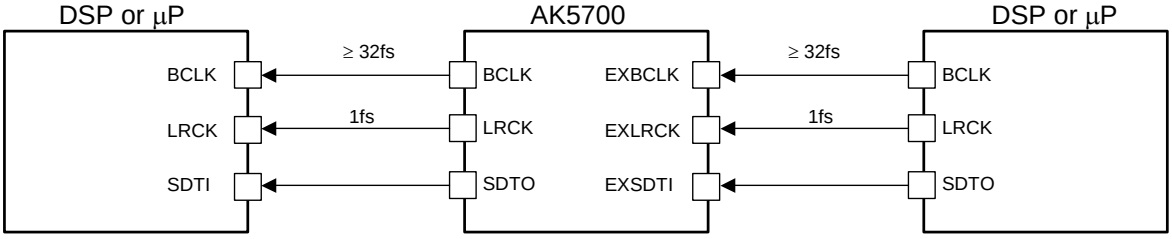


Figure 24. Bypass Mode

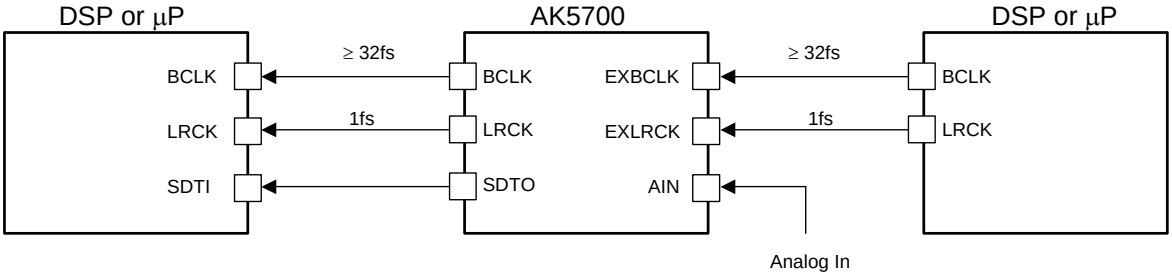


Figure 25. Slave & Bypass Mode

■ Audio Interface Format

Fore types of data format are available and are selected by setting the DIF1-0 bits (see Table 15). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes. LRCK, BCLK and SDTO pins are used in master mode. EXLRCK, EXBCLK and SDTO pins are used in slave mode. In modes 2 and 3, the SDTO is clocked out on the falling edge ("↓") of BCLK/EXBCLK. SDTO pin outputs same data two times in one period of EXLRCK/LRCK.

Mode	DIF1 bit	DIF0 bit	SDTO	BCLK, EXBCLK	Figure	
0	0	0	DSP Mode 0	32fs	See Table 16	
1	0	1	Reserved	-	-	
2	1	0	MSB justified	≥ 32fs	Figure 30	
3	1	1	I^2S compatible	≥ 32fs	Figure 31	Default

Table 15. Audio Interface Format

In Mode 0 (DSP mode 0), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is "0", SDTO data is output by rising edge ("↑") of BCLK/EXBCLK.
When BCKP bit is "1", SDTO data is output by falling edge ("↓") of BCLK/EXBCLK.

MSB data position of SDTO can be shifted by MSBS bit. The shifted period is a half of BCLK/EXBCLK.

DIF1	DIF0	MSBS	BCKP	Audio Interface Format
0	0	0	0	MSB of SDTO is output by the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 26).
		0	1	MSB of SDTO is output by the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 27).
		1	0	MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 28).
		1	1	MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 29).

Table 16. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "–1" at 16bit data is converted to "–1" at 8-bit data. And when the DAC playbacks this 8-bit data, "–1" at 8-bit data will be converted to "–256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.

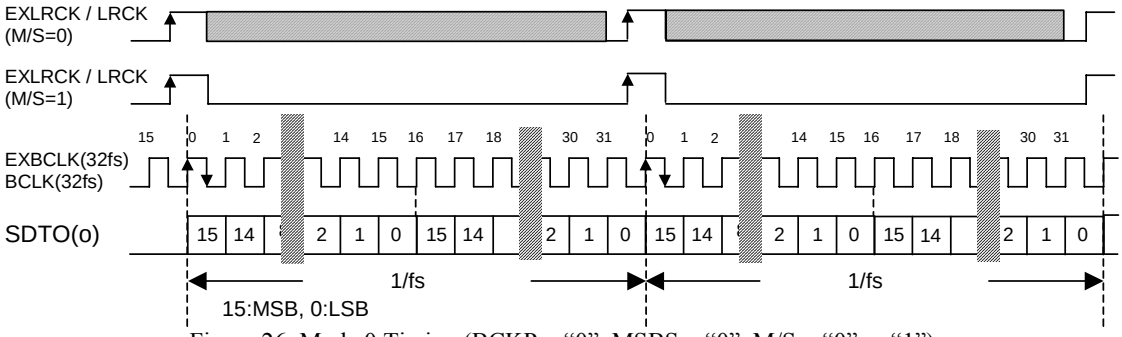


Figure 26. Mode 0 Timing (BCKP = "0", MSBS = "0", M/S = "0" or "1")

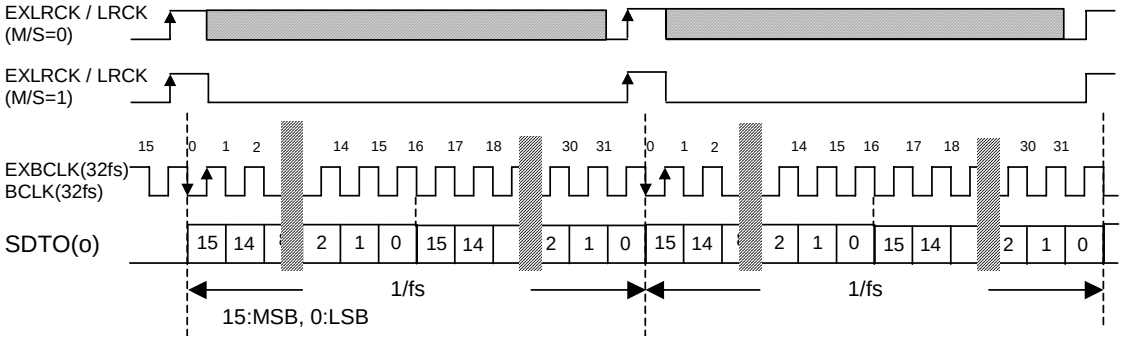


Figure 27. Mode 0 Timing (BCKP = "1", MSBS = "0", M/S = "0" or "1")

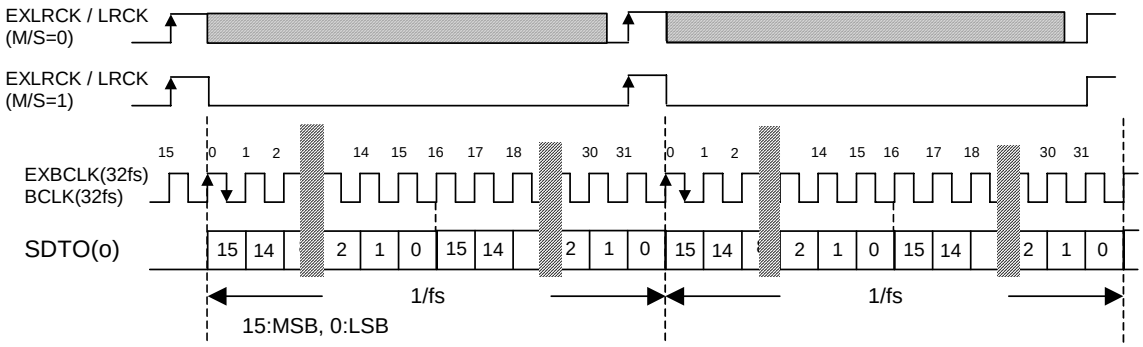


Figure 28. Mode 0 Timing (BCKP = "0", MSBS = "1", M/S = "0" or "1")

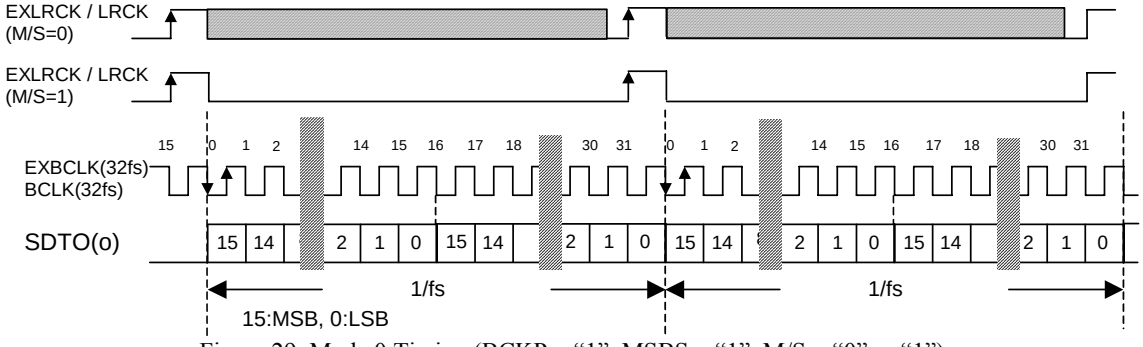


Figure 29. Mode 0 Timing (BCKP = "1", MSBS = "1", M/S = "0" or "1")

Note : The data from 0 to 15 bits is the same as from 16 to 31 bits at the Figure 26, Figure 27, Figure 28, Figure 29

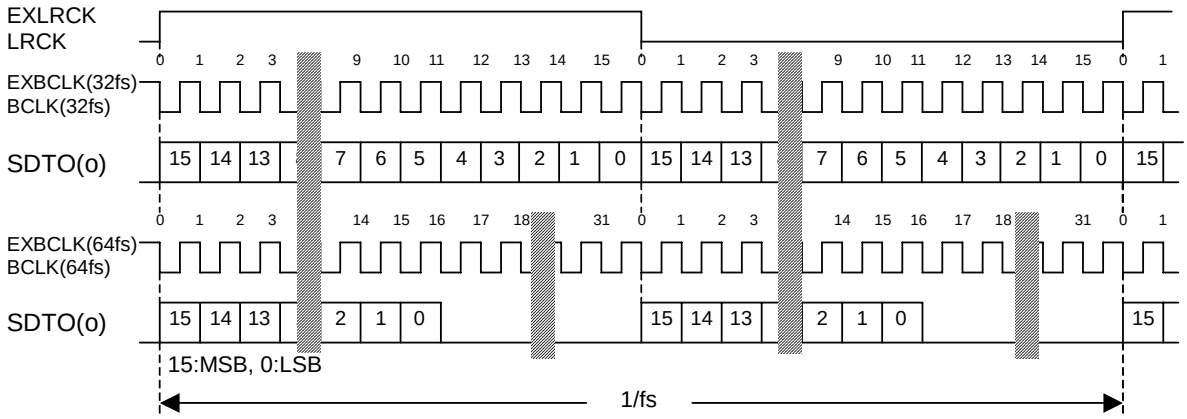


Figure 30. Mode 2 Timing (MSB justified, M/S = "0" or "1")

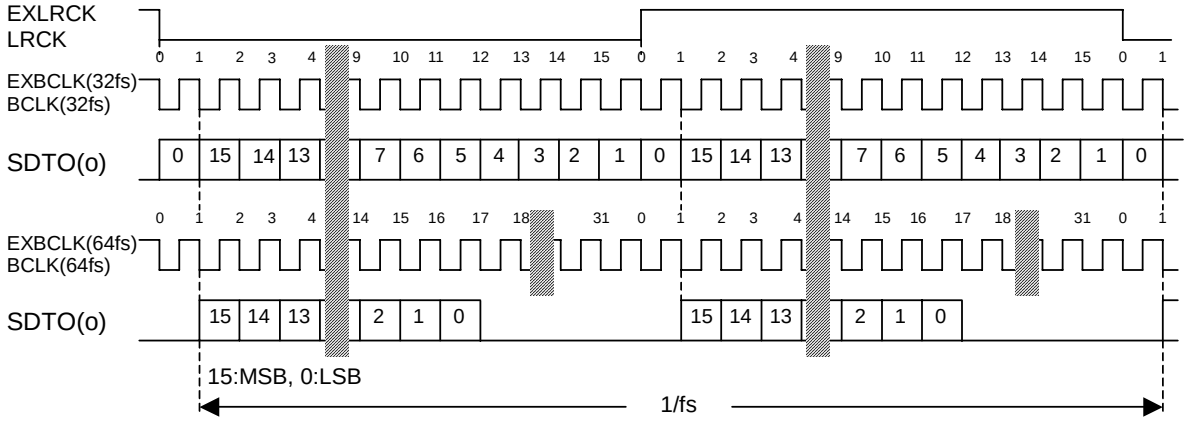


Figure 31. Mode 3 Timing (I^2S, M/S = "0" or "1")

Note : The data from 0 to 15 bits is the same as when LRCK is "H" or "L" at the Figure 30, Figure 31

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is selected by HPF1-0 bits (see Table 17) and scales with sampling rate (fs). The default value is 3.4Hz (@fs=44.1kHz).

HPF1 bit	HPF0 bit	fc			
		fs=44.1kHz	fs=22.05kHz	fs=11.025kHz	
0	0	3.4Hz	1.7Hz	0.85Hz	Default
0	1	6.8Hz	3.4Hz	1.7Hz	
1	0	13.6Hz	6.8Hz	3.4Hz	
1	1	N/A	N/A	N/A	

Table 17. Digital HPF Cut-off Frequency

■ MIC/LINE Input Selector

The AK5700 has input selector. When MDIF1 bit is "0", AIN bit selects AIN1or AIN2. When MDIF1 bit is "1", AIN1pin become AIN+ pin . In this case, full-differential input is available (Figure 33). When full-differential input is used, the signal should not be input to the pins marked by "X" in Table 19.

MDIF1 bit	AIN bit	Ach	
0	0	AIN1	Default
		AIN1	
	1	AIN2	
		AIN2	
	0	AIN1	
	1	N/A	
1	x	N/A	
		AIN+/–	
	x	AIN+/–	

Table 18. MIC/Line In Path Select

Register	Pin		
MDIF1 bit	AIN1 AIN1+	AIN2	AIN1–
0	O	O	-
1	O	X	O

Table 19. Handling of MIC/Line Input Pins ("-": N/A; "X": Signal should not be input.)

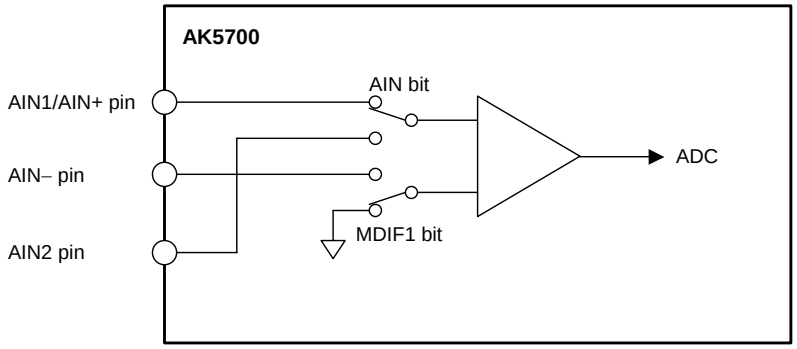


Figure 32. Mic/Line Input Selector

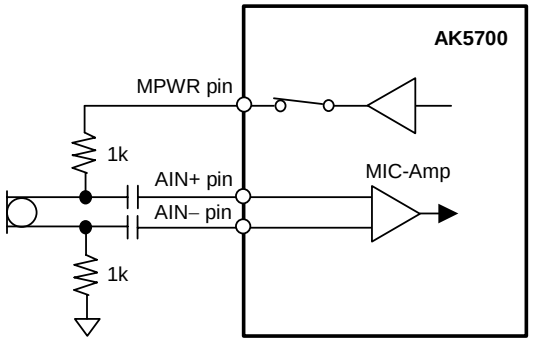


Figure 33. Connection Example for Full-differential Mic Input (MDIF1bit = "1")

■ MIC Gain Amplifier

The AK5700 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN1-0 bits (see Table 20). The typical input impedance is 60kΩ(typ)@MGAIN1-0 bits = "00" or 30kΩ(typ)@MGAIN1-0 bits = "01" or "10".

MGAIN1 bit	MGAIN0 bit	Input Gain	
0	0	0dB	
0	1	+15dB	Default
1	0	+30dB	
1	1	N/A	

Table 20. Mic Input Gain

■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 1.0kΩ. In case of using two sets of mono mic, the load resistance is minimum 2.0kΩ for each channel. No capacitor must not be connected directly to MPWR pin (see Figure 34).

PMMP bit	MPWR pin	
0	Hi-Z	Default
1	Output	

Table 21. MIC Power

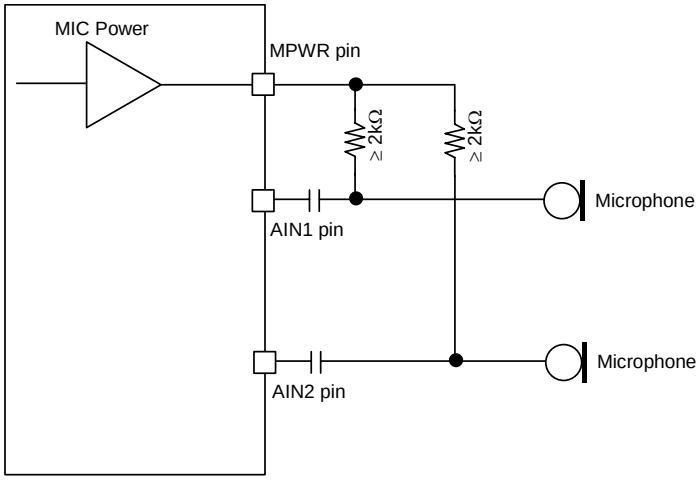


Figure 34. MIC Block Circuit

■ ALC Operation

The ALC (Automatic Level Control) is done by ALC block when ALC bit is "1".

1. ALC Limiter Operation

During the ALC limiter operation, when the output exceeds the ALC limiter detection level (Table 22), the IVL value is attenuated automatically by the amount defined by the ALC limiter ATT step (Table 23).

When ZELMN bit = "0" (zero cross detection is enabled), the IVL value is changed by ALC limiter operation at the individual zero crossing point of zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 24).

When ZELMN bit = "1" (zero cross detection is disabled), IVL value is immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless as the setting of LMAT1-0 bits.

The attenuation operation is done continuously until the input signal level becomes ALC limiter detection level (Table 22) or less. After completing the attenuation operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

LMTH1	LMTH0	ALC Limier Detection Level	ALC Recovery Waiting Counter Reset Level	
0	0	ALC Output ≥ –2.5dBFS	–2.5dBFS > ALC Output ≥ –4.1dBFS	Default
0	1	ALC Output ≥ –4.1dBFS	–4.1dBFS > ALC Output ≥ –6.0dBFS	
1	0	ALC Output ≥ –6.0dBFS	–6.0dBFS > ALC Output ≥ –8.5dBFS	
1	1	ALC Output ≥ –8.5dBFS	–8.5dBFS > ALC Output ≥ –12dBFS	

Table 22. ALC Limiter Detection Level / Recovery Counter Reset Level

ZELMN	LMAT1	LMAT0	ALC Limiter ATT Step		
0	0	0	1 step	0.375dB	Default
	0	1	2 step	0.750dB	
	1	0	4 step	1.500dB	
	1	1	8 step	3.000dB	
1	x	x	1step	0.375dB	

Table 23. ALC Limiter ATT Step

ZTM1	ZTM0		Zero Crossing Timeout Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 24. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM1-0 bits (Table 25) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 22) during the wait time, the ALC recovery operation is done. The IVL value is automatically incremented by RGAIN1-0 bits (Table 26) up to the set reference level (Table 27) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 24). The ALC recovery operation is done at a period set by WTM1-0 bits. If ZTM1-0 is longer than WTM1-0 and no zero crossing occurs, the ALC recovery operation is done at a period set by ZTM1-0 bits.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to "01", IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0), the IVOL values are not increased.

When
"ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
"ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation.

WTM1	WTM0		ALC Recovery Operation Waiting Period			
			8kHz	16kHz	44.1kHz	
0	0	128/fs	16ms	8ms	2.9ms	Default
0	1	256/fs	32ms	16ms	5.8ms	
1	0	512/fs	64ms	32ms	11.6ms	
1	1	1024/fs	128ms	64ms	23.2ms	

Table 25. ALC Recovery Operation Waiting Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.375dB	Default
0	1	2 step	0.750dB	
1	0	3 step	1.125dB	
1	1	4 step	1.500dB	

Table 26. ALC Recovery GAIN Step

REF7-0	GAIN(dB)	Step	
F1H	+36.0	0.375dB	Default
F0H	+35.625		
EFH	+35.25		
:	:		
E2H	+30.375		
E1H	+30.0		
E0H	+29.625		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54.0		
00H	MUTE		

Table 27. Reference Level at ALC Recovery operation

3. Example of ALC Operation

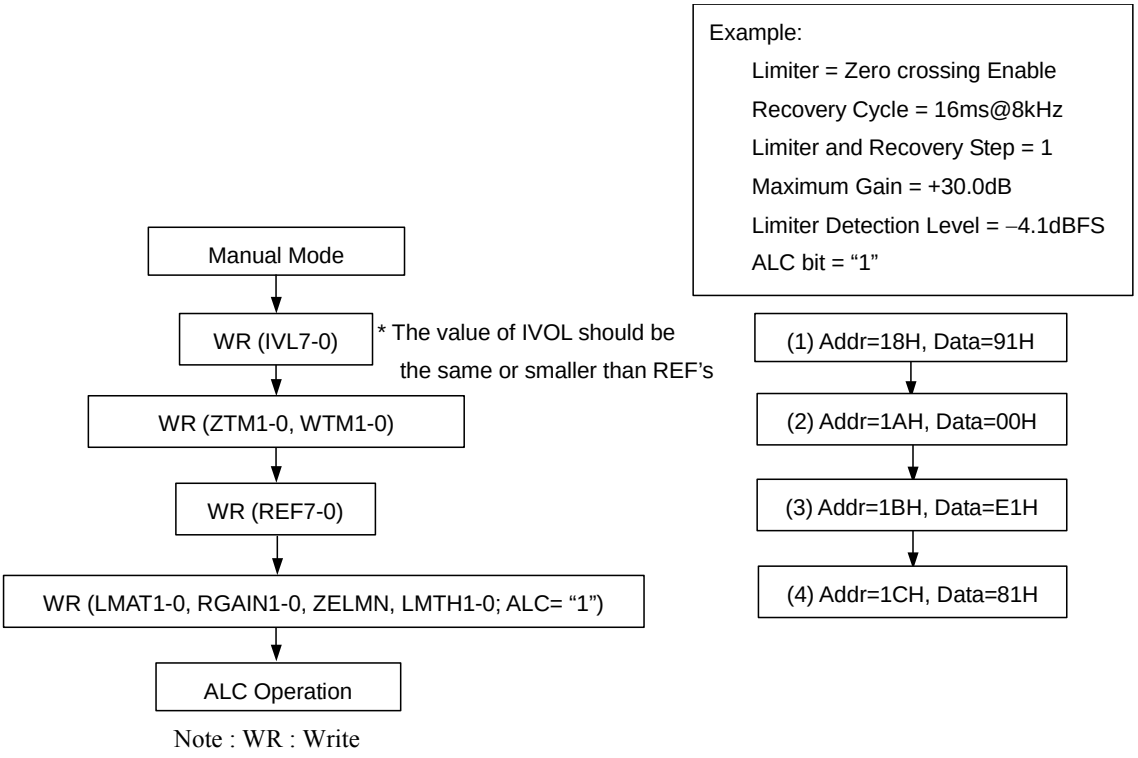
Table 28 shows the examples of the ALC setting for mic recording.

Register Name	Comment	fs=8kHz		fs=44.1kHz	
		Data	Operation	Data	Operation
LMTH	Limiter detection Level	01	–4.1dBFS	01	–4.1dBFS
ZELMN	Limiter zero crossing detection	0	Enable	0	Enable
ZTM1-0	Zero crossing timeout period	00	16ms	10	11.6ms
WTM1-0	Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits	00	16ms	10	11.6ms
REF7-0	Maximum gain at recovery operation	E1H	+30dB	E1H	+30dB
IVL7-0	Gain of IVOL	91H	0dB	91H	0dB
LMAT1-0	Limiter ATT step	00	1 step	00	1 step
RGAIN1-0	Recovery GAIN step	00	1 step	00	1 step
ALC	ALC enable	1	Enable	1	Enable

Table 28. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMADC bit = "0".

- **LMTH, LMAT1-0, WTM1-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN**



Note : WR : Write

Figure 35. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed. For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 bits set the gain of the volume control (Table 29). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits.

If IVL7-0 bits are written during PMADC bit = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADC bit is changed to "1".

IVL7-0	GAIN (dB)	Step	
F1H	+36.0	0.375dB	
F0H	+35.625		
EFH	+35.25		
:	:		
92H	+0.375		
91H	0.0		Default
90H	–0.375		
:	:		
03H	–53.25		
02H	–53.625		
01H	–54		
00H	MUTE		

Table 29. Input Digital Volume Setting

When writing to the IVL7-0 bits continuouslly, the control register should be written by an interval more than zero crossing timeout. If not, IVL is not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVL, this write operation is ignored and zero crossing counter is not reset. Therefore, IVL can be written by an interval less than zero crossing timeout.

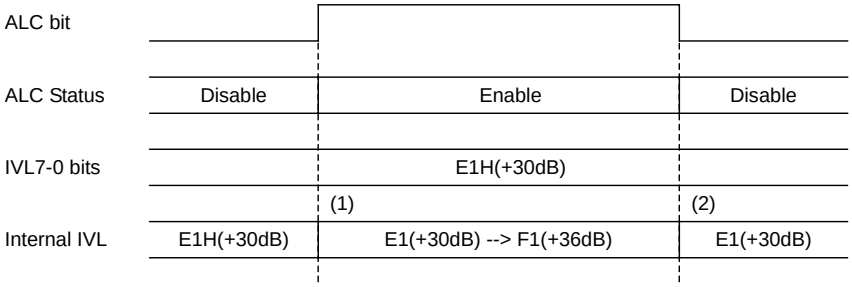


Figure 36. IVOL value during ALC operation

(1) The wait time from ALC bit = "1" to ALC operation start by IVL7-0 bits is at most recovery time (WTM1-0 bits) plus zerocross timeout period (ZTM1-0 bits).
(2) Writing to IVL register (18H) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" by an interval more than zero crossing timeout period after ALC bit = "0".

■ System Reset

Upon power-up, the AK5700 should be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADC bit is changed from "0" to "1". The initialization cycle time is 3088/fs=70.0ms@fs=44.1kHz when HPF1-0 bits are "00" (see Table 30). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's complement, "0". The ADC output reflects the analog input signal after the initialization cycle is complete.

HPF1 bit	HPF0 bit	Init Cycle				
		Cycle	fs=44.1kHz	fs=22.05kHz	fs=11.025kHz	
0	0	3088/fs	70.0ms (Recommendation)	140.0ms	280.1ms	Default
0	1	1552/fs	35.2ms	70.4ms (Recommendation)	140.8ms	
1	0	784/fs	17.8ms	35.6ms	71.1ms (Recommendation)	
1	1	N/A	N/A	N/A	N/A	

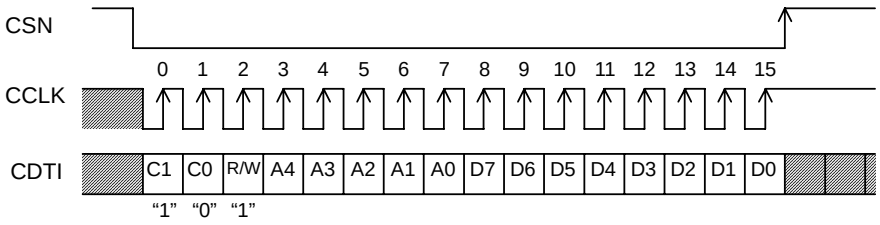
Table 30. ADC Initialization Cycle

■ Serial Control Interface

Internal registers may be written by using the 3-wire μP interface pins (CSN, CCLK and CDTI). CSP pin selects the polarity of CSN pin and chip address.

1) CSP pin = "L"

The data on this interface consists of a 2-bit Chip address (Fixed to "10"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN falling edge("↓"). Clock speed of CCLK is 7MHz (max). The value of internal registers are initialized by PDN pin = "L".

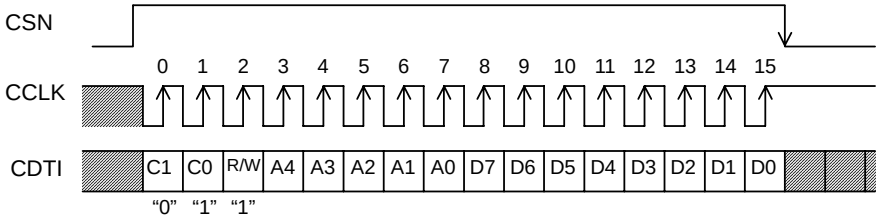


C1-C0: Chip Address (C1 = "1", C0 = "0"); Fixed to "10"
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0: Register Address
D7-D0: Control data

Figure 37. Serial Control I/F Timing (CSP pin = "L")

2) CSP pin = "H"

The data on this interface consists of a 2-bit Chip address (Fixed to "01"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN rising edge("↑"). Clock speed of CCLK is 7MHz (max). The value of internal registers are initialized by PDN pin = "L".



C1-C0: Chip Address (C1 = "0", C0 = "1"); Fixed to "01"
R/W: READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0: Register Address
D7-D0: Control data

Figure 38. Serial Control I/F Timing (CSP pin = "H")

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management	0	0	0	0	0	PMVCM	0	PMADC
11H	PLL Control	0	0	PLL3	PLL2	PLL1	PLL0	M/S	PMPLL
12H	Signal Select	0	0	0	PMMP	0	MDIF1	0	AIN
13H	Mic Gain Control	0	0	0	0	0	0	MGAIN1	MGAIN0
14H	Audio Format Select	0	0	1	0	MSBS	BCKP	DIF1	DIF0
15H	fs Select	HPF1	HPF0	BCKO1	BCKO0	FS3	FS2	FS1	FS0
16H	Clock Output Select	0	0	0	0	THR	MCKO	PS1	PS0
17H	Reserved	0	0	0	0	0	0	0	1
18H	Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
19H	Reserved	1	0	0	1	0	0	0	1
1AH	Timer Select	0	0	0	0	ZTM1	ZTM0	WTM1	WTM0
1BH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
1CH	ALC Mode Control 2	ALC	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
1DH	Mode Control 1	TE3	TE2	TE1	TE0	0	0	0	0
1EH	Mode Control 2	0	0	0	0	0	0	TMASTER	0

Note 26. PDN pin = “L” resets the registers to their default values.
Note 27. “0” must be sent to the register written as “0” and “1” must be sent to the register written as “1”. For addresses except for 10H to 1EH, data must not be written.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	Power Management	0	0	0	0	0	PMVCM	0	PMADC
Default		0	0	0	0	0	0	0	0

PMADC: MIC-Amp and ADC Power Management
0: Power down (Default)
1: Power up
When the PMADC bit is changed from "0" to "1", the initialization cycle (3088/fs=70.0ms@fs= 44.1kHz, HPF1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMVCM: VCOM Power Management
0: Power down (Default)
1: Power up
When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when PMADC=PMPLL=PMMP=MCKO bits = "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMADC, PMPLL and MCKO bits are "0", all blocks are powered-down. The register values remain unchanged. Power supply current is 20μA(typ) in this case. For fully shut down (typ. 1μA), PDN pin should be "L".

When the ADC is not used, external clocks may not be present. When ADC is used, external clocks must always be present.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	PLL Control	0	0	PLL3	PLL2	PLL1	PLL0	M/S	PMPLL
Default		0	0	1	0	0	1	0	0

PMPLL: PLL Power Management
0: EXT Mode and Power Down (Default)
1: PLL Mode and Power up

M/S: Master / Slave Mode Select
0: Slave Mode (Default)
1: Master Mode

PLL3-0: PLL Reference Clock Select (See Table 4)
Default: "1001"(MCKI pin=12MHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	Signal Select	0	0	0	PMMP	0	MDIF1	0	AIN
	Default	0	0	0	0	0	0	0	0

AIN: ADC Input Source Select
0: AIN1 pin (Default)
1: AIN2 pin

MDIF1: ADC Input Type Select
0: Single-ended input (AIN1/AIN2 pin: Default)
1: Full-differential input (AIN+/AIN– pin)

PMMP: MPWR pin Power Management
0: Power down: Hi-Z (Default)
1: Power up

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
13H	Mic Gain Control	0	0	0	0	0	0	MGAIN1	MGAIN0
	Default	0	0	0	0	0	0	0	1

MGAIN1-0: MIC-Amp Gain Control (See Table 20)
Default: “01”(+15dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
14H	Audio Format Select	0	0	1	0	MSBS	BCKP	DIF1	DIF0
	Default	0	0	1	0	0	0	1	1

DIF1-0: Audio Interface Format (See Table 15)
Default: “11” (I^2S)

BCKP: BCLK/EXBCLK Polarity at DSP Mode (See Table 16)
“0”: SDTO is output by the rising edge (“↑”) of BCLK/EXBCLK. (Default)
“1”: SDTO is output by the falling edge (“↓”) of BCLK/EXBCLK.

MSBS: LRCK/EXLRCK Polarity at DSP Mode (See Table 16)
“0”: The rising edge (“↑”) of LRCK/EXLRCK is half clock of BCLK/EXBCLK before the channel change. (Default)
“1”: The rising edge (“↑”) of LRCK/EXLRCK is one clock of BCLK/EXBCLK before the channel change.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
15H	fs Select	HPF1	HPF0	BCKO1	BCKO0	FS3	FS2	FS1	FS0
	Default	0	0	0	1	1	1	1	1

FS3-0: Sampling Frequency Select (See Table 5 and Table 6) and MCKI Frequency Select (See Table 11)
Default: "1111" (44.1kHz)
FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKO1-0: BCLK Output Frequency Select at Master Mode (See Table 10)
Default: "01" (32fs)

HPF1-0: Offset Cancel HPF Cut-off Frequency and ADC Initialization Cycle (See Table 17, Table 30)
Default: "00" (fc=3.4Hz@fs=44.1kHz, Init Cycle=3088/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
16H	Clock Output Select	0	0	0	0	THR	MCKO	PS1	PS0
	Default	0	0	0	0	0	0	0	0

PS1-0: MCKO Output Frequency Select (See Table 9)
Default: "00"(256fs)

MCKO: Master Clock Output Enable
0: Disable: MCKO pin = "L" (Default)
1: Enable: Output frequency is selected by PS1-0 bits.

THR: Bypass Mode (Table 14)
0: OFF (Default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
18H	Input Volume Control	IVL7	IVL6	IVL5	IVL4	IVL3	IVL2	IVL1	IVL0
	Default	1	0	0	1	0	0	0	1

IVL7-0: Input Digital Volume; 0.375dB step, 242 Level (See Table 29)
Default: "91H" (0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1AH	Timer Select	0	0	0	0	ZTM1	ZTM0	WTM1	WTM0
	Default	0	0	0	0	0	0	0	0

WTM1-0: ALC Recovery Waiting Period (see Table 25)
Default: "00" (128/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (see Table 24)
Default: "00" (128/fs)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1BH	ALC Mode Control 1	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
	Default	1	1	1	0	0	0	0	1

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (See Table 27)
Default: "E1H" (+30.0dB)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1CH	ALC Mode Control 2	ALC	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH1	LMTH0
	Default	0	0	0	0	0	0	0	0

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (see Table 22)
Default: "00"

RGAIN1-0: ALC Recovery GAIN Step (see Table 26)
Default: "00"

LMAT1-0: ALC Limiter ATT Step (see Table 23)
Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (Default)
1: Disable

ALC: ALC Enable
0: ALC Disable (Default)
1: ALC Enable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1DH	Mode Control 1	TE3	TE2	TE1	TE0	0	0	0	0
Default		1	0	1	0	0	0	0	0

TE3-0: EXT Master Mode Enable

When TE3-0 bits is set to "0101", the write operation to addr=1EH is enabled.
TE3-0 bits should be set to "1010" except for EXT Master Mode.
TE3-0 bits must not be set to the value except for "1010" and "0101".
Default: "1010"

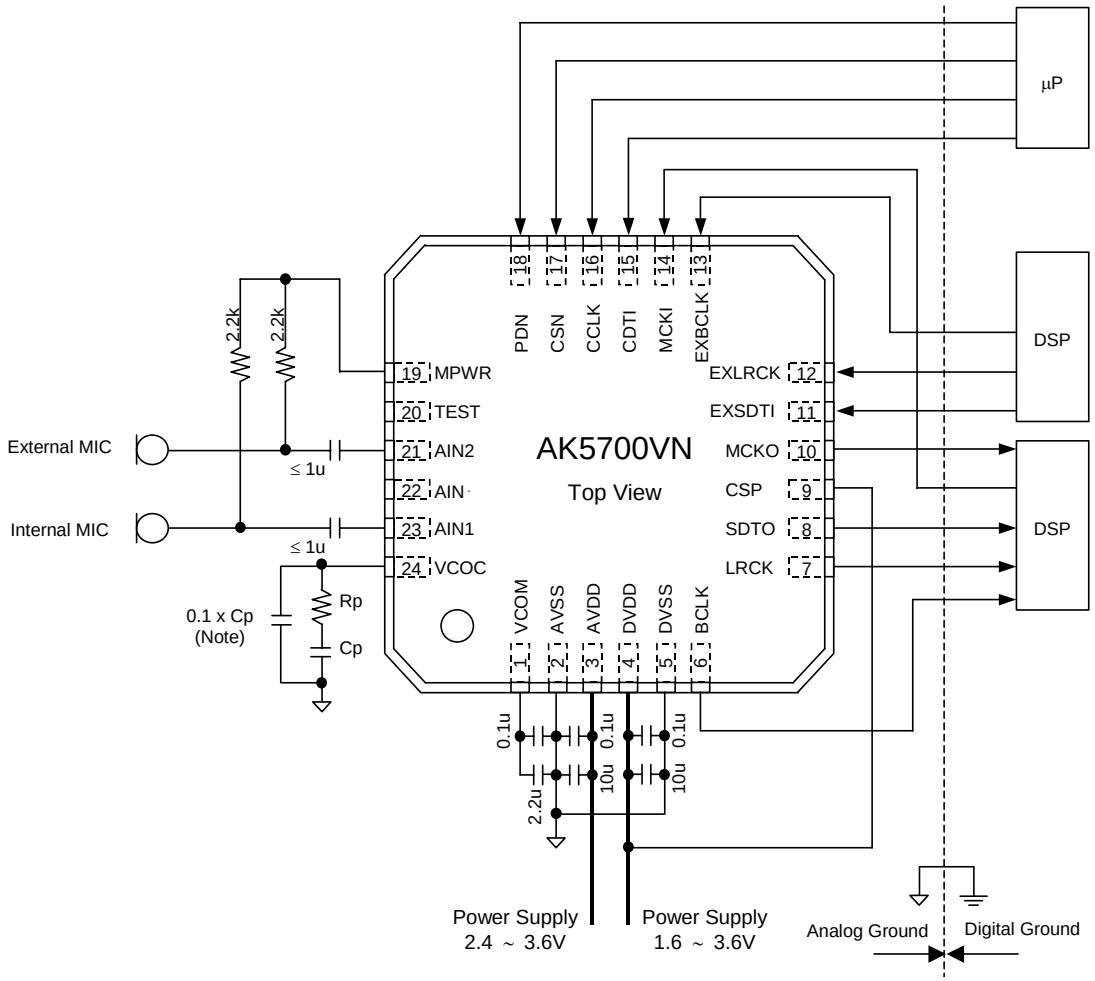
Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
1EH	Mode Control 2	0	0	0	0	0	0	TMASTER	0
Default		0	0	0	0	0	0	0	0

TMASTER: EXT Master Mode

The write operation to TMASTER bit is enabled when TE3-0 bits = "0101".
0: Except EXT Master Mode (Default)
1: EXT Master Mode

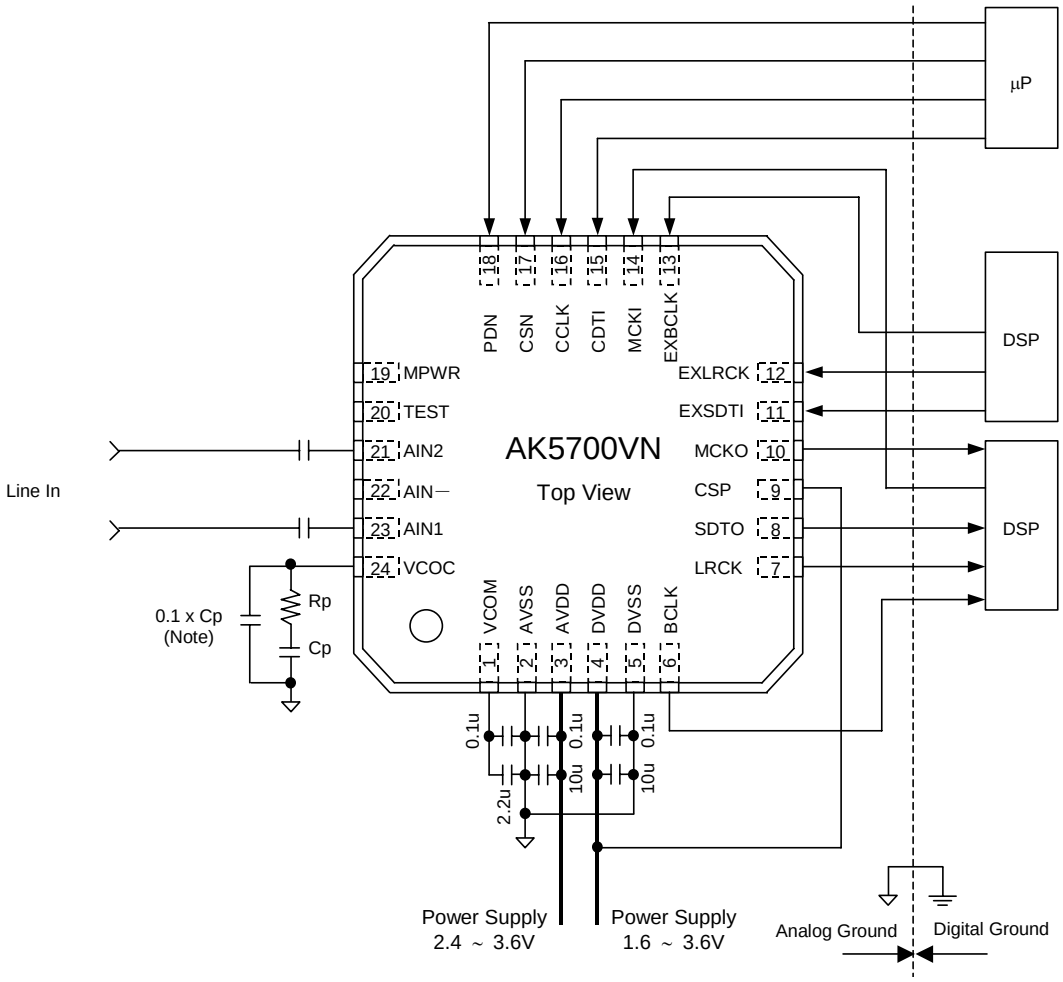
SYSTEM DESIGN

Figure 39 and Figure 40 shows the system connection diagram for the AK5700. An evaluation board [AKD5700] is available which demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:
- AVSS and DVSS of the AK5700 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5700 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK5700 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.
- Mic input AC coupling capacitor should be 1μF or less to start the recording within 100ms.

Figure 39. Typical Connection Diagram (MIC Input)



Notes:
- AVSS and DVSS of the AK5700 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5700 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of VCOC pin is not needed.
- When the AK5700 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.

Figure 40. Typical Connection Diagram (Line Input)

1. Grounding and Power Supply Decoupling

The AK5700 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the system's analog supply. If AVDD and DVDD are supplied separately, the power-up sequence is not critical. AVSS and DVSS of the AK5700 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5700 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5700.

3. Analog Inputs

The analog inputs are single-ended or full-differential and input resistance is 60kΩ (typ)@MGAIN1-0 bits = "00", 30kΩ (typ)@MGAIN1-0 bits = "01" or "10". The input signal range scales with 0.6 x AVDD Vpp(typ)@MGAIN 1-0 bits = "00" centered around the internal common voltage (0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is fc = (1/2πRC). The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF (fc=3.4Hz@ HPF1-0 bits = "00", fs=44.1kHz). The AK5700 can accept input voltages from AVSS to AVDD at single-ended.

CONTROL SEQUENCE

■ Clock Set up

When ADC is powered-up, the clocks must be supplied.

1. PLL Master Mode.

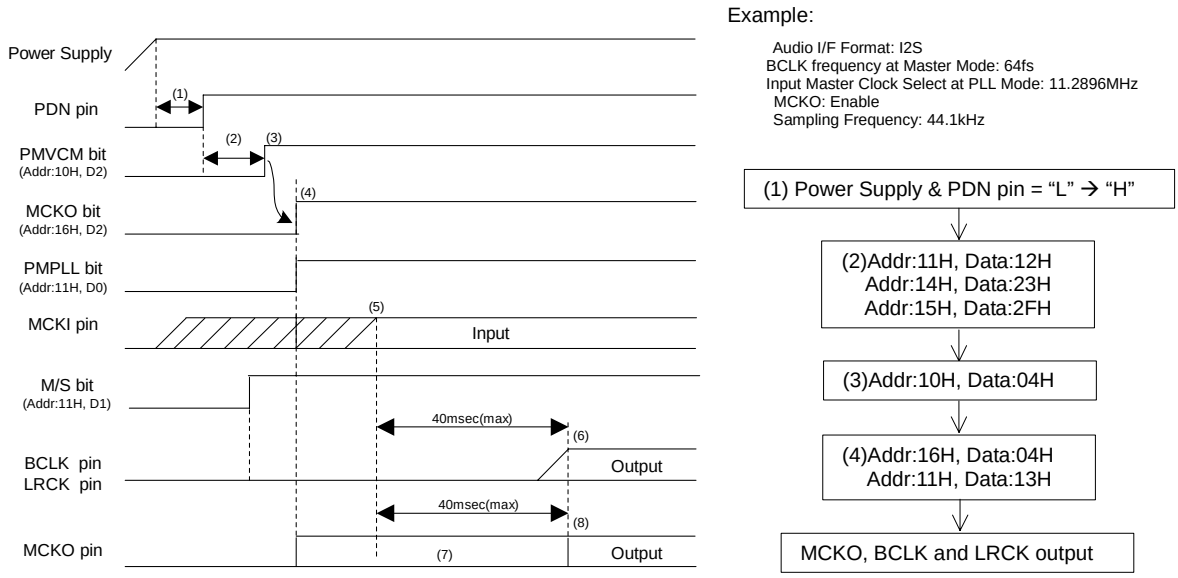


Figure 41. Clock Set Up Sequence (1)

<Example>

(1) After Power Up, PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.

(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period as follows.
(2a) M/S bit = "1" and setting of PLL3-0, FS3-0, BCKO1-0 bits.
(2b) Setting of DIF1-0 bits.

(3) Power UpVCOM: PMVCM bit = "0" → "1"
VCOM should first be powered-up before the other block operates.

(4) In case of using MCKO output: MCKO bit = "1"
In case of not using MCKO output: MCKO bit = "0"

(5) PLL operation starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source. PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).

(6) The AK5700 starts to output the LRCK and BCLK clocks after the PLL becomes stable. Then normal operation starts.

(7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".

(8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (EXLRCK or EXBCLK pin)

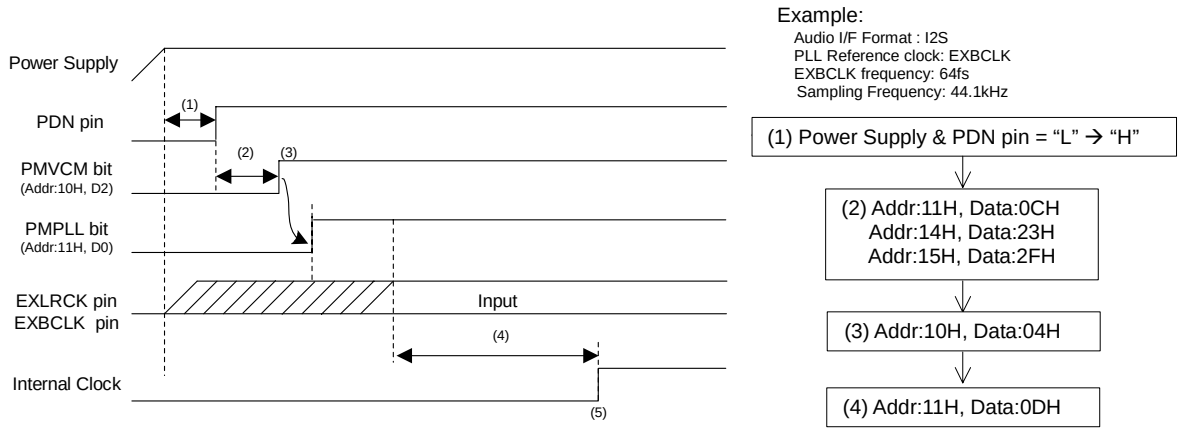


Figure 42. Clock Set Up Sequence (2)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.

(2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (EXLRCK or EXBCLK pin) is supplied. PLL lock time is 160ms(max) when EXLRCK is a PLL reference clock. PLL lock time is 2ms(max) when EXBCLK is a PLL reference clock and the external circuit at VCOC pin is 10k+4.7nF (Table 4).

(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

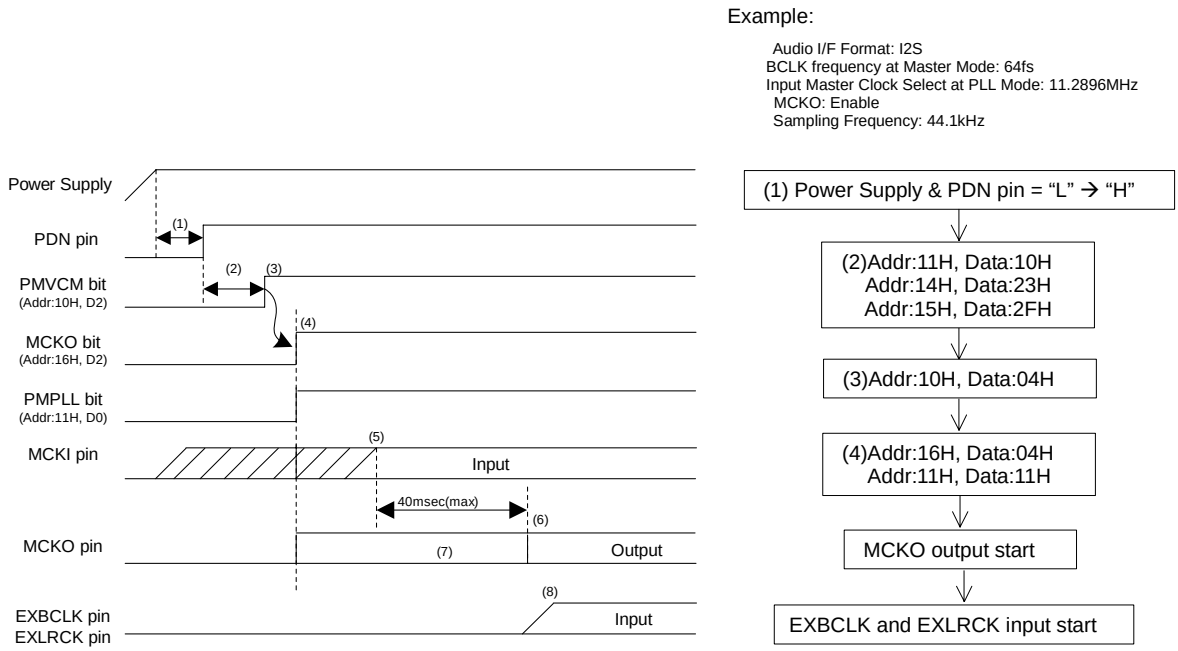


Figure 43. Clock Set Up Sequence (3)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.
(2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Enable MCKO output: MCKO bit = "1"
(5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).
(6) The normal clock is output from MCKO after PLL is locked.
(7) The invalid frequency is output from MCKO during this period.
(8) EXBCLK and EXLRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

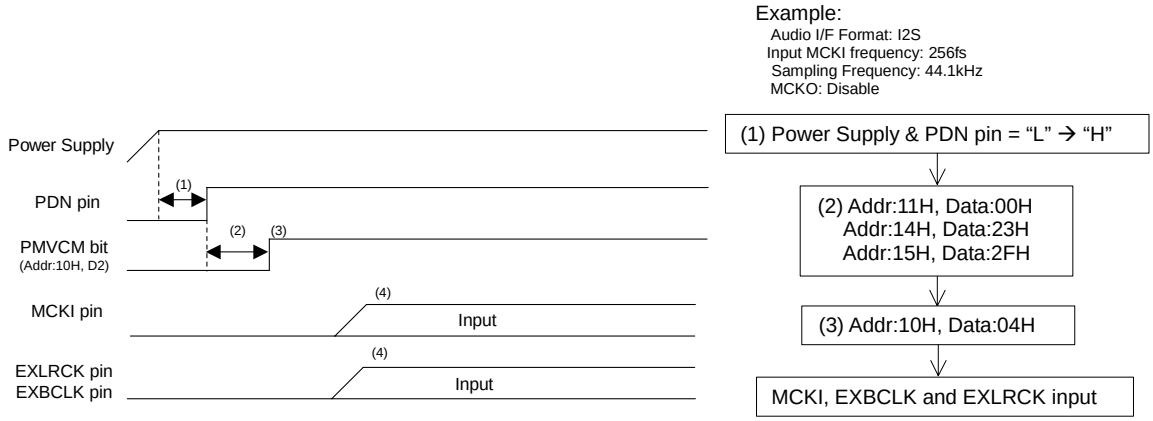


Figure 44. Clock Set Up Sequence (4)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.
(2) DIF1-0 and FS1-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Normal operation starts after the MCKI, EXLRCK and EXBCLK are supplied.

5. EXT Master Mode

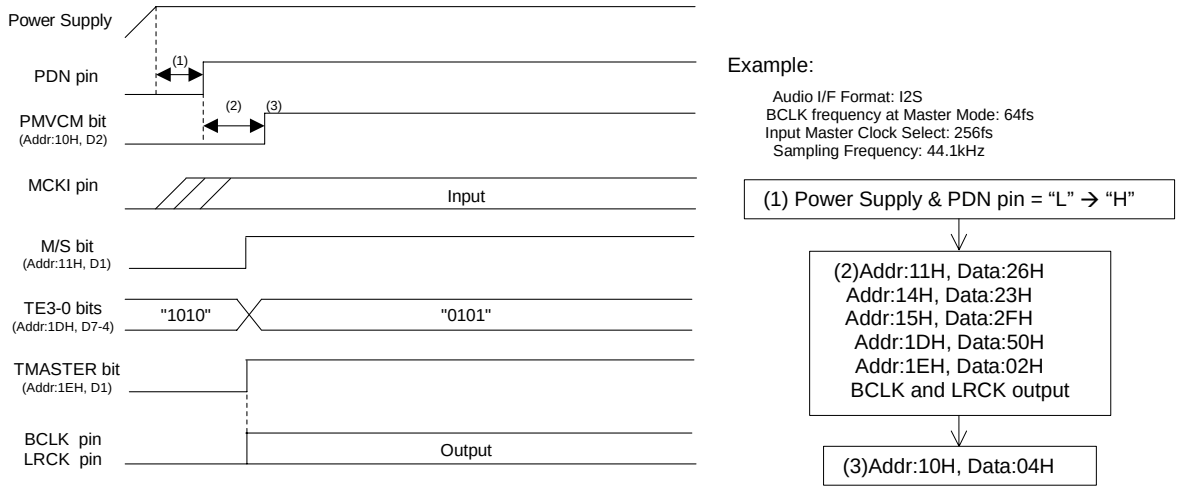


Figure 45. Clock Set Up Sequence (5)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.
(2) DIF1-0, FS1-0, BCKO1-0, M/S, TE3-0 and TMASTER bits should be set during this period as follows.
(2a) M/S bit = "1", setting of FS3-0 and BCKO1-0 bits.
(2b) Setting of DIF1-0 bits.
(2c) TE3-0 bits = "0101"
(2d) TMASTER bit = "1": BCLK and LRCK start to output.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

When the clock mode is changed from EXT Master Mode to other modes, the register should be set as above table after PDN pin = "L" to "H" or TE3-0 bits = "1010".

6. Slave & Bypass Mode

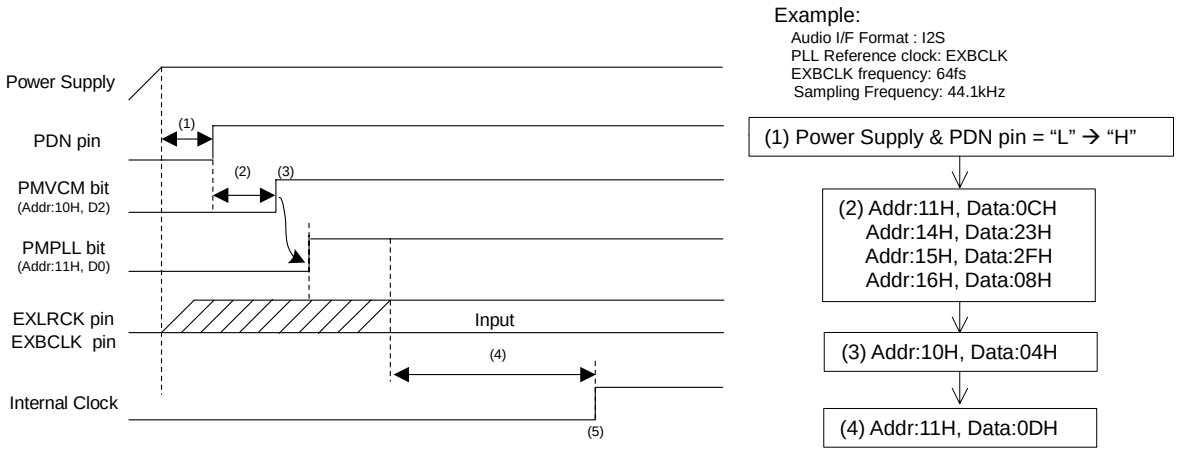


Figure 46. Clock Set Up Sequence (6)

<Example>

(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.

(2) THR bit should be set to "1" and DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.

(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.

(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (EXLRCK or EXBCLK pin) is supplied. PLL lock time is 160ms(max) when EXLRCK is a PLL reference clock. PLL lock time is 2ms(max) when EXBCLK is a PLL reference clock and the external circuit at VCOC pin is 10k+4.7nF (Table 4).

(5) Normal operation stats after that the PLL is locked.

7. Bypass Mode

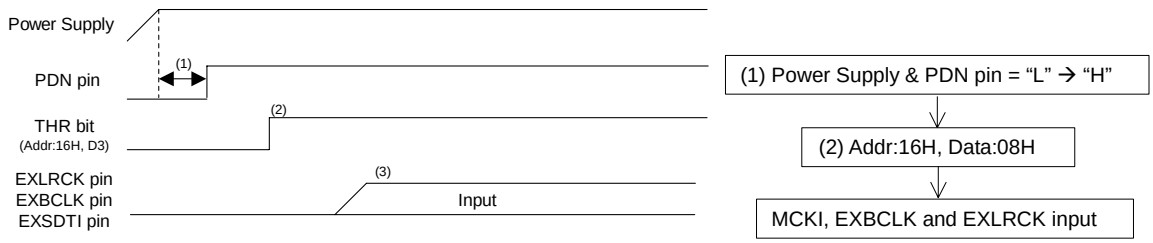


Figure 47. Clock Set Up Sequence (7)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5700.
(2) THR bit should be set to "1".
(3) After EXLRCK, EXBCLK and EXSDTI are input, LRCK, BCLK and SDTO start to output.

■ MIC Input Recording

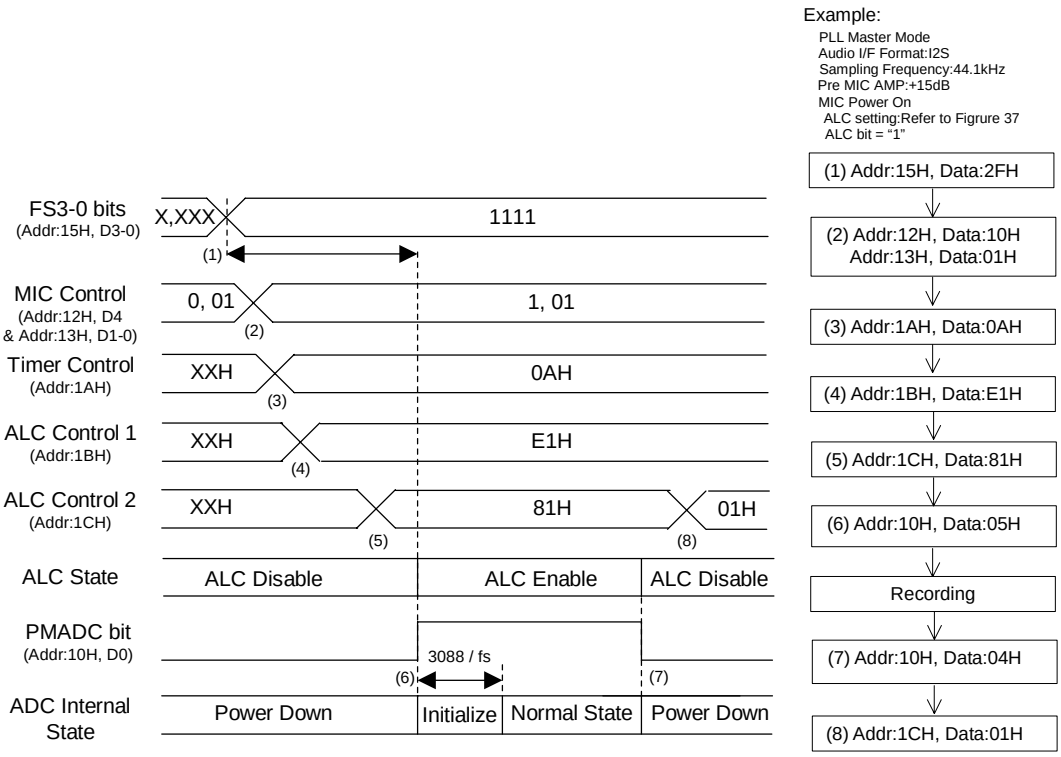


Figure 48. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC setting at fs=44.1kHz. If the parameter of the ALC is changed, please refer to "Figure 35. Registers set-up sequence at ALC operation".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK5700 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 12H&13H)

(3) Set up Timer Select for ALC (Addr: 1AH)

(4) Set up REF value for ALC (Addr: 1BH)

(5) Set up LMTH1-0, RGAIN1-0, LMAT1-0 and ALC bits (Addr: 1CH)

(6) Power Up MIC and ADC: PMADC bit = "0" → "1"
The initialization cycle time of ADC is 3088/fs=70.0ms@fs=44.1kHz, HPF1-0 bits = "00".
After the ALC bit is set to "1" and MIC&ADC block is powered-up, the ALC operation starts from IVOL default value (0dB).
To start the recording within 100ms, the following sequence is required.
(6a) PMVCM=PMMP bits = "1".
(6b) Wait for 2ms, then PMPLL bit = "1".
(6c) Wait for 6ms, then PMADC bit = "1".

(7) Power Down MIC and ADC: PMADC bit = "1" → "0"
When the registers for the ALC operation are not changed, ALC bit may be keeping "1". The ALC operation is disabled because the MIC&ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK5700 goes to the manual mode (ALC bit = "0") or MIC&ADC block is powered-down (PMADC bit = "0"). IVOL gain is not reset when PMADC = "0", and then IVOL operation starts from the setting value when PMADC bit is changed to "1".

(8) ALC Disable: ALC bit = "1" → "0"

■ Stop of Clock

Master clock can be stopped when ADC is not used.

1. PLL Master Mode

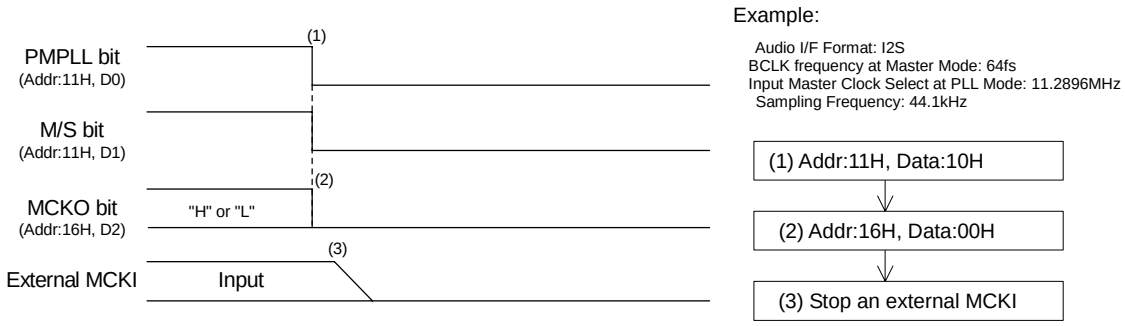


Figure 49. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL=M/S bits = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

2. PLL Slave Mode (EXLRCK, EXBCLK pin)

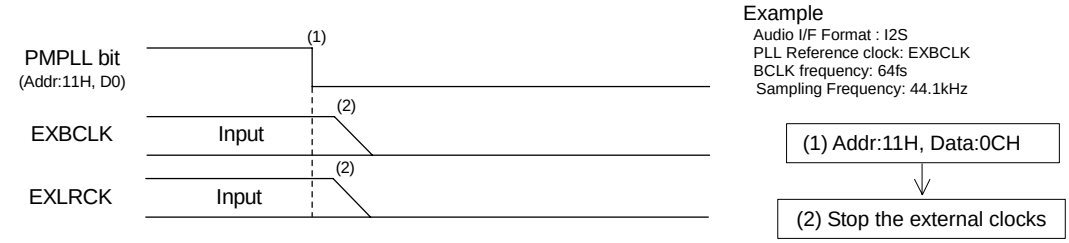


Figure 50. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external EXBCLK and EXLRCK clocks

* Clock stop sequence is the same for Slave&Bypass Mode.

3. PLL Slave Mode (MCKI pin)

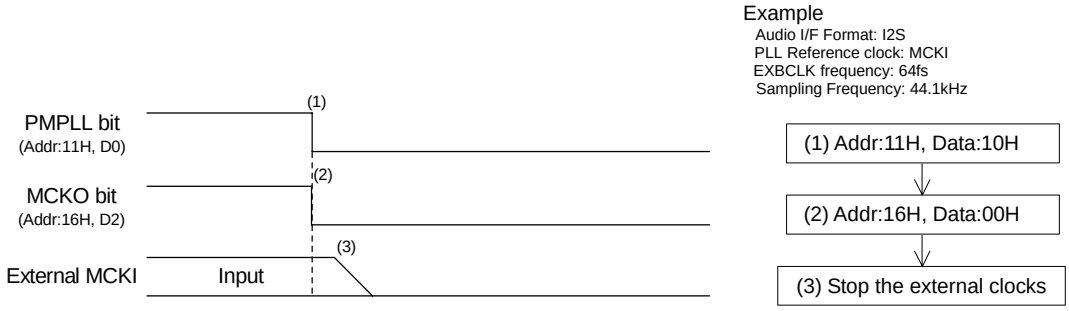


Figure 51. Clock Stopping Sequence (3)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop MCKO output: MCKO bit = "1" → "0"
(3) Stop the external master clock.

4. EXT Slave Mode

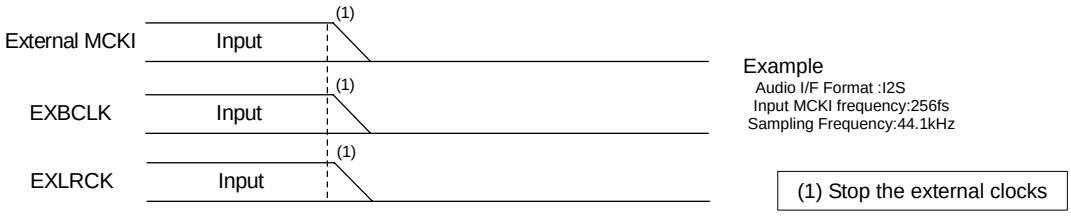


Figure 52. Clock Stopping Sequence (4)

<Example>
(1) Stop the external MCKI, EXBCLK and EXLRCK clocks.

* Clock stop sequence is the same for Bypass Mode.

5. EXT Master Mode

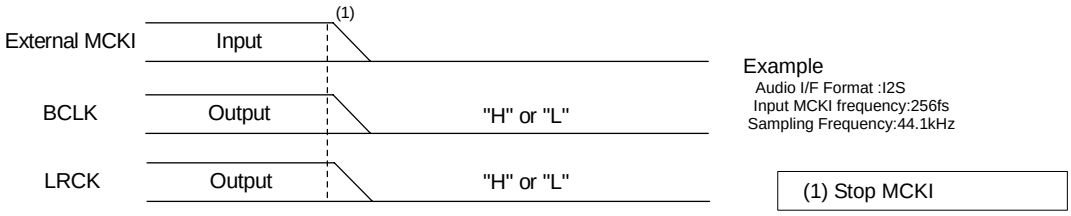


Figure 53. Clock Stopping Sequence (5)

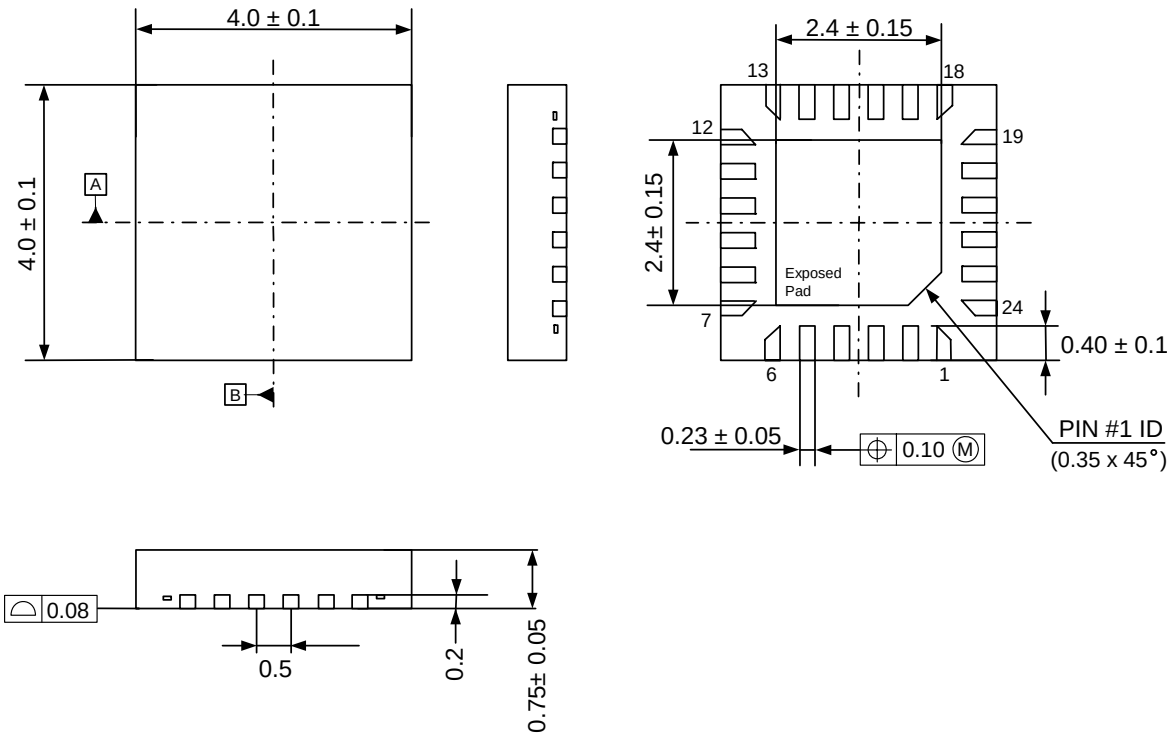
<Example>
(1) Stop MCKI. BCLK and LRCK are fixed to "H" or "L".

■ Power down

Power supply current is typ. 20μA by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting PDN pin = "L". When PDN pin = "L", the registers are initialized.

PACKAGE

● 24pin QFN (Unit: mm)

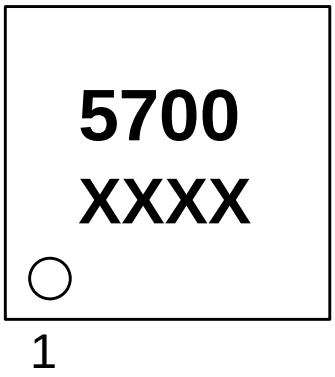


Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.

■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXX : Date code identifier (4 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/11/16	00	First Edition		
06/12/25	01	Error correct	40	Register Map (Addr=17H) Bit (D0) value was changed: 0 → 1