XC6601 Series

ETR0335_002

Low Voltage Input LDO Voltage Regulators

Preliminary

■GENERAL DESCRIPTION

The XC6601 series is a CMOS LDO voltage regulator with precise (±20mV) outputs which enables the operation in ultra low On resistance even where low output voltages to achieve high efficiency of the output current. The series is suited for the application which requires low dropout voltage operation. The series consists of a voltage reference, an error amplifier, a driver transistor, a current limiter, a fold back circuit, a thermal shutdown (TSD) circuit, a Under Voltage Lock Out (U.V.L.O.) and a phase compensation circuit.

The output voltage is selectable in 50mV increments within the range of 0.7V to 1.8V using laser trimming technologies. The output stabilization capacitor (C_L) is also compatible with low ESR ceramic capacitors.

The over current protection circuit (the current limiter and the fold back circuit) and the thermal shutdown circuit (the TSD circuit) are built-in. These two protection circuits will operate when the output current reaches limit level or the junction temperature reaches temperature limit level.

With the built-in U.V.L.O. function, the regulator output is forced OFF when the V_{BIAS} pin or the V_{IN} pin becomes the U.V.L.O. voltage or lower.

The CE function enables the output to be turned off and the series becomes a stand-by mode resulting in greatly reduced power consumption. At the time of entering the stand-by mode, the series enables the electric charge at the output capacitor (C_L) to be discharged via the internal auto-discharge switch placed between the V_{OUT} pin and the V_{SS} pin, as a result the V_{OUT} pin quickly returns to the V_{SS} level.

■APPLICATIONS

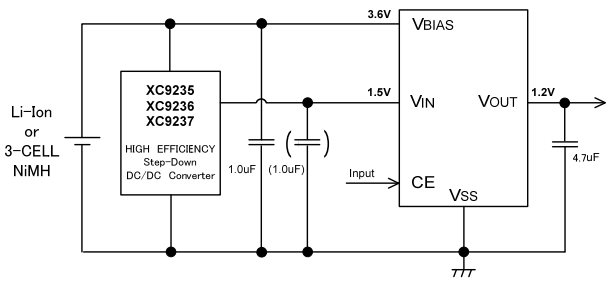
- ●Mobile phones
- ●Cordless phones
- ●Wireless communication equipment
- ●Portable games
- ●Cameras
- ●Audio visual equipment
- ●Portable AV equipment
- ●PDAs

■FEATURES

Maximum Output Current	: 400mA (Limiter 500mA TYP.)
Dropout Voltage	: 35mV@I_{OUT}=100mA (TYP.) (at V_{BIAS} - $V_{OUT(E)}$=2.4V)
Bias Voltage Range	: 2.5V ~ 6.0V (V_{BIAS} - $V_{OUT(E)}$≧0.9V)
Input Voltage Range	: 1.0V ~ 3.0V (V_{IN}≦V_{BIAS})
Output Voltage Range	: 0.7V ~ 1.8V (50mV increments)
Output Voltage Accuracy	:±20mV
Power Consumption	: I_{BIAS}=25μA , I_{IN}=1.0μA (TYP.) : I_{BIAS}=0.01μA , I_{IN}=0.01μA (TYP.)
U.V.L.O.	: V_{BIAS}=2.0V, V_{IN}=0.4V (TYP.)
TSD (Detect/Release)	:150℃/125℃ (TYP.)
Operating Temperature Range	: -40℃ ~ 85℃
C_L High Speed Auto-Discharge	
Low ESR Capacitor	: Ceramic Capacitor Compatible
Packages	: USP-6C, SOT-25, SOT-89-5

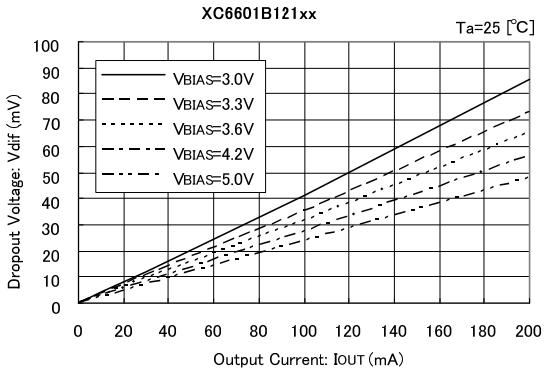
■ TYPICAL APPLICATION CIRCUIT

●V_{BIAS} =3.6V , V_{IN} =1.5V , V_{OUT} =1.2V



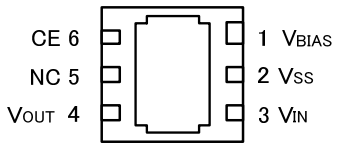
■ TYPICAL PEFORMANCE CHARACTERISTICS

●Dropout Voltage vs. Output Current



■PIN CONFIGURATIOIN

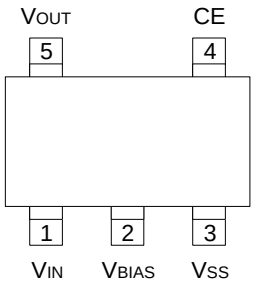
●USP-6C



USP-6C
(BOTTOM VIEW)

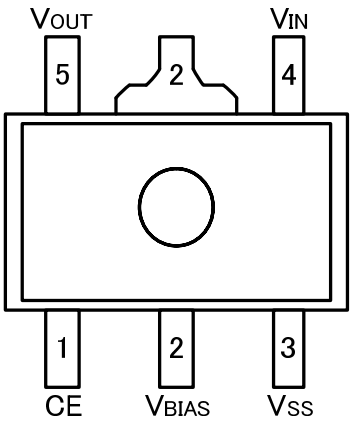
*The heat dissipation pad of the USP-6C package is recommended to solder as the recommended mount pattern and metal mask pattern for mounting strength. The mount pattern should be electrically opened or connected to the VBIAS (No.1) pin.

●SOT-25



SOT-25
(TOP VIEW)

●SOT-89-5



SOT-89-5
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTION
USP-6C	SOT-25	SOT-89-5		
1	2	2	VBIAS	Power Supply Input
3	1	4	VIN	Driver Transistor Input
4	5	5	VOUT	Output
2	3	3	VSS	Ground
6	4	1	CE	ON/OFF Control

■PRODUCT CLASSIFICATION

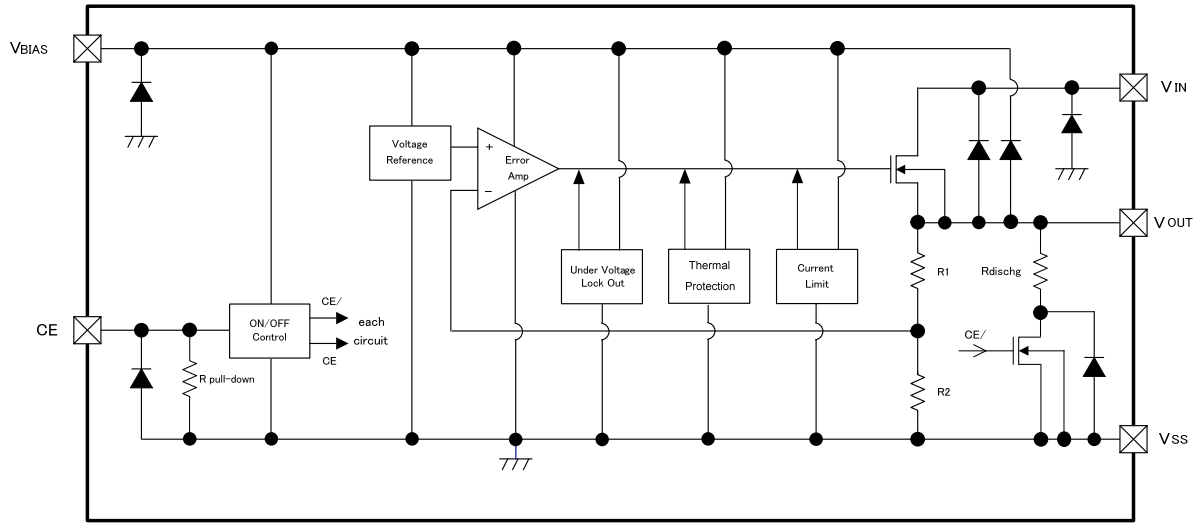
●Ordering Information

XC6601①②③④⑤⑥

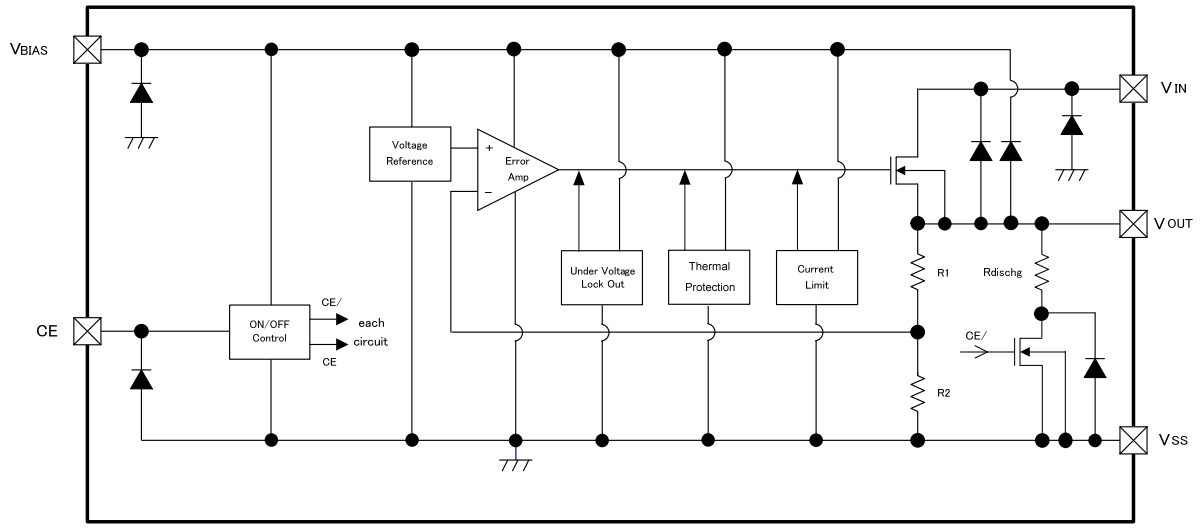
MARK	DESCRIPTION	SYMBOL	DESCRIPTION
①	Type of Regulators	A	: CE High Active, Pull-Down Resistor Built-in, CL Auto Discharge Function
		B	: CE High Active, No Pull-Down Resistor Built-in, CL Auto Discharge Function
②③	Output Voltage	07 ~ 18	: e.g.) VOUT(T)=1.2V⇒②=1,③=2
④	Output Voltage Accuracy	1	: 100mV increments, ±20mV accuracy e.g.) 1.2V⇒②=1,③=2,④=1
		B	: 50mV increments, ±20mV accuracy e.g.) 1.25V⇒②=1,③=2,④=B
⑤	Packages	M	: SOT-25
		E	: USP-6C
		P	: SOT-89-5
⑥	Device Orientation	R	: Embossed Tape (Standard Feed)
		L	: Embossed Tape (Reverse Feed)

■BLOCK DIAGRAMS

(1) XC6601A Series



(2) XC6601B Series



*Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■MAXIMUM ABSOLUTE RATINGS

Ta=25 ℃

PARAMETER		SYMBOL	RATINGS	UNITS
Bias Voltage		V_{BIAS}	V_{SS}-0.3 ~ +7.0	V
Input Voltage		V_{IN}	V_{SS}-0.3 ~ +7.0	V
Output Current		I_{OUT}	700 (*1)	mA
Output Voltage		V_{OUT}	V_{SS}-0.3 ~ V_{BIAS}+0.3	V
			V_{SS}-0.3 ~ V_{IN}+0.3	
CE Input Voltage		V_{CE}	V_{SS}-0.3 ~ +7.0	V
Power Dissipation	USP-6C	Pd	120	mW
	SOT-25		250	
	SOT-89-5		500	
Operating Temperature Range		Topr	-40 ~ +85	℃
Storage Temperature Range		Tstg	-55 ~ +125	℃

(*1) I_{OUT}=Less than Pd / (V_{IN}-V_{OUT})

■ELECTRICAL CHARACTERISTICS

Ta=25 ℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Bias Voltage (*1)	V_{BIAS}	V_{CE} =V_{BIAS}, V_{IN} =$V_{OUT(T)}$+0.3V	2.5	-	6.0	V	①
Input Voltage (*2)	V_{IN}	V_{BIAS}=V_{CE}=3.6V	1.0	-	3.0	V	①
Output Voltage	$V_{OUT(E)}$ (*3)	V_{BIAS}=V_{CE}=3.6V, V_{IN} =$V_{OUT(T)}$+0.3V, I_{OUT}=1mA	-0.02	$V_{OUT(T)}$ (*4)	+0.02	V	①
			E-0 (*5)				
Maximum Output Current	I_{OUTMAX}	V_{BIAS}=V_{CE}=3.6V, V_{IN} =$V_{OUT(T)}$+0.3V	400	-	-	mA	①
Load Regulation	△V_{OUT}	V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V, 1mA≦I_{OUT}≦100mA	-	10	-	mV	①
Dropout Voltage	Vdif (*7)	V_{BIAS}=V_{CE}, I_{OUT}=100mA	E-1 (*6)			mV	①
Supply Current 1	I_{BIAS}	V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V V_{OUT}=OPEN	-	25	-	μA	①
Supply Current 2	I_{IN}	V_{BIAS}=V_{CE}=3.6V, V_{IN}=$V_{OUT(T)}$+0.3V V_{OUT}=OPEN	-	1.0	-	μA	①
Bias Current (*10)	$I_{BIASMAX}$	$V_{OUT(T)}$≧0.95V, V_{BIAS}=CE=3.6V, V_{IN}=$V_{OUT(T)}$+0.05V, V_{OUT}=$V_{OUT(T)}$ - 0.05V	-	2.0	-	mA	①
		$V_{OUT(T)}$＜0.95V, V_{BIAS}=CE=3.6V, V_{IN}=1.0V V_{OUT}= $V_{OUT(T)}$ - 0.05V					
Stand-by Current 1	I_{BIAS_STB}	V_{BIAS}=6.0V, V_{IN}=3.0V, V_{CE}=V_{SS}	-	0.01	-	μA	①
Stand-by Current 2	I_{IN_STB}	V_{BIAS}=6.0V, V_{IN}=3.0V, V_{CE}=V_{SS}	-	0.01	-	μA	①
Bias Regulation	△V_{OUT}/ △V_{BIAS} • V_{OUT}	2.5V≦V_{BIAS}≦6.0V, V_{IN}=$V_{OUT(T)}$+0.3V, V_{BIAS}=V_{CE}, I_{OUT}=1mA	-	0.01	-	%/V	①
Input Regulation	△V_{OUT}/ △V_{IN} • V_{OUT}	$V_{OUT(T)}$≧0.90V, $V_{OUT(T)}$+0.1V≦V_{IN}≦3.0V, V_{BIAS}=V_{CE}=3.6V, I_{OUT}=1mA	-	0.01	-	%/V	①
		$V_{OUT(T)}$＜0.90V, 1.0V≦V_{IN}≦3.0V V_{BIAS}=V_{CE}=3.6V, I_{OUT}=1mA					
Bias Voltage U.V.L.O.	V_{BIAS_UVLO}	V_{CE} =V_{BIAS}, V_{IN} =$V_{OUT(T)}$+0.3V, I_{OUT}=1mA	-	2.0	-	V	①
Input Voltage U.V.L.O.	V_{IN_UVLO}	V_{BIAS}=V_{CE}=3.6V, I_{OUT}=1mA	-	0.4	-	V	①
V_{BIAS} Ripple Rejection	V_{BIAS_PSRR}	V_{BIAS}=3.6V_{DC}+0.2$V_{p\text{-}pAC}$, V_{IN}=$V_{OUT(T)}$+0.3V, I_{OUT}=30mA,f=1kHz	-	40	-	dB	②
V_{IN} Ripple Rejection	V_{IN_PSRR}	V_{IN}=$V_{OUT(T)}$+0.3V_{DC}+0.2$V_{p\text{-}pAC}$, V_{BIAS}=3.6V, I_{OUT}=30mA, f=1kHz	-	60	-	dB	②

■ELECTRICAL CHARACTERISTICS (Continued)

Ta=25 ℃

PARAMETER	SYNBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Output Voltage Temperature Characteristics	△VOUT/ △Topr • VOUT	VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V , IOUT=30mA, - 40℃≦ Topr ≦85℃	-	±100	-	ppm/ ℃	①
Limit Current	ILIM	VOUT=VOUT(E)×0.95, VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V	400	-	-	mA	①
Short Current	ISHORT	VBIAS=VCE=3.6V, VIN=VOUT(T)+0.3V, VOUT=0V	-	50	-	mA	①
Thermal Shutdown Detect Temperature	TTSD	Junction Temperature	-	150	-	℃	①
Thermal Shutdown Release Temperature	TTSR	Junction Temperature	-	125	-	℃	①
Hysteresis Width	TTSD−TTSR		-	25	-	℃	①
CL Auto-Discharge Resistance (*7)	Rdischg	VBIAS=3.6V, VIN= VOUT(T)+0.3V, VCE= VSS, VOUT=VOUT(T)	-	450	-	Ω	①
CE "H" Level Voltage	VCEH	VBIAS=3.6V, VIN= VOUT(T)+0.3V	1.0	-	6.0	V	①
CE "L" Level Voltage	VCEL	VBIAS=3.6V, VIN= VOUT(T)+0.3V		-	0.25	V	①
CE "H" Level Current (A Series)	ICEH	VBIAS=VCE=6.0V, VIN=VOUT(T)+0.3V	3.5	-	7.0	μA	①
CE "H" Level Current (B Series)			-0.1	-	0.1		
CE "L" Level Current	ICEL	VBIAS=6.0V, VCE=VSS VIN=VOUT(T)+0.3V	-0.1	-	0.1	μA	①

NOTE:
* 1: Please use Bias voltage V_{BIAS} within the range $V_{BIAS} - V_{OUT(E)} \geqq 0.9V$
* 2: Please use Input voltage V_{IN} within the range $V_{IN} \leqq V_{BIAS}$
* 3: VOUT(E) = Effective output voltage (Refer to the voltage chart E-0 and E-1)
* 4: VOUT (T) = Specified output voltage
* 5: E-0 = Please refer to the table named OUTPUT VOLTAGE CHART
* 6: E-1 = Please refer to the table named DROPOUT VOLTAGE CHART
* 7: Vdif = {VIN1(*8)-VOUT1(*9)}.
* 8: VIN1 = The input voltage when VOUT1 appears as input voltage is gradually decreased.
* 9: VOUT1 = A voltage equal to 98% of the output voltage while maintaining an amply stabilized output voltage when VIN=VOUT(T) +0.3V is input at the VIN pin.
* 10: IBIASMAX = A supply current at the V_{BIAS} pin providing for the output current (I_{OUT}) .

■OUTPUT VOLTAGE CHART

SETTING OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) VOUT	
VOUT(T)	MIN.	MAX.
0.70	0.680	0.720
0.75	0.730	0.770
0.80	0.780	0.820
0.85	0.830	0.870
0.90	0.880	0.920
0.95	0.930	0.970
1.00	0.980	1.020
1.05	1.030	1.070
1.10	1.080	1.120
1.15	1.130	1.170
1.20	1.180	1.220
1.25	1.230	1.270

SETTING OUTPUT VOLTAGE (V)	E-0 OUTPUT VOLTAGE (V) VOUT	
VOUT(T)	MIN.	MAX.
1.30	1.280	1.320
1.35	1.330	1.370
1.40	1.380	1.420
1.45	1.430	1.470
1.50	1.480	1.520
1.55	1.530	1.570
1.60	1.580	1.620
1.65	1.630	1.670
1.70	1.680	1.720
1.75	1.730	1.770
1.80	1.780	1.820

■DROPOUT VOLAGE CHART (Continued)

SETTING OUTPUT VOLTAGE (V)	E-1 DROPOUT VOLTAGE (mV) Vdif														
	VBIAS=3.0 (V)			VBIAS=3.3 (V)			VBIAS=3.6 (V)			VBIAS=4.2 (V)			VBIAS=5.0 (V)		
	Vgs (*1)	Vdif		Vgs	Vdif		Vgs	Vdif		Vgs	Vdif		Vgs	Vdif	
VOUT(T)		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.		TYP.	MAX.
0.70	2.30	36	-	2.60	33	-	2.90	31	-	3.50	28	-	4.30	26	-
0.75	2.25	37	-	2.55	34	-	2.85	31	-	3.45	28	-	4.25	26	-
0.80	2.20			2.50			2.80			3.40			4.20		
0.85	2.15	38	-	2.45	35	-	2.75	32	-	3.35	29	-	4.15	26	-
0.90	2.10			2.40			2.70			3.30			4.10		
0.95	2.05	40	-	2.35	36	-	2.65	33	-	3.25	29	-	4.05	26	-
1.00	2.00			2.30			2.60			3.20			4.00		
1.05	1.95	42	-	2.25	37	-	2.55	34	-	3.15	30	-	3.95	27	-
1.10	1.90			2.20			2.50			3.10			3.90		
1.15	1.85	44	-	2.15	38	-	2.45	35	-	3.05	30	-	3.85	27	-
1.20	1.80			2.10			2.40			3.00			3.80		
1.25	1.75	47	-	2.05	40	-	2.35	36	-	2.95	31	-	3.75	27	-
1.30	1.70			2.00			2.30			2.90			3.70		
1.35	1.65	50	-	1.95	42	-	2.25	37	-	2.85	31	-	3.65	28	-
1.40	1.60			1.90			2.20			2.80			3.60		
1.45	1.55	54	-	1.85	44	-	2.15	38	-	2.75	32	-	3.55	28	-
1.50	1.50			1.80			2.10			2.70			3.50		
1.55	1.45	58	-	1.75	47	-	2.05	40	-	2.65	33	-	3.45	28	-
1.60	1.40			1.70			2.00			2.60			3.40		
1.65	1.35	63	-	1.65	50	-	1.95	42	-	2.55	34	-	3.35	29	-
1.70	1.30			1.60			1.90			2.50			3.30		
1.75	1.25	75	-	1.55	54	-	1.85	44	-	2.45	35	-	3.25	29	-
1.80	1.20			1.50			1.80			2.40			3.20		

*1): Vgs is a Gate –Source voltage of the driver transistor that is defined as the value of VBIAS - VOUT (T).
A value of the dropout voltage is determined by the value of the Vgs.

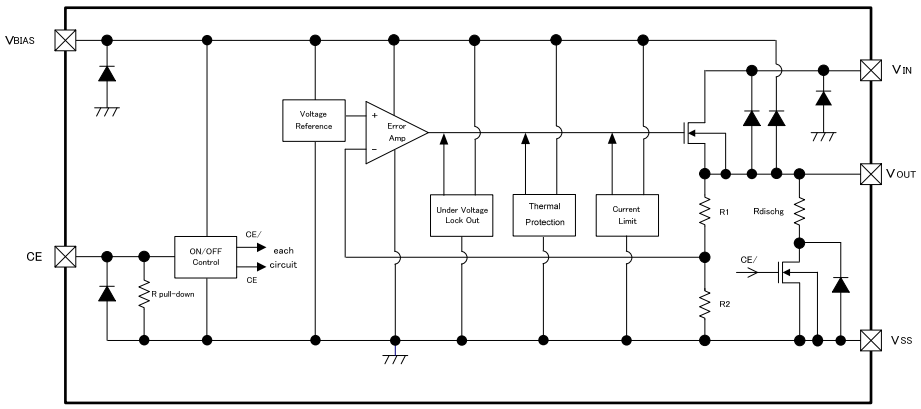
■OPERATIONAL EXPLANATION

<Voltage Regulator>

The voltage divided by resistors R1 & R2 is compared with the internal reference voltage by the error amplifier. The P-channel MOSFET which is connected to the VOUT pin is then driven by the subsequent output signal. The output voltage at the VOUT pin is controlled & stabilized by a system of negative feedback.

V_{BIAS} pin is power supply pin for output voltage control circuit, protection circuit and CE circuit. When output current increase, the V_{BIAS} pin supplies output current also. VIN pin is connected to a driver transistor and provides output current.

In order to obtain high efficient output current through low on-resistance, please take enough Vgs (=V_{BIAS} – V_{OUT}) of the driver transistor. Output current triggers operation of constant current limiter and foldback circuit, heat generation triggers operation of thermal shutdown circuit, the driver transistor circuit is forced OFF when V_{BIAS} or V_{IN} voltage goes lower than U.V.L.O. voltage. Further, the IC's internal circuitry can be shutdown via the CE pin's signal.



XC6601A series

<Low ESR Capacitor>

With the XC6601 series, a stable output voltage is achievable even if used with low ESR capacitors, as a phase compensation circuit is built-in. The output capacitor (C_L) should be connected as close to V_{OUT} pin and V_{SS} pin to obtain stable phase compensation. Values required for the phase compensation are as the table below.

For a stable power input, please connect an bias capacitor (C_{BIAS}) of 1.0μF between the V_{BIAS} pin and the VSS pin. Also, please connect an input capacitor (C_{IN}) of 1.0μF between the VIN pin and the VSS pin. In order to ensure the stable phase compensation while avoiding run-out of values, please use the capacitor (C_{BIAS}, C_{IN}, C_L) which does not depend on bias or temperature too much. The table below shows recommended values of C_{BIAS}, C_{IN}, C_L.

SETTING VOLTAGE	BIAS CAPACITOR	INPUT CAPACITOR	OUTPUT CAPACITOR
	C_{BIAS}	C_{IN}	C_L
0.7V～1.8V	C_{BIAS}=1.0μF	C_{IN}=1.0μF	C_L=4.7μF

Recommended Values of C_{BIAS}, C_{IN}, C_L

■OPERATIONAL EXPLANATION (Continued)

<C_L High Speed Auto-Discharge>

XC6601 series can quickly discharge the electric charge at the output capacitor (C_L) when a low signal to the EN pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the V_{OUT} pin and the V_{SS} pin. When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it could avoids malfunction. At that time, CL discharge resistance is depended on a bias voltage. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R] and an output capacitor value (C_L) as τ (τ=C x R), the output voltage after discharge via the N channel transistor is calculated by the following formulas.

$V = V_{OUT} \times e^{-t/\tau}$, *or* $t = \tau \ln (V_{OUT(E)} / V)$

V : Output voltage after discharge, $V_{OUT(E)}$: Output voltage, t: Discharge time,

τ : C_L auto-discharge resistance R×Output capacitor (C_L) value C

<Current Limit, Short-Circuit Protection>

The XC6601 series' foldback circuit operates as an output current limiter and a short protection of the output pin. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. When the output pin is shorted to the V_{SS} level, current flows about 50mA.

<Thermal Shutdown Circuit (TSD) >

When the junction temperature of the built-in driver transistor reaches the temperature limit level (150℃ TYP.), the thermal shutdown circuit operates and the driver transistor will be set to OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature (125℃ TYP.).

<Under Voltage Lock Out (U.V.L.O.) >

When the V_{BIAS} pin voltage drops below 2.0V (TYP.) or V_{IN} pin voltage drops below 0.4V (TYP.), the output driver transistor is forced OFF by U.V.L.O. function to prevent false output caused by unstable operation of the internal circuitry. When the V_{BIAS} pin voltage rise at 2.2V (TYP.) or the V_{IN} pin voltage rises at 0.4V (TYP.), the U.V.L.O. function is released. The driver transistor is turned on in the state and start to operate voltage regulation.

<CE Pin>

The IC internal circuitry can be shutdown via the signal from the CE pin with the XC6601 series. In shutdown mode, output at the V_{OUT} pin will be pulled down to the V_{SS} level via R1 & R2. However, as for the XC6601 series, the CL auto-discharge resistor is connected in parallel to R1 and R2 while the power supply is applied to the V_{IN} pin. Therefore, time until the V_{OUT} pin reaches the V_{SS} level becomes short.

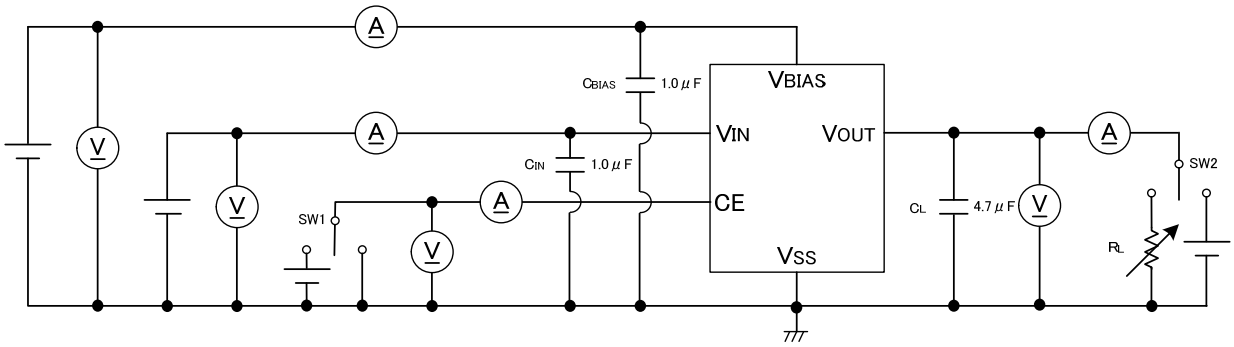
The CE pin of XC6601A has pull-down circuitry so that CE input current increase during IC operation. The CE pin of XC6601B does not have pull-down circuitry so that logic is not fixed when the CE pin is open. If the CE pin voltage is taken from V_{BIAS} pin or V_{SS} pin then logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry when medium voltage is input.

■NOTE ON USE

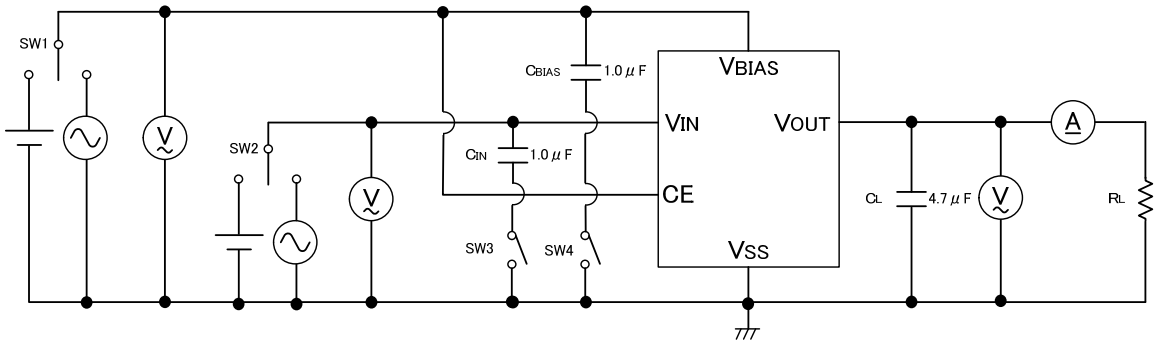
1. Please use this IC within the stated absolute maximum ratings. The IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{BIAS} and V_{SS} wiring or V_{IN} and V_{SS} wiring in particular.
3. Please wire the bias capacitor (C_{BIAS}), input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.
4. Capacitance values of these capacitors (C_{BIAS}, C_{IN}, C_L) are decreased by the influences of bias voltage and ambient temperature. Care shall be taken for capacitor selection to ensure stability of phase compensation from the point of ESR influence.

■TEST CIRCUITS

Circuit ①

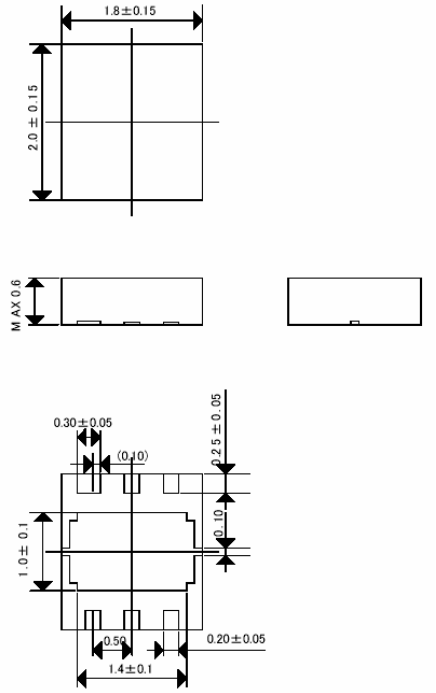


Circuit ②

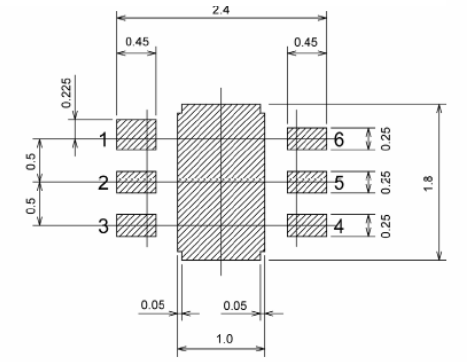


■PACKAGING INFORMATION

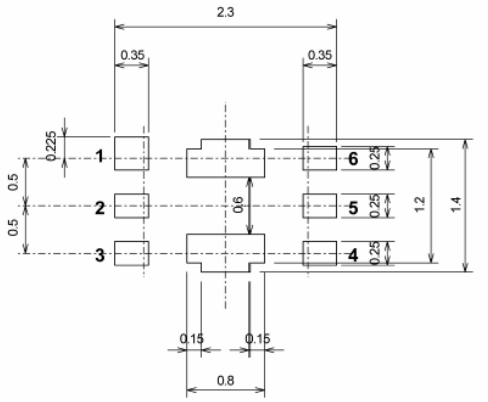
●USP-6C



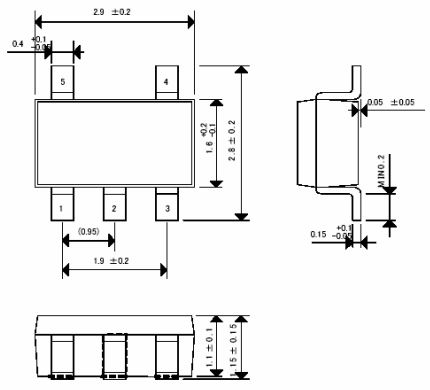
USP-6C Recommended Pattern Layout



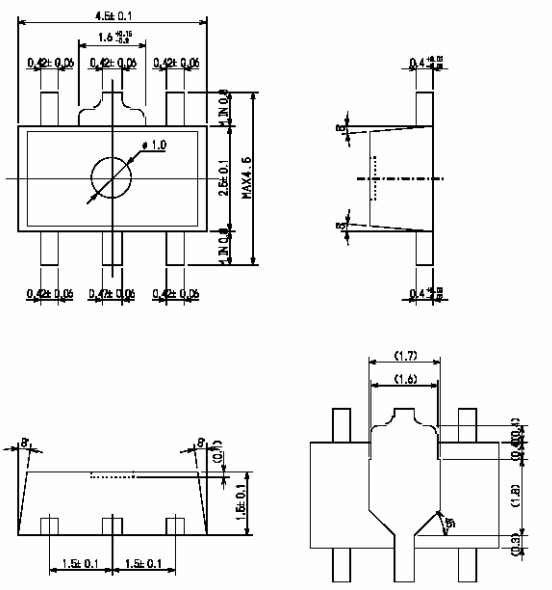
USP-6C Recommended Metal Mask Design



●SOT-25



●SOT-89-5



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