64K X46402

Dual Voltage CPU Supervisor with 64K Password Protected EEPROM

FEATURES

- **Dual Voltage Detection and Reset Assertion**
  - **—Low Vcc Monitor**
  - **—Low V2MON Monitor**
  - **—Low Vcc Block of EEPROM Writes**
  - **—$\overline{\text{RESET}}$ Signal Valid down to Vcc=1V**
- **Selectable Watchdog Timer**
  - **—150ms, 450ms, 1s, 5s, 10s, 20s, 1min, OFF**
- **Volatile Flag shows Watchdog/Low Voltage Reset**
- **64kbit 2-wire Serial EEPROM**
  - **—1MHz Serial Interface speed**
  - **—64-Byte Page Write Mode**
- **Two 64-Byte OTP memory blocks**
  - **—Requires 64-bit OTP password to write**
- **Adjustable size Password Protected Array**
  - **—64 Bit Read and Write Array Passwords**
  - **—Non-password protected array area**
- **8 count tamper counter for invalid passwords**
- **Operates at 2.5-3.7V**
- **8L TSSOP package**

DESCRIPTION

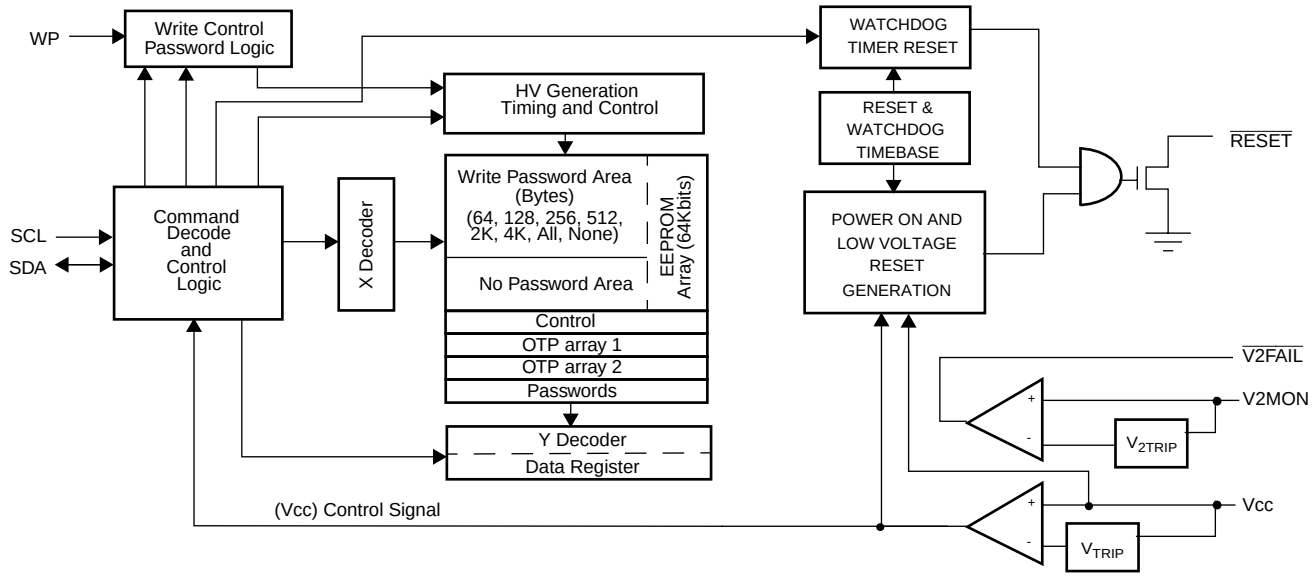
The X46402 combines several functions into one device. The first is a dual voltage CPU supervisor plus 64Kbit serial EEPROM memory with password protected write and read operations. The size of the password protected area is selectable by 3 control bits. A Write Protect (WP) pin in conjunction with a WPEN bit provides hardware OTP control of the configuration of the array. Password protected areas require 64 bit read or write passwords prior to access. The eighth illegal password entry (regardless of the number of correct entries) sets an OTP tamper bit. This bit is one of the 32 bits in the Device ID.

A secondary voltage monitor circuit activates a $\overline{\text{V2FAIL}}$ pin when the secondary supply voltage drops below a V2trip voltage. This circuit is primarily intended to detect the immediate loss of the battery supply.

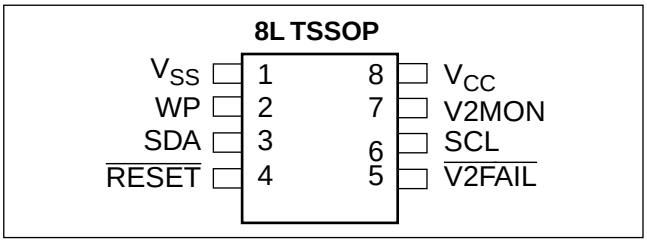
A low Vcc voltage detect circuit activates a $\overline{\text{RESET}}$ pin when Vcc drops below a V_{TRIP} voltage. This signal also blocks read or write operations.

A watchdog timer with the time period controlled by three bits provides several possible time out periods from 150ms to 1 minute.

Functional Diagram



PACKAGE/PINOUTS



PIN NAMES

VSS	Ground
SDA	Serial Data
VCC	Power
SCL	Serial Clock
WP	Write Protect
V2MON	Voltage monitor input
$\overline{\text{RESET}}$	Low Voltage Detect Output
$\overline{\text{V2FAIL}}$	V2 Voltage Fail Output

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with other open drain or open collector outputs. An open drain requires the use of a pull-up resistor.

Write Protect (WP)

The WP pin works in conjunction with a nonvolatile WPEN bit to “lock” the setting of the Watchdog Timer control and the memory write protect bits.

Reset Output ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ is an active LOW, open drain output which goes active whenever Vcc falls below the minimum Vtrip sense level. It will remain active until Vcc rises above the minimum Vtrip sense level for 150ms. $\overline{\text{RESET}}$ goes active if the Watchdog Timer is enabled and there is no start bit before the end of the selectable Watchdog time-out period. A serial start bit will reset the Watchdog Timer. $\overline{\text{RESET}}$ also goes active on power up at 1V and remains active for 150ms after the power supply stabilizes.

V2 Voltage Fail Output ($\overline{\text{V2FAIL}}$)

$\overline{\text{V2FAIL}}$ is an active LOW, open drain output which goes active whenever V2MON falls below the minimum V2trip sense level. It will remain active until V2MON rises above the minimum V2MON sense level.

DEVICE OPERATION

Power On Reset

Application of power to the X46402 activates a Power On Reset Circuit. This circuit goes active at 1V and pulls the $\overline{\text{RESET}}$ pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When Vcc exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{\text{RESET}}$ allowing the processor to begin executing code.

Low Voltage Monitoring

During operation, the X46402 monitors the V_{CC} and V2MON levels and compares these with internal, preset voltages.

When the internal low voltage detect circuitry senses that V2MON is low, the $\overline{\text{V2FAIL}}$ pin goes active. Typically this would be used by the processor as an interrupt to stop the execution of the code or to do housekeeping in preparation for an impending power failure.

When the internal low voltage detect circuitry senses that Vcc is low, the following happens:

—The $\overline{\text{RESET}}$ pin goes active.

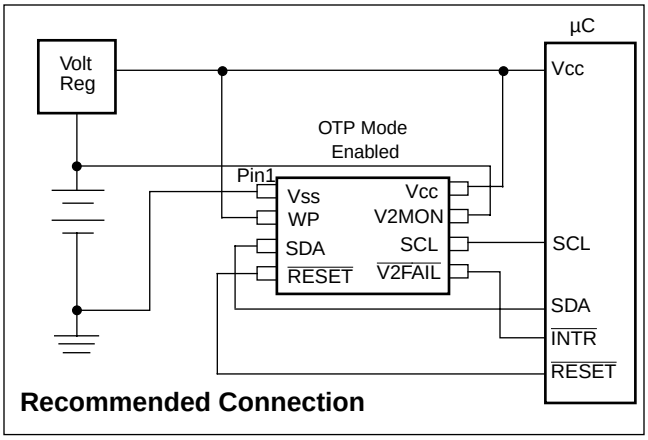
—The Flag bit in the control register is set to zero.

—Communication to the device is interrupted and any command is aborted. If a serial nonvolatile store is in progress when power fails, the circuitry does not stop the nonvolatile store operation, but attempts to complete the operation.

The $\overline{\text{RESET}}$ and $\overline{\text{V2FAIL}}$ signals remain active until Vcc voltage drops below 1V. $\overline{\text{RESET}}$ remains active until Vcc returns and exceeds V_{TRIP} for 200ms. $\overline{\text{V2FAIL}}$ remains active until immediately after V2MON returns and exceeds it’s minimum voltage.

Watchdog Timer

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the Start bit. The microprocessor must send a start bit periodically to prevent a $\overline{\text{RESET}}$ signal. The start bit must occur prior to the expiration of the watchdog time-out period. The state of three nonvolatile control bits in the Control Register determines the watchdog timer period. The microprocessor can change these watchdog bits, or they may be “locked” by tying the WP pin HIGH and setting the WPEN bit HIGH.



Recommended Connection

ARCHITECTURE

Data Memory

This 64kbit memory array can be partitioned into password protected or non-password protected areas. When password protected, the contents are readable after sending a “Memory Read” password. The contents of a password protected portion of the memory array are writeable with a “Memory Write” Password. This array is re-writable up to the limit of the EEPROM endurance.

OTP

The second section of memory consists of two 64-byte arrays, each writable only once. These arrays are always password protected. Reading from either of these arrays requires the use of an “OTP Read” password. Both arrays can be read with a single operation. Writing either array requires an “OTP Write” Password. Writing more than 64 bytes to each array results in the data “wrapping” around and over-writing previous values.

Array	Address
OTP Array 1	0000h - 003Fh
OTP Array 2	0040h - 007Fh

Control Register

A password protected read or write array command at address FFFFh reads or writes the Control Register. Since the control register contains information relating to the password protection, it is necessary to use the Array passwords to access the control register.

The Control Register contains bits that control the watchdog timer and the hardware write protect features and is formatted as follows:

7	6	5	4	3	2	1	0
WPEN	FLB	WD2	WD1	WD0	BL2	BL1	BL0

Write Protect Enable bit (WPEN)

The WP pin, in conjuction with a WPEN bit programmed HIGH, provides Hardware Write Protection. This prevents changes to the control register contents even with a valid password. When either the WP pin or WPEN bit is LOW, a 64 bit Array write array password is required to change the contents of the control register. When both the WP pin and the WPEN bit are HIGH, the Control Register cannot be written.

Flag Bit

The flag bit is a volatile bit. It can be used to determine if a reset condition was due to a power failure or watchdog reset condition. If power fails (i.e. the internal low voltage detect signal goes active), the bit is set to ’0’. This bit is also set or reset by a Control Register write operation. A watchdog reset does not change the state of the flag bit.

Watchdog Timer Control

The Watchdog time-out period is controlled by the bits WD2, WD1, and WD0. See the following Table.

Table 1. Watchdog Time Control Bits

Control Register Bits			Watchdog Time-out (Typical)
WD2	WD1	WD0	
0	0	0	1 Second
0	0	1	450 Milliseconds
0	1	0	150 Milliseconds
0	1	1	Disabled
1	0	0	1 minute
1	0	1	20 seconds
1	1	0	10 seconds
1	1	1	5 seconds

Password Protection Configuration

Portions of the memory array may be “locked”. This area of memory is password protected and is defined by the bits BL2, BL1 and BL0. For these protected areas it is necessary to use a Read password to output data and an “Array Write” Password to write data. This block lock area is re-writable, by issuing the correct password.

Table 2. Password Protected Block Size Select

BL2 BL1 BL0	Password Protected Addresses (Use Password Command)	Non-Password Protected Addresses (Use Password or No-Password Commands)
000	None	0000h - 1FFFh
001	0000h - 003Fh	0040h - 1FFFh
010	0000h - 007Fh	0080h - 1FFFh
011	0000h - 00FFh	0100h - 1FFFh
100	0000h - 01FFh	0200h - 1FFFh
101	0000h - 07FFh	0800h - 1FFFh
110	0000h - 0FFFh	1000h - 1FFFh
111	0000h - 1FFFh	None

SERIAL MEMORY OPERATION

There are four primary modes of operation for the X46402; Protected READ and WRITE of the memory and OTP arrays and unprotected Read and Write of non-password protected areas of the memory array. Protected operations must be performed with one of four 8-byte passwords.

The basic method of communication for the password protected areas of the device is established by generating a start condition, then transmitting a command, followed by the correct password. All parts will be shipped from the factory with all passwords equal to ‘0’. The user must perform ACK Polling to determine the validity of the password, before starting a data transfer (see Acknowledge Polling.) Only after the correct password is accepted and a ACK polling has been performed, can the data transfer occur.

Non-password protected areas of the memory array are accessed in the same manner as access to password protected areas, except the password and the password acknowledge polling sequences are not required.

Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

If the X46402 is in a nonvolatile write cycle a “no ACK” (SDA=HIGH) response will be issued in response to loading of the command byte. If a stop is issued prior to the start of a nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

The basic sequence is illustrated in Figure 1.

After each transaction is completed, the X46402 will reset and enter into a standby mode. This will also be the response if an unsuccessful attempt is made to access a protected array.

Password Protection

The X46402 requires a 64 bit write password to change the contents of the control register or to write to a block protected memory area. The X46402 also requires a 64 bit read password to output the contents of the block protected array or the control register. The block protection is controlled by the [BL2:BL0] bits and allows the options described in Table 2. If an area is block protected, it needs a password prior to each read or write to the area. The passwords cannot be read, even after the device receives the correct password.

Figure 1. X46402 Device Operation (Password Protected Areas)

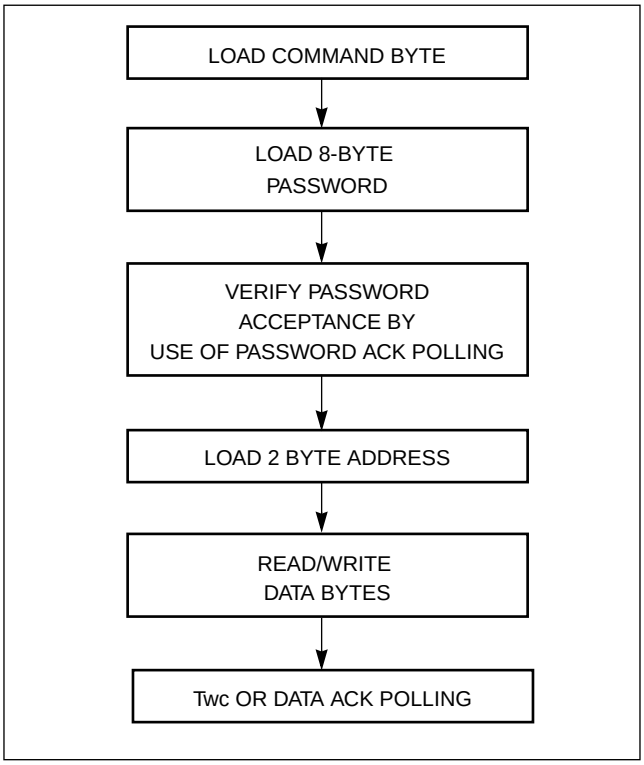


Figure 2. Set V_{TRIP} Level Sequence ($V_{CC} \geq V_{TRIP}$)

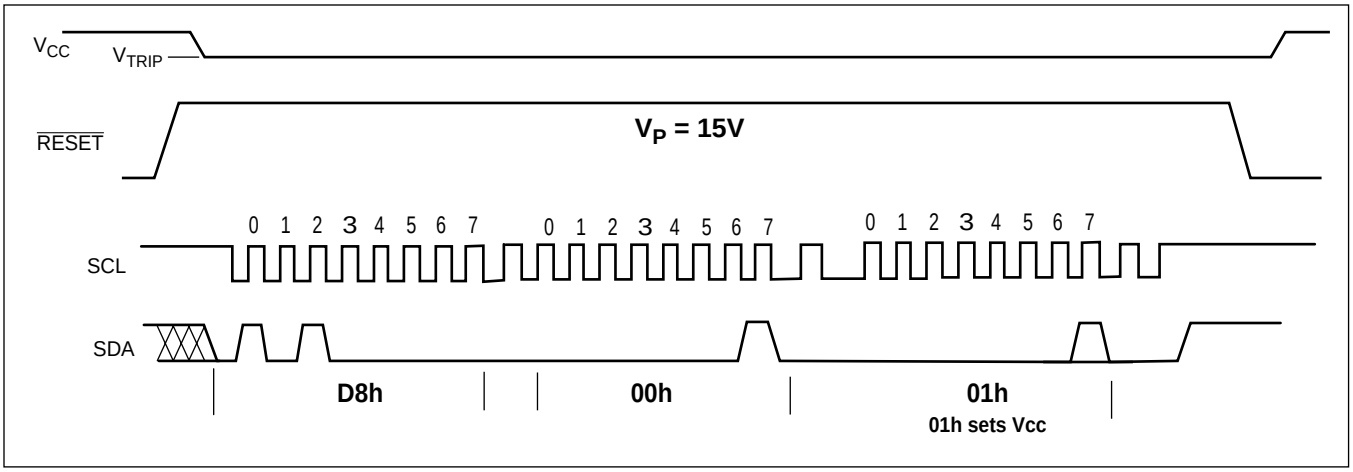


Figure 3. Set $V2_{TRIP}$ Level Sequence ($V_{CC} \geq V2_{TRIP}$)

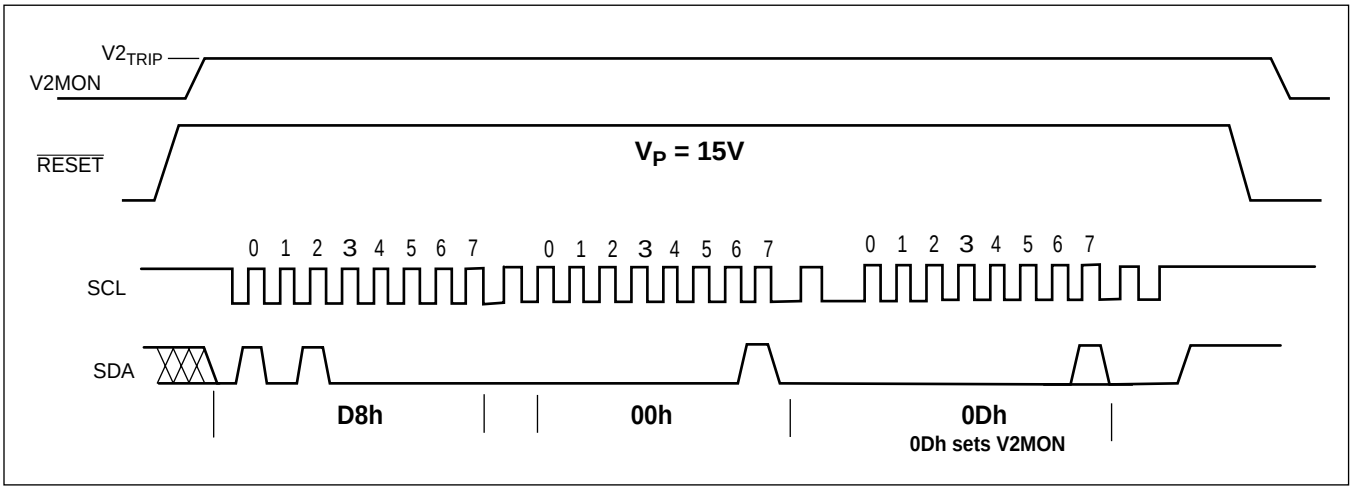


Figure 4. Reset V_{TRIP} Level Sequence (Vcc > 3V, WEL is set.)

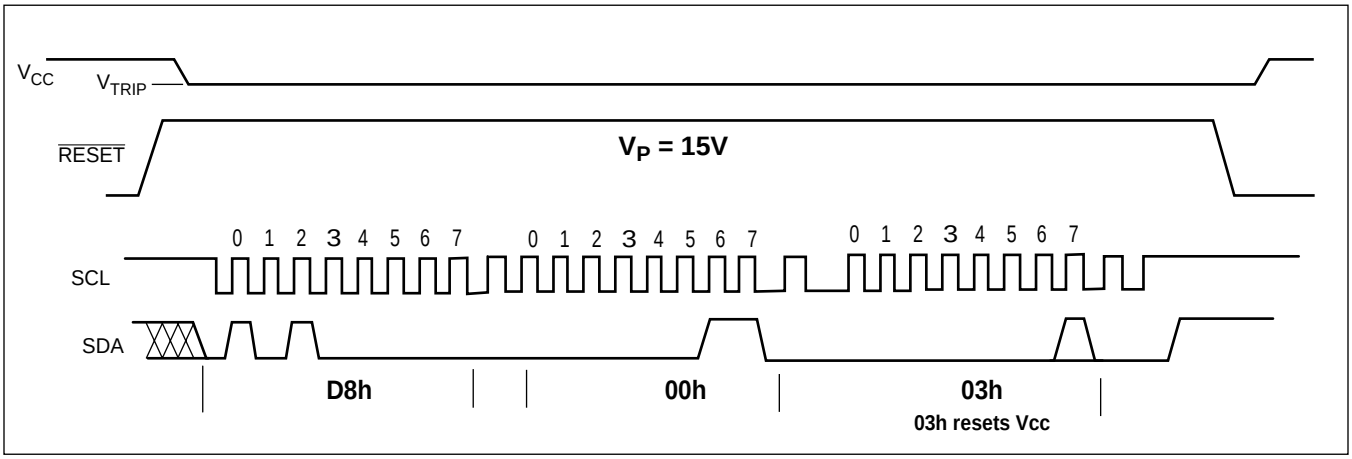
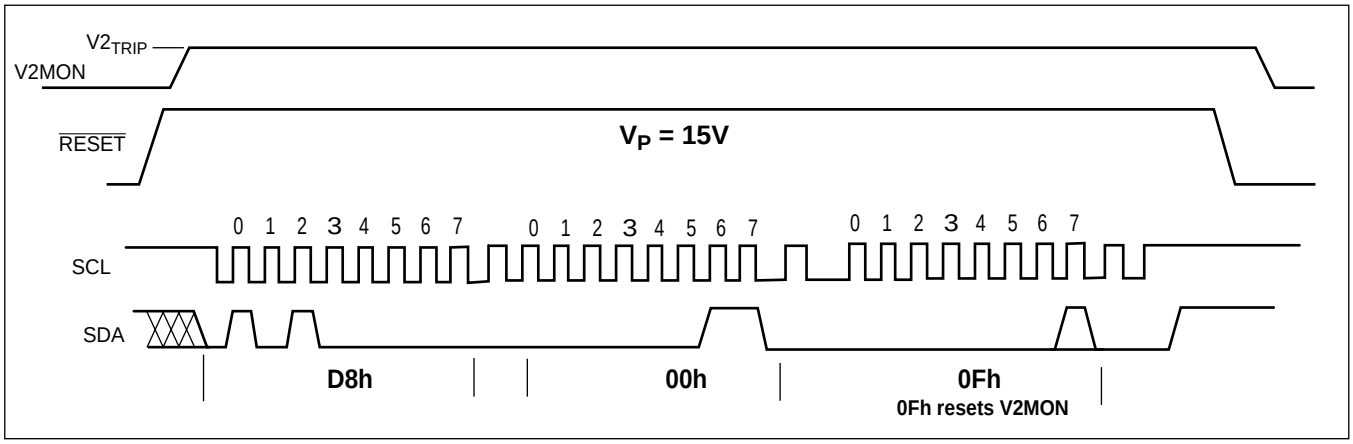


Figure 5. Reset $V2_{TRIP}$ Level Sequence (Vcc > 3V, WEL is set.)



V_{CC} AND V2MON THRESHOLD RESET PROCEDURE

The X46402 is shipped with standard V_{TRIP}, and $V2_{TRIP}$ voltages. These values will not change over normal operating and storage conditions. However, in applications where the standard thresholds are not exactly right, or if higher precision is needed in the threshold value, the X46402 trip points may be adjusted. The procedure is described below, and uses the application of a high voltage control signal.

Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP},$V2_{TRIP}$ to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

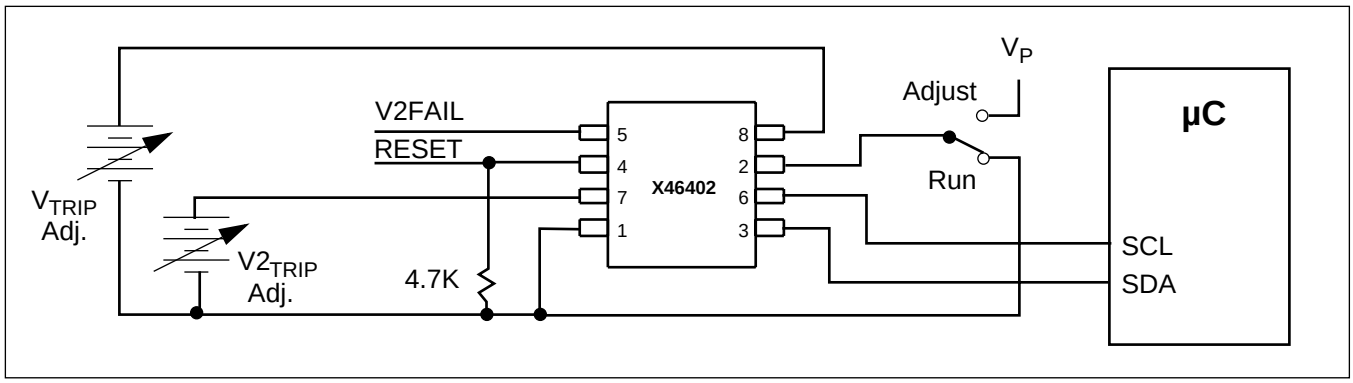
To set the new voltages, apply the desired V_{TRIP} threshold voltage to the Vcc pin, the $V2_{TRIP}$ voltage to the V2MON pin, then tie the $\overline{RESET}$ pin to the programming voltage V_P Then, write data 01h or 0Dh address 00h to program V_{TRIP}, $V2_{TRIP}$ respectively. The stop bit following a valid write operation initiates the programming sequence. Bring $\overline{RESET}$ LOW to complete the operation. Note: this operation also writes 01h, or 0Dh to address 00h.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP}, the $V2_{TRIP}$ to a "native" voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When the threshold is reset, the new level is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP}, $V2_{TRIP}$ voltage, apply the desired V_{TRIP} or $V2_{TRIP}$ threshold voltage to the Vcc or V2MON pin, respectively, and tie the $\overline{RESET}$ pin to the programming voltage V_P Then write 03h or 0Fh to address 00h. The stop bit of a valid write operation initiates the programming sequence. Bring $\overline{RESET}$ LOW to complete the operation. Note: this operation also writes 03h or 0Fh to address 00h of the EEPROM array.

Figure 6. Sample V_{TRIP} Reset Circuit



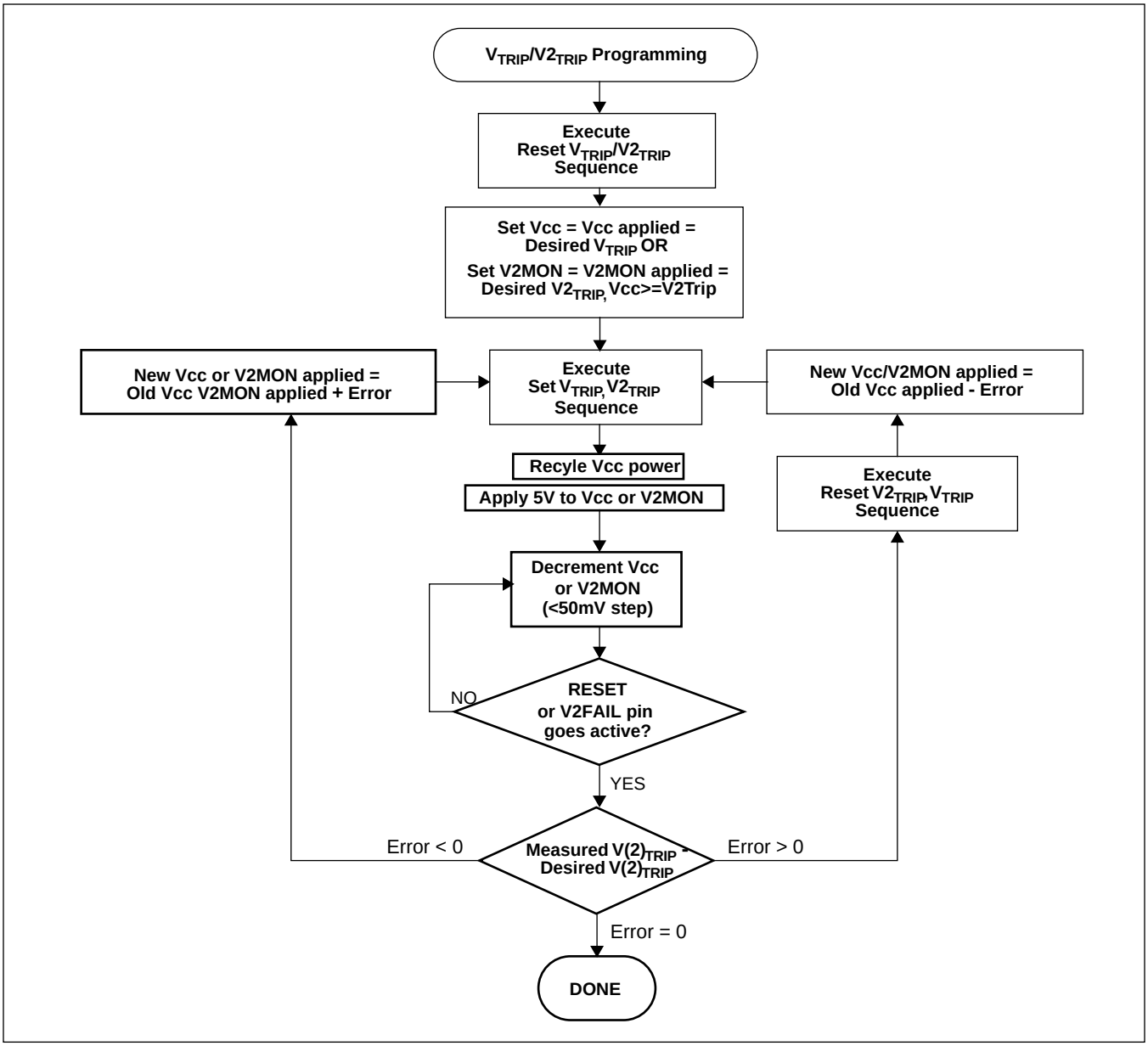
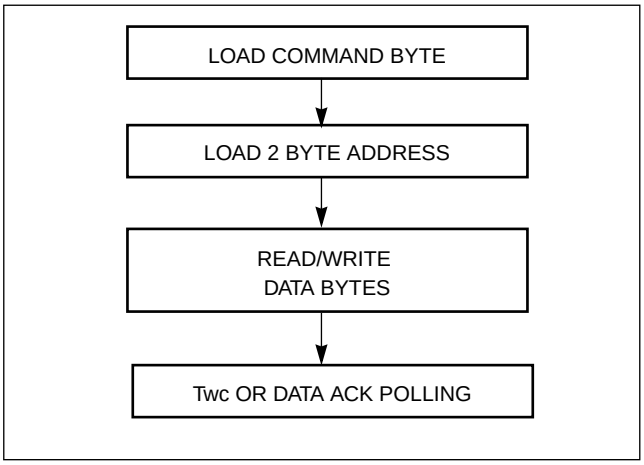


Figure 7. X46402 Device Operation (Non-Password Protected Areas)



Tamper Counter

The X46402 contains a tamper counter. The entry of an invalid password increments the counter. This operation requires an internal nonvolatile cycle, requiring up to 10 ms to complete. To minimize the possibility of of an unauthorized person monitoring the device current to detect the enry of the correct password, an internal high voltage cycle is initiated even when the counter does not increment. As such, each password entry requires up to 10ms to acknowledge, so a long period of time would be required to correctly guess the password.

On the eighth incorrect password entry, a one-time programmable tamper bit is set in the Device ID area. The Tamper Counter increments with each incorrect password attempt and cannot be reset, except by the Reset Device Command. When the tamper counter overflows, the device is “locked”. In the locked condition, none of the password commands respond except Reset Device. No-password commands are always available. The locked condition is determined by reading the device ID and reading bit 32. The device is reset by the Master Reset or Reset Device commands.

Device Protocol

The X46402 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as a receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X46402 will be considered a slave in all applications.

After each byte written to or read from the X46402, the address pointer is incremented by 1. This allows the user to read from the entire device after sending only a single address. It also allows an entire page to be written in one operation. An exception to this address incrementation occurs during a read. After reading address 1FFFh the device goes into an idle mode, so additional reads return all “1s”.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figure 8 and Figure 9.

Start Condition

All commands are preceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X46402 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

A start may be issued to terminate the input of a control byte or the input data to be written. This will reset the device and leave it ready to begin a new read or write command. A start bit generated while the part is outputting data is accepted as a start as long as the device is not outputting a ’zero’.

Stop Condition

All communications are be terminated by a stop condition. The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to reset the device during a command or data input sequence and will leave the device in the standby power mode. As with starts, stops are recognized while the device outputs data, as long as the data output is not a ‘zero’.

Figure 8. Data Validity

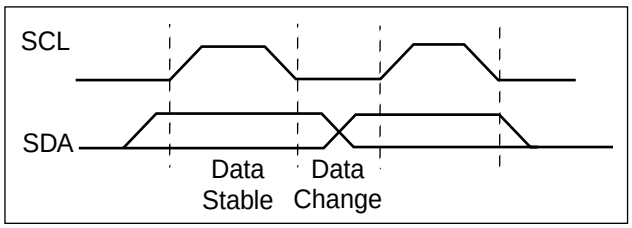
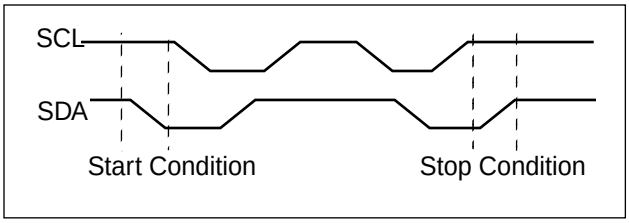


Figure 9. Definition of Start and Stop Conditions Acknowledge



Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

The X46402 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write condition have been selected, the X46402 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

Read Device ID Command

A special, non-password protected command reads the device ID. The device ID is a 32 bit identification code that can be generic or tailored to the needs of an individual company. The last of the 32 bits indicates whether the device has been tampered with by an unauthorized user attempting to enter invalid passwords.

Reset Device Command

The Reset Device command resets the tamper bit, clears the tamper counter and removes the tamper “lock” (allowing the device to accept commands). However, the Reset Device command does not clear any memory array area.

Table 3. X46402 Instruction Set

1st Byte after Start	1st Byte after Password	2nd Byte after Password	Command Description	Password used
1000 0000	High Address	Low address	Password Memory Array Read	Memory Read
1000 1000	High Address	Low address	OTP Read	OTP Read
1001 0000	High Address	Low address	Password Memory Array Write	Memory Write
1001 1000	High Address	Low address	OTP Write	OTP Write
1010 0000	0000 0000	0000 0000	Change Memory Read Password	Memory Read
1010 1000	0000 0000	0000 0000	Change OTP Read Password	OTP Read
1011 0000	0000 0000	0000 0000	Change Memory Write Password	Memory Write
1011 1000	0000 0000	0000 0000	Change OTP Write Password	OTP Write
1100 0000	0000 0000	0000 0000	Change Reset Password	Reset
1100 1000	High Address	Low address	No-Password Memory Array Read	None
1101 1000	High Address	Low address	No-Password Memory Array Write	None
1110 1000	not used	not used	Reset Device Command (Resets Tamper bit)	Reset
1111 0000	not used	not used	ACK Polling command (Ends Password operation)	None
All the rest			Reserved	

Notes: Illegal command codes will be disregarded. The part will respond with a “no-ACK” to the illegal byte and then return to the standby mode.

PROGRAM OPERATIONS

Password Protected Array Programming

The password protected memory array write or OTP write requires issuing an 8-bit Password Write command followed by the password, password ACK command, the address and then the data bytes transferred as illustrated in Figure 10. Up to 64 bytes (or more) may be transferred. Sending more than 64 bytes results in data wrapping and over-writing previous data. After the last byte to be transferred is acknowledged, a stop condition is issued which starts the nonvolatile write cycle.

Non-Password Protected Array Programming

The non-password protected memory array program mode requires issuing the 8-bit No-Password Write command followed by the address and then the data bytes transferred as illustrated in Figure 11. Up to 64 bytes (or more) may be transferred. Sending more than 64 bytes results in data wrapping and over-writing previous data. After the last byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle.

Figure 10. Password Protected Array Programming (Memory and OTP arrays)

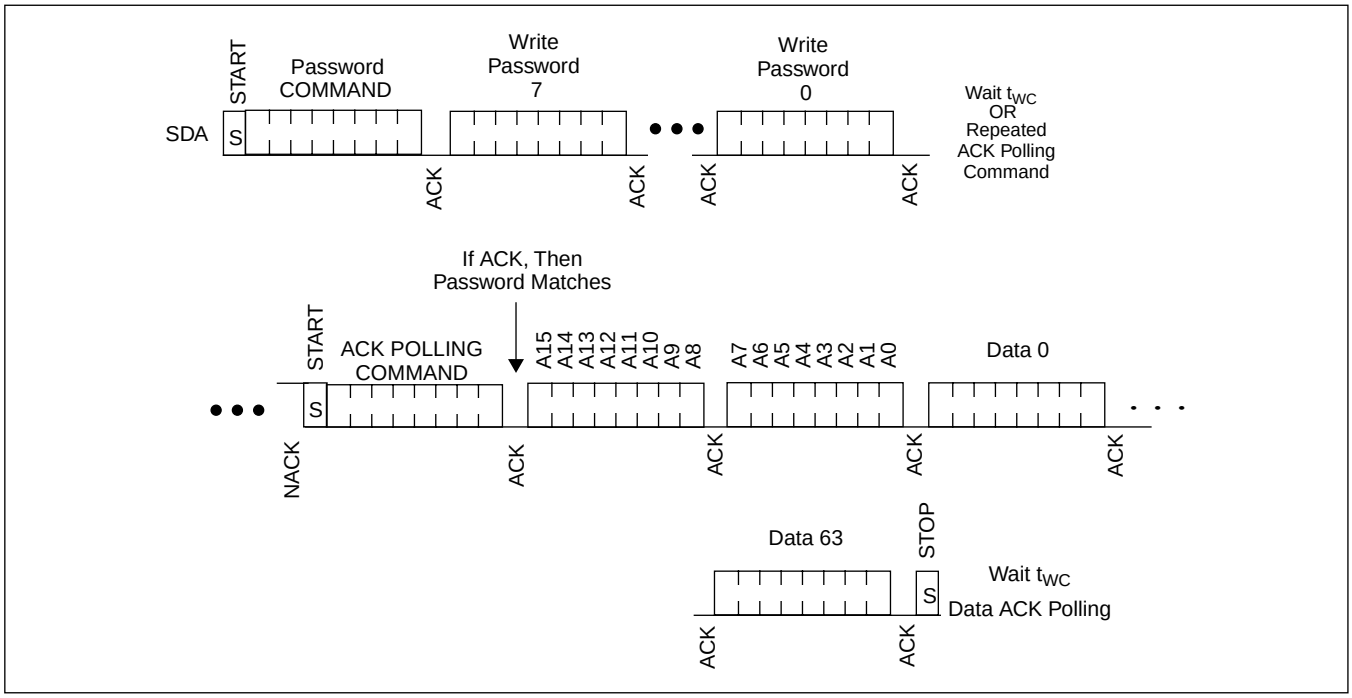
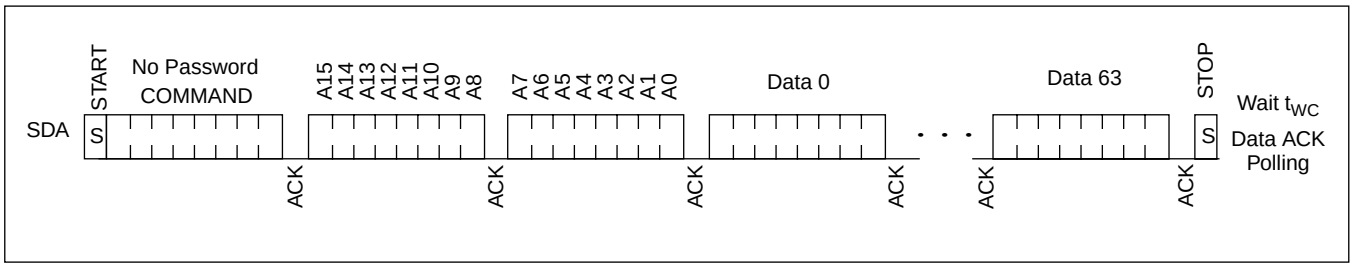


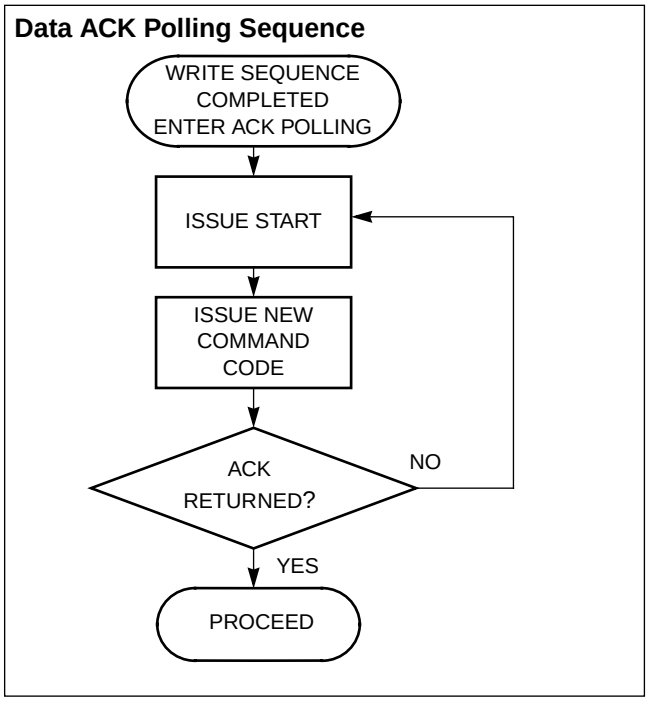
Figure 11. Non-Password Protected Array Programming (Memory array only)



ACK Polling

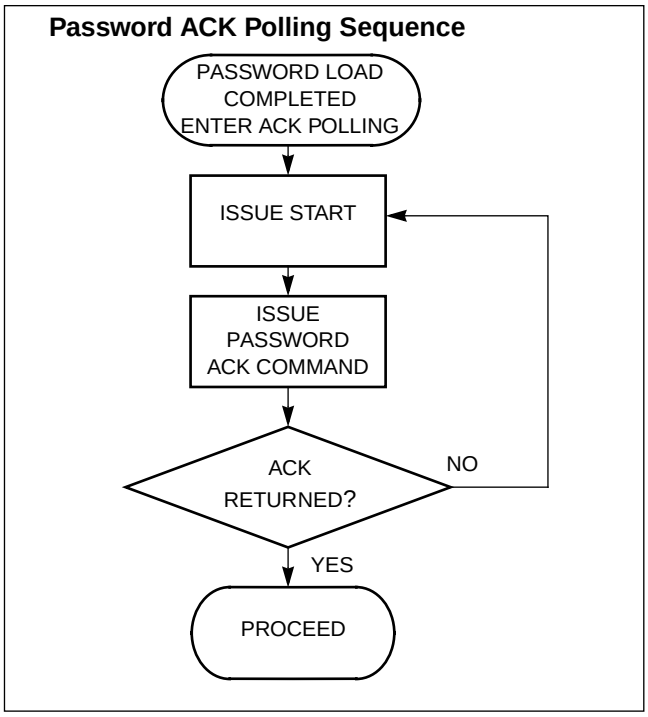
Once a stop condition is issued to indicate the end of the host's write sequence, the X46402 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can begin immediately. This involves issuing the start condition followed by the new command code of 8 bits (1st byte of the protocol.) If the X46402 is still busy with the nonvolatile write operation, it will issue a "no-ACK" in response. If the nonvolatile write operation has completed, an "ACK" will be returned and the host can then proceed with the rest of the protocol. See Figure 12.

Data ACK Polling Sequence



After the password sequence, there is always a nonvolatile write cycle. This is done to discourage random guesses of the password if the device is being tampered with. In order to continue the transaction, the X46402 requires the master to perform an ACK polling with the specific code of F0h. As with regular Acknowledge polling the user can either time out for 10ms, and then issue the ACK polling once, or continuously loop as described in the flow.

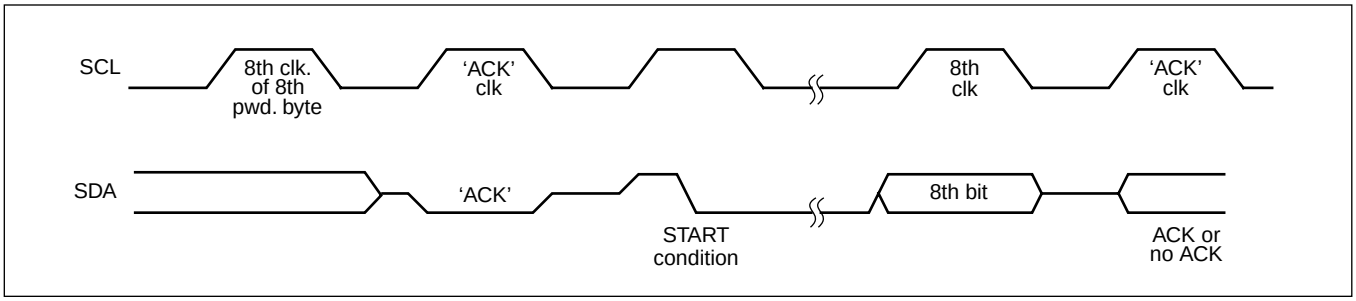
Password ACK Polling Sequence



If the password that was inserted was correct, then an "ACK" will be returned once the nonvolatile cycle is over, in response to the ACK polling cycle immediately following it.

If the password that was inserted was incorrect, then a "no ACK" will be returned even if the nonvolatile cycle is over. Therefore, the user cannot be certain that the password is incorrect until the 10ms write cycle time has elapsed.

Figure 12. Acknowledge Polling



PASSWORD PROTECTED READ OPERATIONS

Password protected read operations are initiated in the same manner as password protected write operations but with a different command code.

Password Random Read (Data Array, OTP Arrays)

Data from a password protected array can be randomly read after sending a single password. To do this, the master issues a start bit, sends a Password Read instruction and read password, performs Password Ack Polling, then issues the desired 2 byte address. The host receives the first byte from the X46402 and sends a NACK, followed by a repeated start bit. A new 8-bit address specifies the next byte to read. This process can continue indefinitely as long as the each byte read out of the X46402 is "NACKed" and followed by a repeated start.

The address automatically increments after each read operation. As such, a special case arises. A random read of address 00FFh automatically increments to 0100h after reading the byte. Consider the following example.

Example: A system needs data from password protected locations 0020h and 0150h and the designer does not wish to send the password twice. After receiving data from 0020h, the host sends a NACK and a repeated start, followed by address byte FFh. The data read from location 0FFh is ignored, but the operation has adjusted the address pointer to 100h. Another NACK and repeated start followed by the address 50h allows the contents of 150h to be read by the host.

A random read of either of the OTP arrays can access all locations of both arrays without another password command sequence.

A password random read operation will also return valid data if accessing a non-password protected area of the array. See Figure 13.

Password Sequential Read

The host can read sequentially within an array after the password acceptance sequence. The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory array contents to be serially read during one operation. At the end of the address space (address 1FFFh for the memory array, 7Fh for the OTP array) the device goes into an idle state and data output is all "1s". To continue reading at another address requires a new Read operation. Refer to Figure 14 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, the host sends a stop condition with or without a preceding acknowledge.

After sending a Password Read command and the correct password, the entire array, including non-password protected areas will be read with a sequential read command.

After sending a Password Array Read command and correct password, the entire array, including non-password protected areas are read by a sequential read command.

NON-PASSWORD READ OPERATIONS

Non-password protected read operations are initiated in the same manner as non-password protected write operations but with a different command code.

No-Password Random Read

The master issues the start condition, then a No-password Read instruction, then issues the word address. Once the first byte has been read, another start can be issued followed by a new 8-bit address. A No-Password random read operation is not allowed to a password protected area. In a No-Password Random Read from address 00FFh, the address pointer changes to 100h after outputting the data byte and operates in the same manner as the password protected operation. See Figure 15.

No-Password Sequential Read

The host can read sequentially within the un-protected area of the array after receiving the No-password Command and an address within the unprotected address space. The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire un-protected memory array contents to be serially read during one operation. At the end of the address space (address 1FFFh) the device goes into an idle state and a new read sequence must be initiated to continue reading at another address. Refer to Figure 16 for the address, acknowledge and data transfer sequence. An acknowledge must follow each 8-bit data transfer. After the last bit has been read, the host sends a stop condition with or without a preceding acknowledge.

COMBINED RANDOM/SEQUENTIAL OPERATIONS

A random read and sequential read can be combined, however there are some limitations. Both password protected or non-password operations operate in the same way. After sending a random read command and reading the first byte, continued clocks will return successive addresses. However, after more than one byte of data is returned, it is not possible to initiate a new random read, without issuing a stop and starting a new command. This also allows multiple random read operations and a sequential read operation, as long as the last operation is sequential. Note: A read operation that includes a random read of the last byte in the memory or OTP arrays cannot include a sequential read operation.

Figure 13. Password Protected Random Read

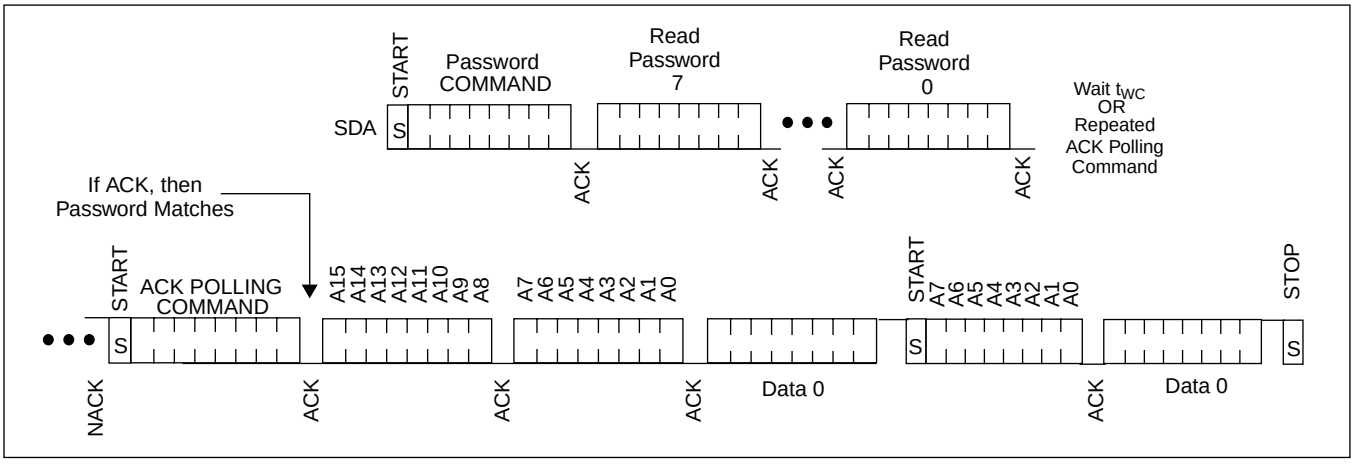


Figure 14. Password Protected Sequential Read

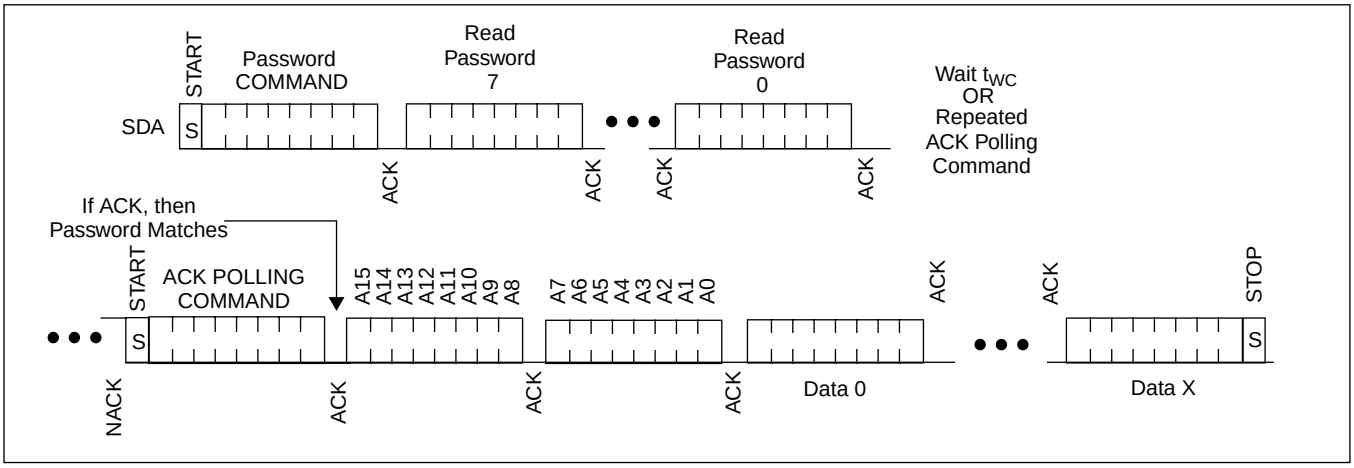


Figure 15. Non-Password Protected Random Read

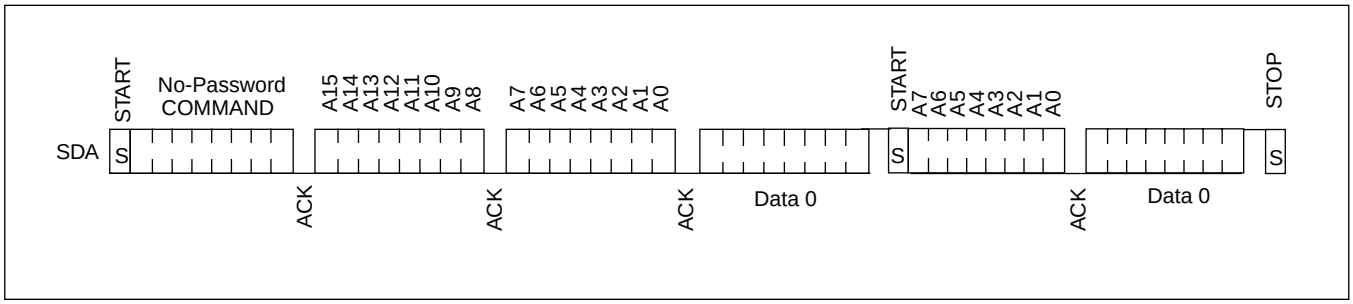


Figure 16. Non-Password Protected Sequential Read

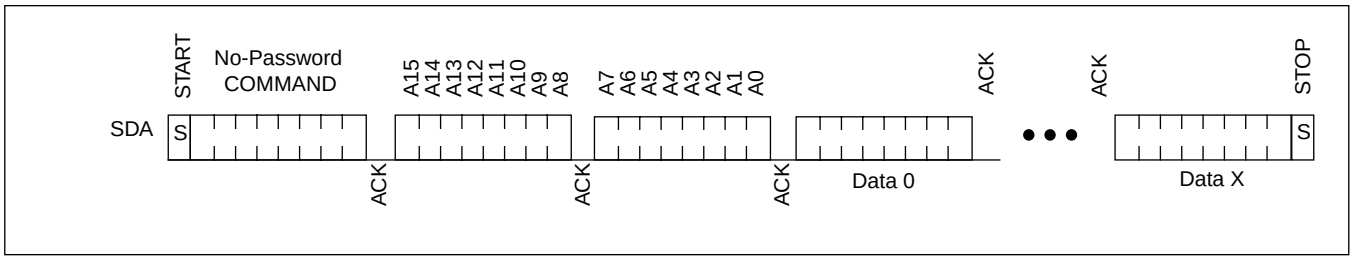
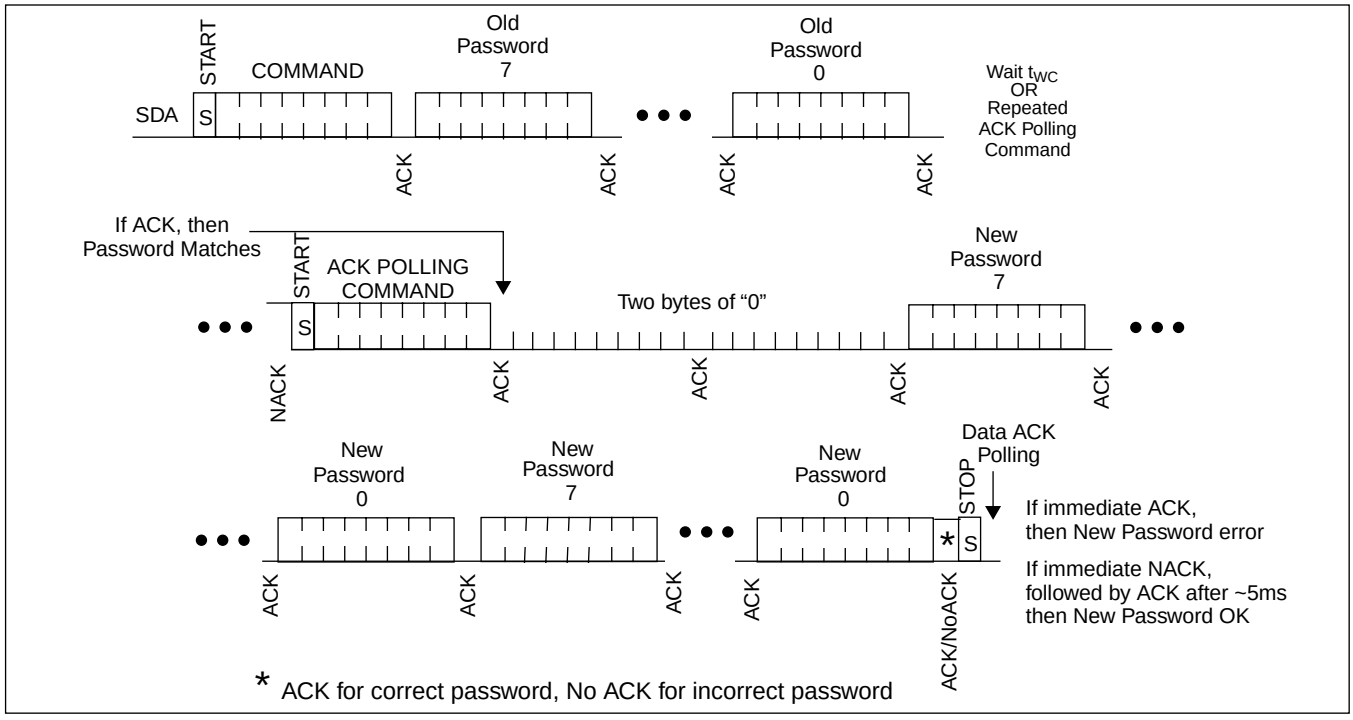
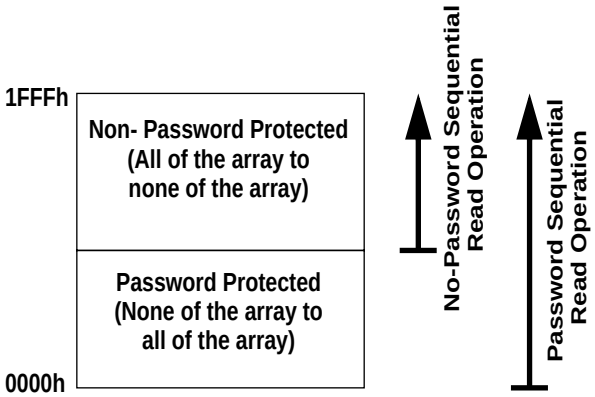


Figure 17. Change Passwords



Note on Read/Write Operations



Notes:

Using a “password read” or a “password write” to a non-password protected area is acceptable, because the password is received and accepted prior to an address transmission. It is assumed that access to non-password protected areas is uncontrolled, so either method should work.

Using a “no-password read” or a “no-password write” on a password protected area would not work. Trying to access a password protected area without the password match causes the device to return a NACK after the address.

A password sequential read that starts in the password protected area can continue into and through the non-password protected area. It will not “wrap” back to address ’0’.

A no-password sequential read can only start in the non-password protected area and cannot “wrap” back into the protected area.

CHANGE PASSWORD COMMAND

When changing a password, the Change Password command is sent to the device. The old password follows. When the old password is accepted (as indicated by the ACK Polling Command sequence), the new password is sent to the device twice, following two bytes of zero. A stop bit initiates the store of the new password. To be successful in the password change operation the first and second transmission of the new password must match and there must be exactly 16 password bytes. If this is not the case, the operation is aborted and the password remains unchanged.

PASSWORDS

The sequence in Figure 17 shows how to change (program) the passwords. The programming of passwords is done twice prior to the nonvolatile write cycle in order to verify that the new password is consistent. After the eight bytes are entered in the second pass, a comparison takes place. A mismatch will cause the part to ignore the change command and enter into the standby mode.

There are two ways to determine whether the operation was completed successfully. The Data ACK polling method can determine if a password has been loaded correctly, however the data ACK command must be issued less than 2ms after the stop bit. After this time, it cannot be determined if the password has been loaded correctly, without trying the new password. To determine if the new password has been loaded correctly the data ACK polling command is issued immediately following the stop bit. If it returns an ACK, then the two passes of the new password entry do not match. If it returns a “no ACK” then the passwords match and a high voltage cycle is in progress. The high voltage cycle is complete when a subsequent data ACK command returns an “ACK”.

An easier way to determine that the password has been changed correctly is to read the ACK bit following the second writing of the new password. If the device returns an ACK, the password is good. A No ACK indicates something went wrong. If there was an error, the password remains unchanged.

There is no way to read any of the passwords.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias . . . . . –65°C to +135°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on any Pin with respect to V_{SS} . . . . . –1V to +7V
D.C. Output Current 5mA
Lead Temperature (Soldering, 10 seconds) . . . . . .300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Extended	–20°C	+85°C

Device	Supply Voltage Limits
X46402	2.5V to 3.7V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

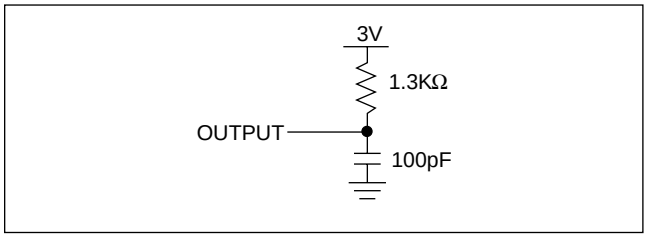
Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	f_{SCL} = 1MHz, $\overline{RESET}$ = $\overline{V2FAIL}$ = V_{CC} w/ pull up resistor V_{2MON} = V_{CC}
I_{CC2}(3)	V_{CC} Supply Current (Write)		3	mA	f_{SCL} = 1MHz, $\overline{RESET}$ = $\overline{V2FAIL}$ = V_{CC} w/ pull up resistor RST = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		50	µA	V_{IL} = V_{CC} x 0.1, V_{IH} = V_{CC} x 0.9 f_{SCL} = 1MHz, f_{SDA} = 400 KHz
I_{SB2}(1)	V_{CC} Supply Current (Standby)		1	µA	V_{SDA} = V_{SCL} = V_{2MON} = V_{CC} Other = GND or V_{CC}–0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL1}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	V_{CC} = 3.0V
V_{IH1}(2)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	V_{CC} = 3.0V
V_{IL2}(2)	Input LOW Voltage	–0.5	V_{CC} x 0.1	V	V_{CC} = 3.0V
V_{IH2}(2)	Input HIGH Voltage	V_{CC} x 0.9	V_{CC} + 0.5	V	V_{CC} = 3.0V
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

Table 4. CAPACITANCE (T_A = +25°C, f = 1MHz, V_{CC} = 3V)

Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (WP, SCL, V_{2MON})	6	pF	V_{IN} = 0V

Notes: (1) Must perform a stop command after a read command prior to measurement
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5
Output Load	100pF

AC CHARACTERISTICS

AC Specifications (Over the recommended operating conditions)

Symbol	Parameter	Min	Typ(1)	Max	Units
f_{SCL}	SCL Clock Frequency	0		1000	KHz
t_{IN}	Pulse width of spikes which must be suppressed by the input filter	10			ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.05		0.55	µs
t_{BUF}	Time the bus must be free before a new transmit can start	0.5			µs
t_{LOW}	Clock LOW Time	0.6			µs
t_{HIGH}	Clock HIGH Time	0.4			µs
$t_{SU:STA}$	Start Condition Setup Time	0.25			µs
$t_{HD:STA}$	Start Condition Hold Time	0.25			µs
$t_{SU:DAT}$	Data In Setup Time	100			ns
$t_{HD:DAT}$	Data In Hold Time	0			µs
$t_{SU:STO}$	Stop Condition Setup Time	0.25			µs
t_{DH}	Data Output Hold Time	0	100		ns
t_R	SDA and SCL Rise Time (10% to 90% of Vcc)	10		100	ns
t_F	SDA and SCL Fall Time	10		100	ns

RESET AC SPECIFICATIONS

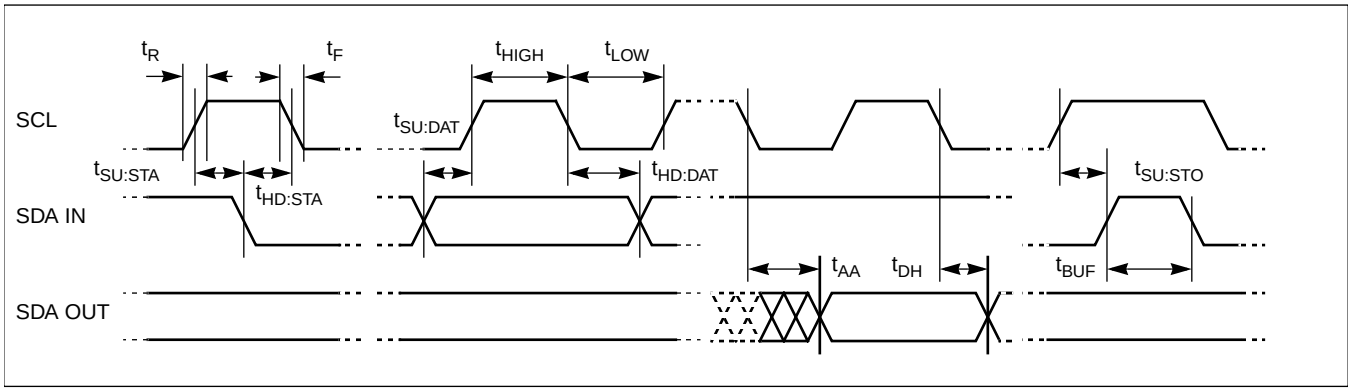
Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}(1)	Write Cycle Time		5	10	mS

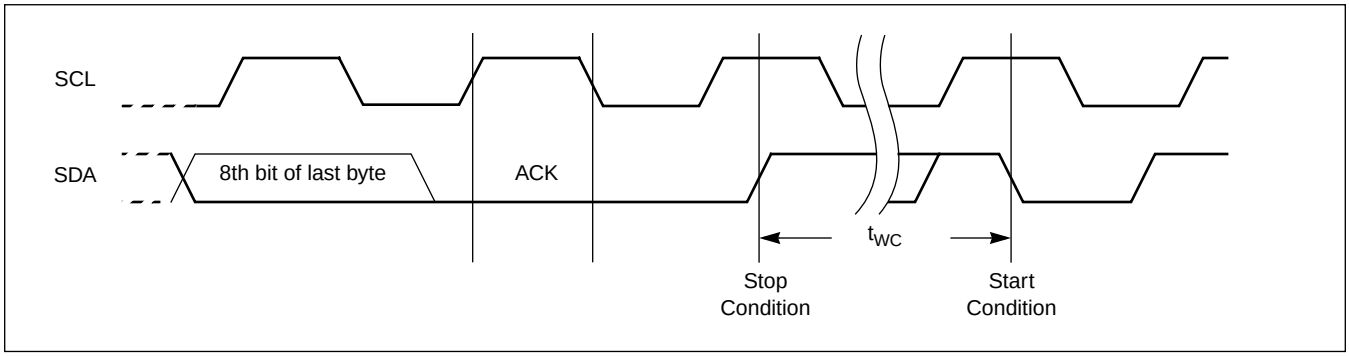
Notes: 1. t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

TIMING DIAGRAMS

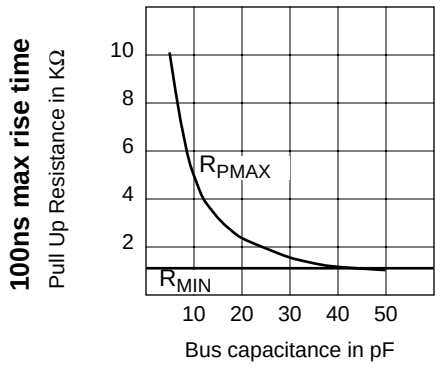
Bus Timing



Write Cycle Timing



GUIDELINES FOR CALCULATING TYPICAL VALUES OF BUS PULL UP RESISTORS



$$R_{MIN} = \frac{V_{CCMAX} - 0.4}{I_{OLMIN}} = 1100\Omega$$

$$V_{IH} = Vcc\left(1 - e^{\frac{-t_{RMAX}}{R_{PMAX}C_{BUS}}}\right)$$

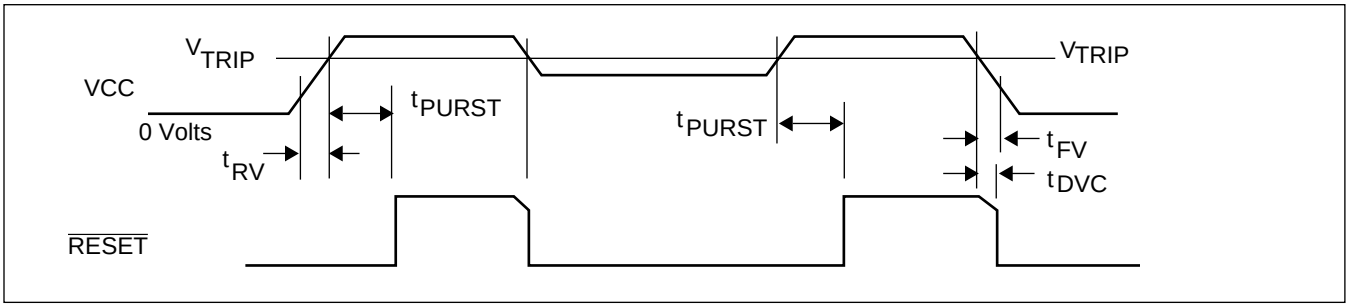
For $V_{IH} = 0.9V_{CC}$

$$R_{PMAX} = \frac{t_R}{2.3(C_{BUS})}$$

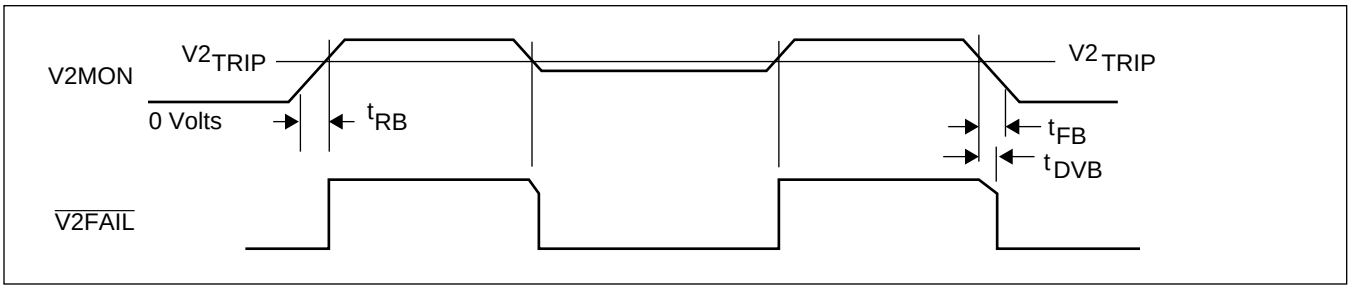
t_{RMAX} = maximum allowable SDA rise time

POWER-UP AND POWER-DOWN TIMING

$\overline{\text{RESET}}$ Output Timing



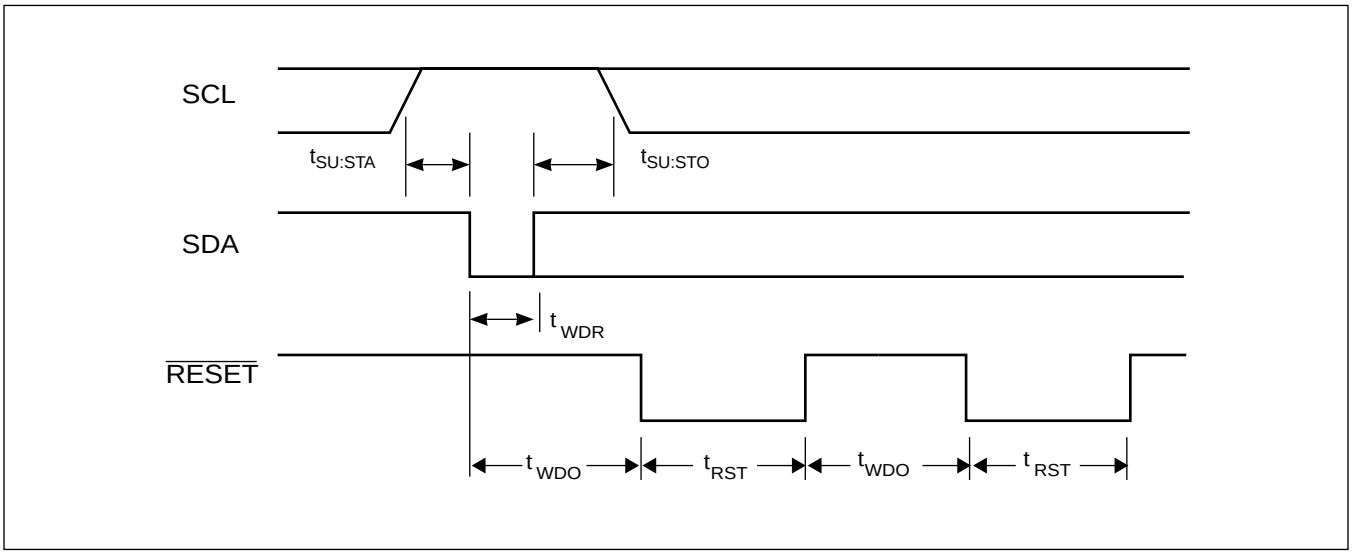
$\overline{\text{V2FAIL}}$ Output Timing



Symbol	Parameter	Min.	Typ.	Max.	Units
V_{TRIP}	$\overline{RESET}$ Trip Point Voltage	2.4	–	3.5	V
V_{2TRIP}	$\overline{V2FAIL}$ Trip Point Voltage	1.7	–	3.5	V
V_{TH}	V_{TRIP} Hysteresis (HIGH to LOW vs. LOW to HIGH V_{TRIP} voltage)		40		mV
V_{2TA}	V_{2TRIP} Hysteresis (HIGH to LOW vs. LOW to HIGH V_{TRIP} voltage)		40		mV
t_{PURST}	Power-up Reset Timeout	75	150	225	ms
t_{DVC}(5)	Detect V_{CC} Low Voltage to Reset Output (Vcc = 2.3V)			65	µs
t_{DVB}(5)	Detect V_{2MON} Low Voltage to Reset Output (Vcc = 2.5-3.7V)			100	µs
t_{FV}(5)	V_{CC} Fall Time	100			µs
t_{RV}(5)	V_{CC} Rise Time	100			µs
t_{FB}(5)	V_{2MON} Fall Time	500			ns
t_{RB}(5)	V_{2MON} Rise Time	500			ns
V_{RVALID}	Reset Valid V_{CC}	1			V

Notes: (5) This parameter is periodically sampled and not 100% tested.
(6) Typical values not tested.

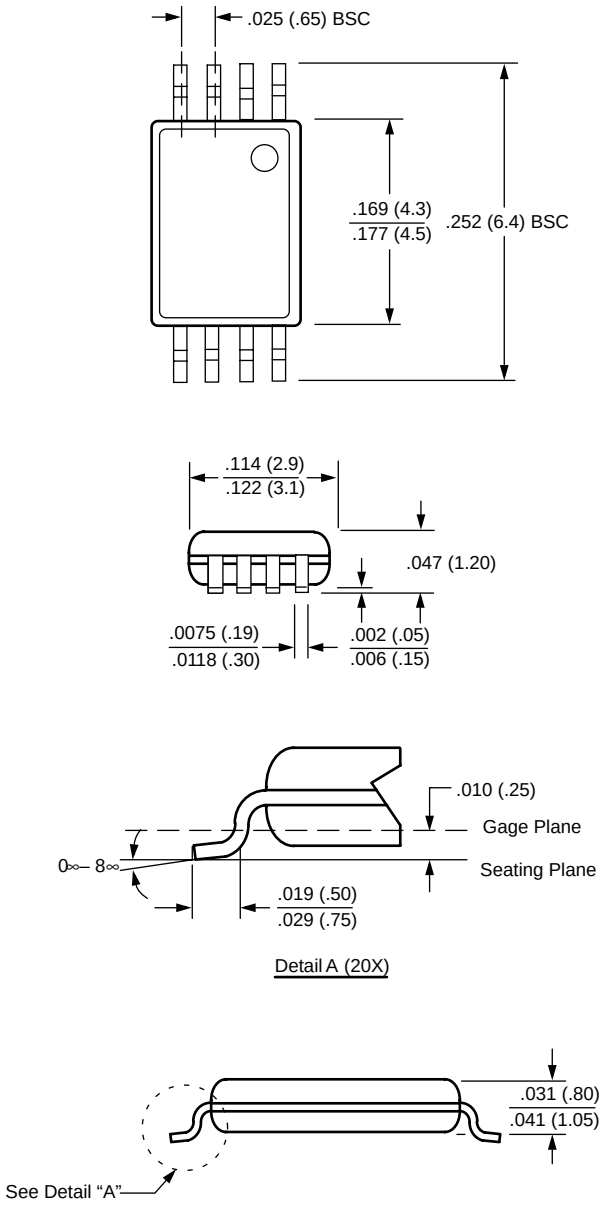
Start Bit vs. $\overline{RESET}$ Timing



RESET Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{WDO}	Watchdog Timeout Period,				
	WD2 = 0, WD1 = 1, WD0 = 0	75	150	225	ms
	WD2 = 0, WD1 = 0, WD0 = 1	225	450	675	ms
	WD2 = 0, WD1 = 0, WD0 = 0	0.5	1	1.5	sec
	WD2 = 1, WD1 = 1, WD0 = 1	2.5	5	7.5	sec
	WD2 = 1, WD1 = 1, WD0 = 0	5	10	15	sec
	WD2 = 1, WD1 = 0, WD0 = 1	10	20	30	sec
	WD2 = 1, WD1 = 0, WD0 = 0	30	60	90	sec
t_{WDR}	SDA LOW duration (Reset the Watchdog)	400			ns
t_{RST}	Reset Timeout	75	150	225	ms

8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

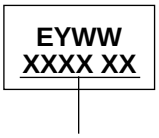
ORDERING INFORMATION

V_{CC} Range	V_{TRIP}	V_{2TRIP}	Package	Operating Temperature Range	Part Number
2.5–3.7V	3.1	2.6	8L TSSOP	0°C–70°C	X46402V8-3.1
				-20°C–85°C	X46402V8E-3.1
2.5–3.7V	3.1	1.7	8L TSSOP	0°C–70°C	X46402V8-3.1A
				-20°C–85°C	X46402V8E-3.1A
2.5–3.7V	2.9	2.3	8L TSSOP	0°C–70°C	X46402V8-2.9
				-20°C–85°C	X46402V8E-2.9

Notes: Tolerance for Vtrip and V2trip are +/-5%

PART MARK CONVENTION

8-Lead TSSOP



	V_{TRIP}	$V2_{TRIP}$	Temp
4642 AR =	3.1	2.6	0 to 70° C
4642 AS =	3.1	2.6	-20 to 85°C
4642 AT =	3.1	1.7	0 to 70° C
4642 AU =	3.1	1.7	-20 to 85°C
4642 AV =	2.9	2.3	0 to 70° C
4642 AW =	2.9	2.3	-20 to 85°C