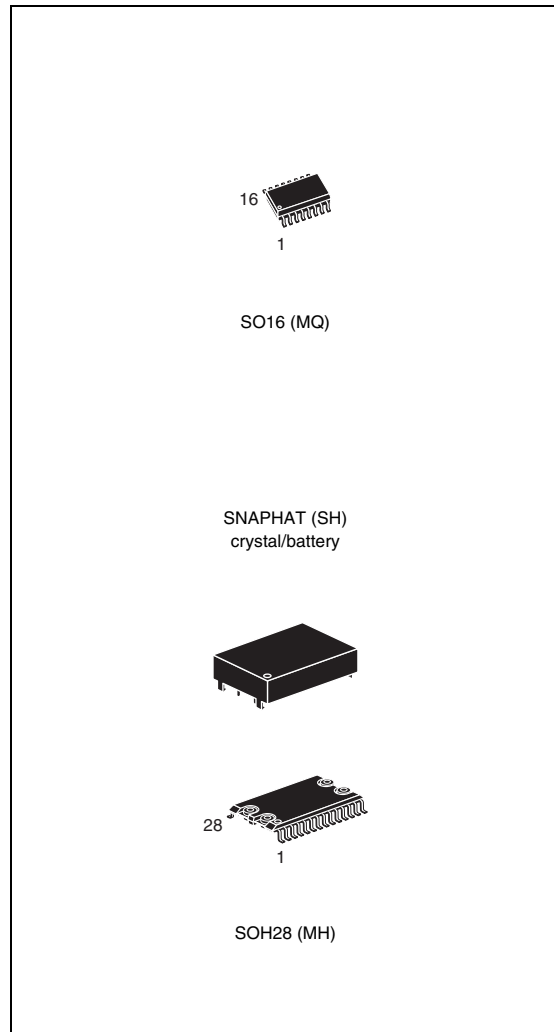


## 5 V or 3 V NVRAM supervisor for up to 8 LPSRAMs

Not recommended for new design

### Features

- Converts low power SRAM into NVRAMs
- Precision power monitoring and power switching circuitry
- Automatic WRITE-protection when  $V_{CC}$  is out-of-tolerance
- Two-input decoder allows control for up to 8 SRAMs (with 2 devices active in parallel)
- Choice of supply voltages and power-fail deselect voltages:
  - M40Z300:
    - $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$
    - $\text{THS} = V_{SS}: 4.5 \text{ V} \leq V_{PFD} \leq 4.75 \text{ V}$
    - $\text{THS} = V_{OUT}: 4.2 \text{ V} \leq V_{PFD} \leq 4.5 \text{ V}$
  - M40Z300W:
    - $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$
    - $\text{THS} = V_{SS}: 2.8 \text{ V} \leq V_{PFD} \leq 3.0 \text{ V}$
    - $V_{CC} = 2.7 \text{ V to } 3.3 \text{ V}$
    - $\text{THS} = V_{OUT}: 2.5 \text{ V} \leq V_{PFD} \leq 2.7 \text{ V}$
- Reset output ( $\overline{\text{RST}}$ ) for power on reset
- Battery low pin ( $\overline{\text{BL}}$ )
- Less than 12 ns chip enable access propagation delay (for 5.0 V device)
- Packaging includes a 28-lead SOIC and SNAPHAT<sup>®</sup> top (to be ordered separately), or A 16-lead SOIC
- SOIC package provides direct connection for a SNAPHAT top which contains the battery
- RoHS compliant
  - Lead-free second level interconnect



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# 1 Description

The M40Z300/W NVRAM supervisor is a self-contained device which converts a standard low-power SRAM into a non-volatile memory. A precision voltage reference and comparator monitors the  $V_{CC}$  input for an out-of-tolerance condition.

When an invalid  $V_{CC}$  condition occurs, the conditioned chip enable outputs ( $\overline{E1}_{CON}$  to  $\overline{E4}_{CON}$ ) are forced inactive to write-protect the stored data in the SRAM. During a power failure, the SRAM is switched from the  $V_{CC}$  pin to the lithium cell within the SNAPHAT<sup>®</sup> to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns.

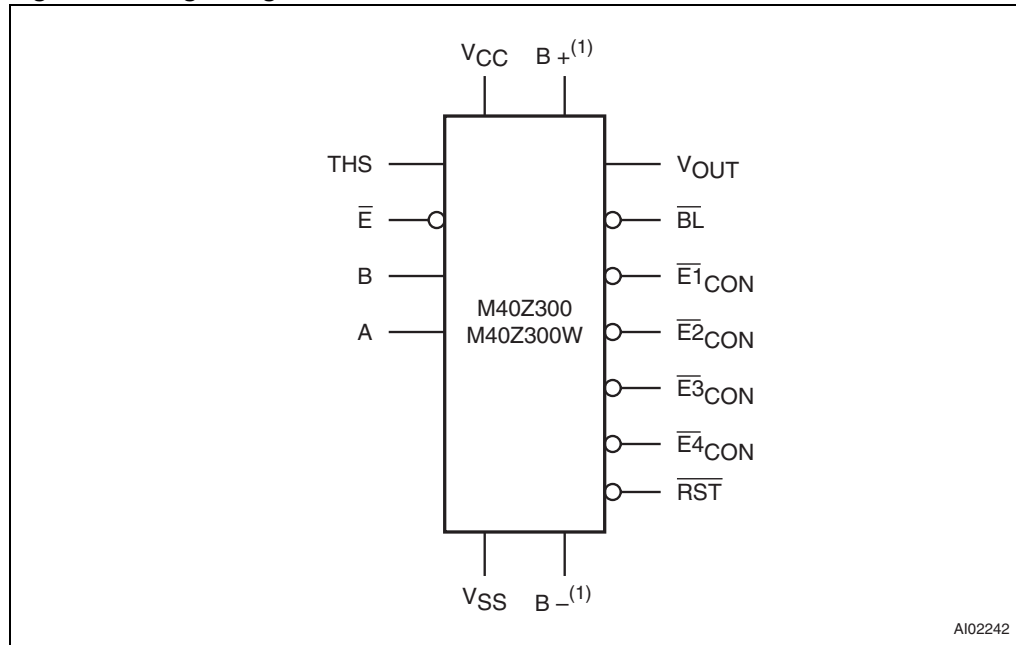
The 28-pin, 330 mil SOIC provides sockets with gold plated contacts for direct connection to a separate SNAPHAT housing containing the battery. The SNAPHAT housing has gold plated pins which mate with the sockets, ensuring reliable connection. The housing is keyed to prevent improper insertion. This unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process which greatly reduces the board manufacturing process complexity of either directly soldering or inserting a battery into a soldered holder. Providing non-volatility becomes a "SNAP." The 16-pin SOIC provides battery pins for an external user-supplied battery.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The 28-pin SOIC and battery packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is "M4ZXX-BR00SH".

**Caution:** Do not place the SNAPHAT battery top in conductive foam, as this will drain the lithium button-cell battery.

Figure 1. Logic diagram



1. For 16-pin SOIC package only.

Table 1. Signal names

THS	Threshold select input
$\overline{E}$	Chip enable input
$\overline{E1}_{CON}$ - $\overline{E4}_{CON}$	Conditioned chip enable output
A, B	Decoder inputs
$\overline{RST}$	Reset output (open drain)
$\overline{BL}$	Battery low output (open drain)
$V_{OUT}$	Supply voltage output
$V_{CC}$	Supply voltage
$V_{SS}$	Ground
B +	Positive battery pin
B -	Negative battery pin <sup>(1)</sup>
NC	Not connected internally

1. For M40Z300W, B- must be connected to the negative battery terminal only (not to pin 8,  $V_{SS}$ ).

Figure 2. 28-pin SOIC connections

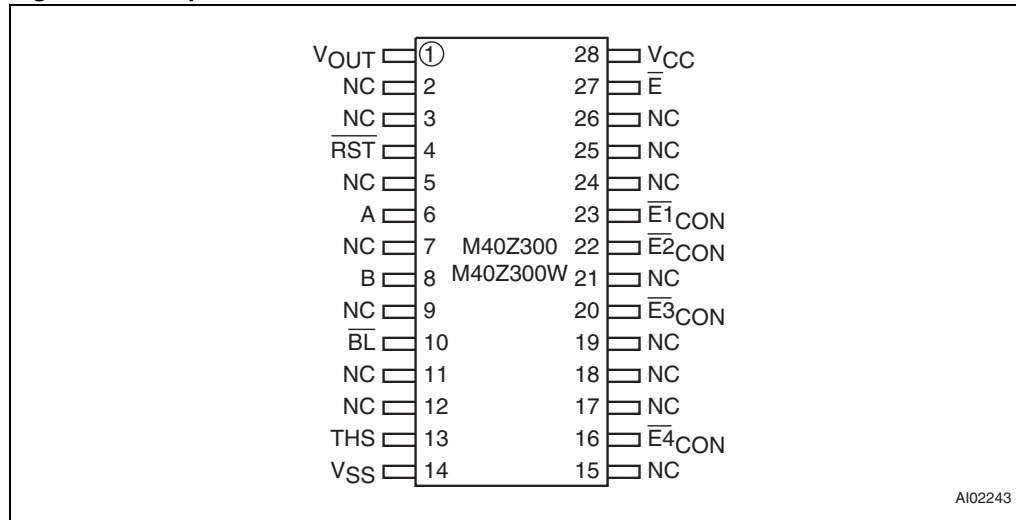


Figure 3. M40Z300 16-pin SOIC connections

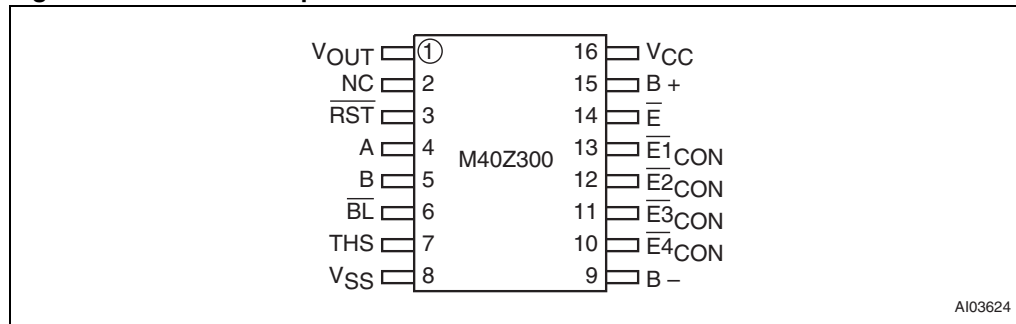
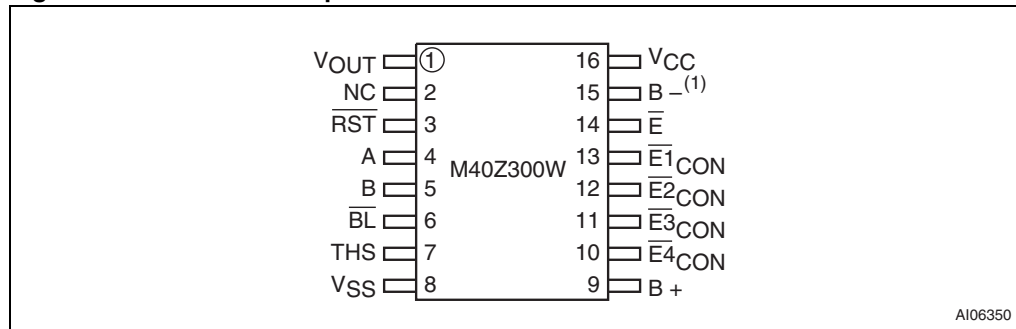
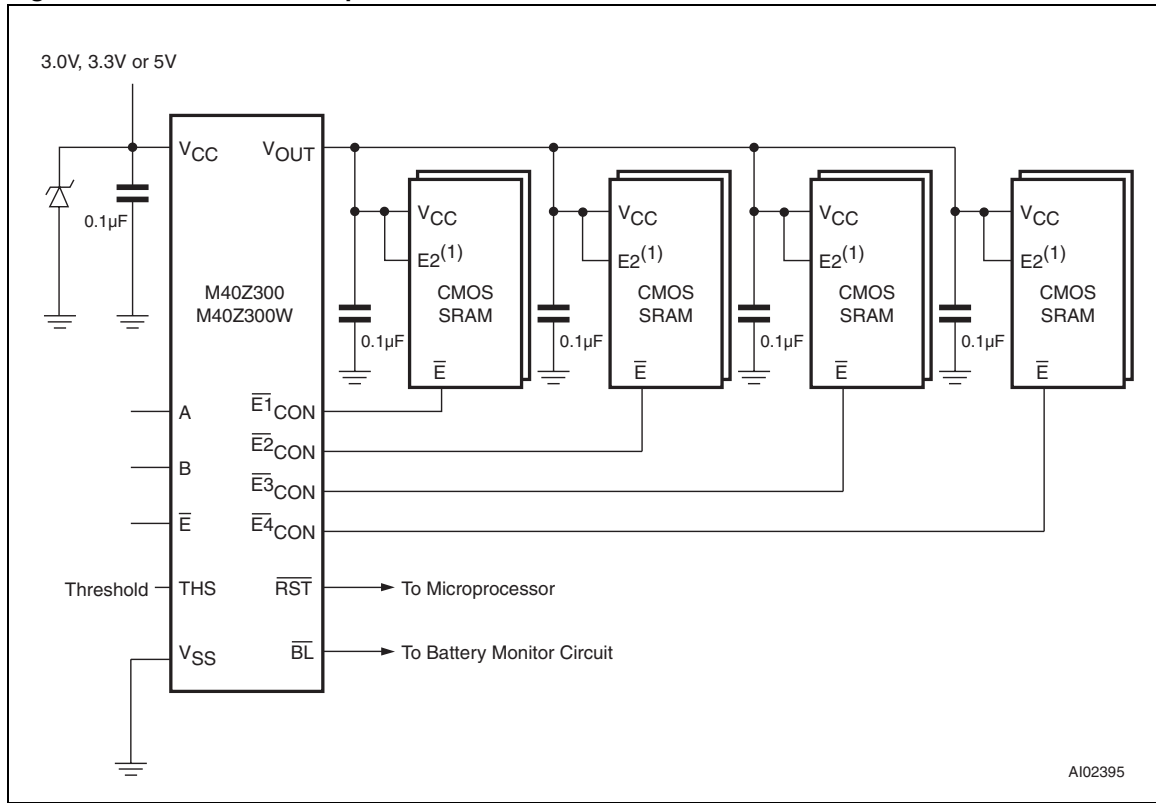


Figure 4. M40Z300W 16-pin SOIC connections



1. For M40Z300W, B- must be connected to the negative battery terminal only (not to pin 8, VSS).

Figure 5. Hardware hookup



1. If the second chip enable pin (E2) is unused, it should be tied to  $V_{OUT}$ .



## 2 Operation

The M40Z300/W, as shown in [Figure 5 on page 8](#), can control up to four (eight, if placed in parallel) standard low-power SRAMs. These SRAMs must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ( $\overline{E1}_{CON}$  to  $\overline{E4}_{CON}$ ) output pins follow the chip enable ( $\overline{E}$ ) input pin with timing shown in [Figure 6 on page 10](#) and [Table 7 on page 17](#). An internal switch connects  $V_{CC}$  to  $V_{OUT}$ . This switch has a voltage drop of less than 0.3V ( $I_{OUT1}$ ).

When  $V_{CC}$  degrades during a power failure,  $\overline{E1}_{CON}$  to  $\overline{E4}_{CON}$  are forced inactive independent of  $\overline{E}$ . In this situation, the SRAM is unconditionally write protected as  $V_{CC}$  falls below an out-of-tolerance threshold ( $V_{PFD}$ ). For the M40Z300 the power fail detection value associated with  $V_{PFD}$  is selected by the Threshold Select (THS) pin and is shown in [Table 6 on page 15](#). For the M40Z300W, the THS pin selects both the supply voltage and  $V_{PFD}$  (also shown in [Table 6 on page 15](#)).

*Note:* In either case, THS pin must be connected to either  $V_{SS}$  or  $V_{OUT}$ .

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time  $t_{WPT}$ ,  $\overline{E1}_{CON}$  to  $\overline{E4}_{CON}$  are unconditionally driven high, write protecting the SRAM. A power failure during a WRITE cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below  $V_{PFD}$  (min), the user can be assured the memory will be write protected within the Write Protect Time ( $t_{WPT}$ ) provided the  $V_{CC}$  fall time exceeds  $t_F$  (see [Figure 6 on page 10](#)).

As  $V_{CC}$  continues to degrade, the internal switch disconnects  $V_{CC}$  and connects the internal battery to  $V_{OUT}$ . This occurs at the switchover voltage ( $V_{SO}$ ). Below the  $V_{SO}$ , the battery provides a voltage  $V_{OHB}$  to the SRAM and can supply current  $I_{OUT2}$  (see [Table 6 on page 15](#)).

When  $V_{CC}$  rises above  $V_{SO}$ ,  $V_{OUT}$  is switched back to the supply voltage. Outputs  $\overline{E1}_{CON}$  to  $\overline{E4}_{CON}$  are held inactive for  $t_{CER}$  (120ms maximum) after the power supply has reached  $V_{PFD}$ , independent of the  $\overline{E}$  input, to allow for processor stabilization (see [Figure 10 on page 16](#)).

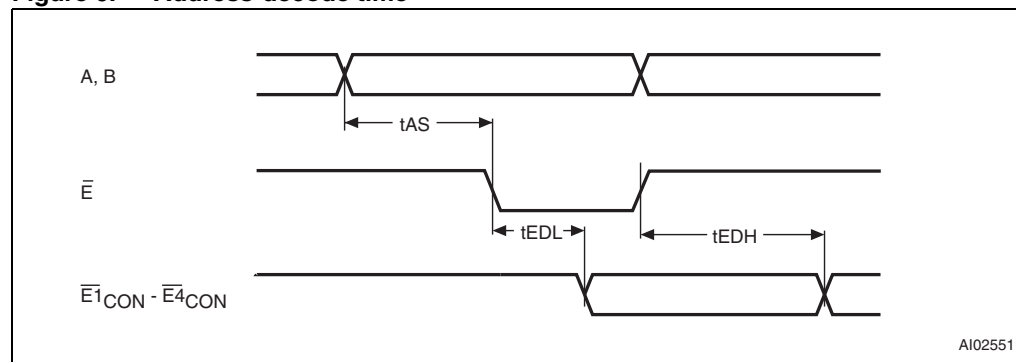
## 2.1 Two to four decode

The M40Z300/W includes a 2 input (A, B) decoder which allows the control of up to 4 independent SRAMs. The truth table for these inputs is shown in [Table 2](#).

**Table 2. Truth table**

Inputs			Outputs			
$\bar{E}$	B	A	$\bar{E}1_{CON}$	$\bar{E}2_{CON}$	$\bar{E}3_{CON}$	$\bar{E}4_{CON}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

**Figure 6. Address-decode time**



*Note:* During system design, compliance with the SRAM timing parameters must comprehend the propagation delay between  $\bar{E}1_{CON}$  -  $\bar{E}4_{CON}$ .

## 2.2 Data retention lifetime calculation

Most low power SRAMs on the market today can be used with the M40Z300/W NVRAM SUPERVISOR. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40Z300/W and SRAMs to be “Don't Care” once  $V_{CC}$  falls below  $V_{PFD}(\min)$ . The SRAM should also guarantee data retention down to  $V_{CC} = 2.0$  V. The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included. If the SRAM includes a second chip enable pin ( $\bar{E}2$ ), this pin should be tied to  $V_{OUT}$ .

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0 V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use.

The data retention current value of the SRAMs can then be added to the  $I_{BAT}$  value of the M40Z300/W to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT<sup>®</sup> of your choice can then be divided by this current to determine the amount of data retention available (see [Table 13 on page 23](#)).

**Caution:** Take care to avoid inadvertent discharge through  $V_{OUT}$  and  $\overline{E1}_{CON}$  -  $\overline{E4}_{CON}$  after battery has been attached.

For a further more detailed review of lifetime calculations, please see application note AN1012.

## 2.3 Power-on reset output

All microprocessors have a reset input which forces them to a known state when starting. The M40Z300/W has a reset output ( $\overline{RST}$ ) pin which is guaranteed to be low within  $t_{WPT}$  of  $V_{PFD}$  (see [Table 7](#)). This signal is an open drain configuration. An appropriate pull-up resistor should be chosen to control the rise time. This signal will be valid for all voltage conditions, even when  $V_{CC}$  equals  $V_{SS}$ .

Once  $V_{CC}$  exceeds the power failure detect voltage  $V_{PFD}$ , an internal timer keeps  $\overline{RST}$  low for  $t_{REC}$  to allow the power supply to stabilize.

## 2.4 Battery low pin

The M40Z300/W automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The battery low (BL) pin will be asserted if the battery voltage is found to be less than approximately 2.5 V. The  $\overline{BL}$  pin will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below 2.5 V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal  $V_{CC}$  is supplied. In order to insure data integrity during subsequent periods of battery backup mode, the battery should be replaced. The SNAPHAT<sup>®</sup> top should be replaced with valid  $V_{CC}$  applied to the device.

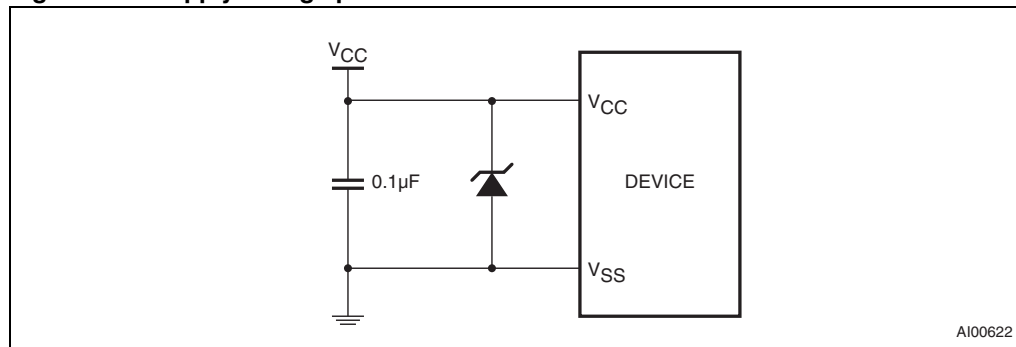
The M40Z300/W only monitors the battery when a nominal  $V_{CC}$  is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The  $\overline{BL}$  pin is an open drain output and an appropriate pull-up resistor to  $V_{CC}$  should be chosen to control the rise time.

## 2.5 $V_{CC}$ noise and negative going transients

$I_{CC}$  transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the  $V_{CC}$  bus. These transients can be reduced if capacitors are used to store energy which stabilizes the  $V_{CC}$  bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of  $0.1 \mu\text{F}$  (as shown in [Figure 7](#)) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on  $V_{CC}$  that drive it to values below  $V_{SS}$  by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from  $V_{CC}$  to  $V_{SS}$  (cathode connected to  $V_{CC}$ , anode to  $V_{SS}$ ). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

**Figure 7. Supply voltage protection**



### 3 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit	
T <sub>A</sub>	Ambient operating temperature	Grade 1	0 to 70	°C
		Grade 6	-40 to 85	°C
T <sub>STG</sub>	Storage temperature	SNAPHAT®	-40 to 85	°C
		SOIC	-55 to 125	°C
T <sub>SLD</sub> <sup>(1)</sup>	Lead solder temperature for 10 seconds	260	°C	
V <sub>IO</sub>	Input or output voltage	-0.3 to V <sub>CC</sub> + 0.3	V	
V <sub>CC</sub>	Supply voltage	M40Z300	-0.3 to 7.0	V
		M40Z300W	-0.3 to 4.6	V
I <sub>O</sub>	Output current	20	mA	
P <sub>D</sub>	Power dissipation	1	W	

1. For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

**Caution:** Negative undershoots below -0.3 V are not allowed on any pin while in the battery backup mode.

**Caution:** Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

## 4 DC and AC parameters

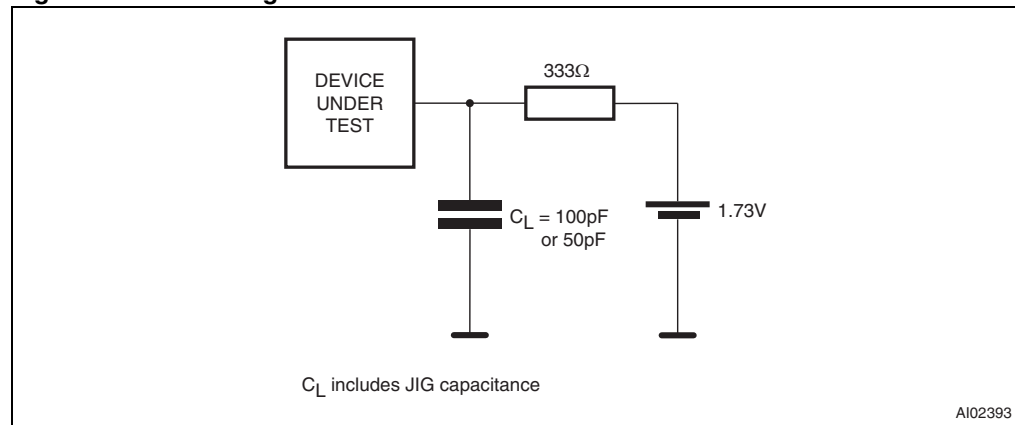
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in [Table 4: DC and AC measurement conditions](#). Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 4. DC and AC measurement conditions**

Parameter		M40Z300	M40Z300W
V <sub>CC</sub> supply voltage		4.5 to 5.5 V	2.7 to 3.6 V
Ambient operating temperature	Grade 1	0 to 70 °C	0 to 70 °C
	Grade 6	-40 to 85 °C	-40 to 85 °C
Load capacitance (C <sub>L</sub> )		100 pF	50 pF
Input rise and fall times		≤ 5 ns	≤ 5 ns
Input pulse voltages		0 to 3 V	0 to 3 V
Input and output timing ref. voltages		1.5 V	1.5 V

*Note:* Output High Z is defined as the point where data is no longer driven.

**Figure 8. AC testing load circuit**



*Note:* 50 pF for M40Z300W.

**Table 5. Capacitance**

Symbol	Parameter <sup>(1)(2)</sup>	Min	Max	Unit
C <sub>IN</sub>	Input capacitance	-	8	pF
C <sub>OUT</sub> <sup>(3)</sup>	Input/output capacitance	-	10	pF

1. Sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 6. DC characteristics

Sym	Parameter	Test condition <sup>(1)</sup>	M40Z300			M40Z300W			Unit
			Min	Typ	Max	Min	Typ	Max	
$I_{LI}^{(2)}$	Input leakage current	$0 V \leq V_{IN} \leq V_{CC}$			$\pm 1$			$\pm 1$	$\mu A$
$I_{CC}$	Supply current	Outputs open		3	6		2	4	mA
$V_{IL}$	Input low voltage		-0.3		0.8	-0.3		0.8	V
$V_{IH}$	Input high voltage		2.2		$V_{CC} + 0.3$	2.0		$V_{CC} + 0.3$	V
$V_{OL}$	Output low voltage	$I_{OL} = 4.0 \text{ mA}$			0.4			0.4	V
	Output low voltage (open drain) <sup>(3)</sup>	$I_{OL} = 10 \text{ mA}$			0.4			0.4	V
$V_{OH}$	Output high voltage	$I_{OH} = -2.0 \text{ mA}$	2.4			2.4			V
$V_{OHB}$	$V_{OH}$ battery backup <sup>(4)</sup>	$I_{OUT2} = -1.0 \mu A$	2.0	2.9	3.6	2.0	2.9	3.6	V
$I_{OUT1}$	$V_{OUT}$ current (active)	$V_{OUT} > V_{CC} - 0.3$			250			150	mA
		$V_{OUT} > V_{CC} - 0.2$			150			100	mA
$I_{OUT2}$	$V_{OUT}$ current (battery backup)	$V_{OUT} > V_{BAT} - 0.3$		100			100		$\mu A$
$I_{CCDR}$	Data retention mode current <sup>(5)</sup>				100			100	nA
THS	Threshold select voltage		$V_{SS}$		$V_{OUT}$	$V_{SS}$		$V_{OUT}$	V
$V_{PFD}$	Power-fail deselect voltage (THS = $V_{SS}$ )		4.5	4.6	4.75	2.8	2.9	3.0	V
	Power-fail deselect voltage (THS = $V_{OUT}$ )		4.2	4.35	4.5	2.5	2.6	2.7	V
$V_{SO}$	Battery backup switchover voltage			3.0			2.5		V
$V_{BAT}$	Battery voltage		2.0	2.9	3.6	2.0	2.9	3.6	V

- Valid for ambient operating temperature:  $T_A = 0$  to  $70$  °C or  $-40$  to  $85$  °C;  $V_{CC} = 2.7$  to  $3.6$  V or  $4.5$  to  $5.5$  V (except where noted).
- Outputs deselected.
- For  $\overline{RST}$  &  $\overline{BL}$  pins (open drain).
- Chip enable outputs ( $\overline{E1}_{CON}$  -  $\overline{E4}_{CON}$ ) can only sustain CMOS leakage currents in the battery backup mode. Higher leakage currents will reduce battery life.
- Measured with  $V_{OUT}$  and  $\overline{E1}_{CON}$  -  $\overline{E4}_{CON}$  open.

Figure 9. Power-down timing

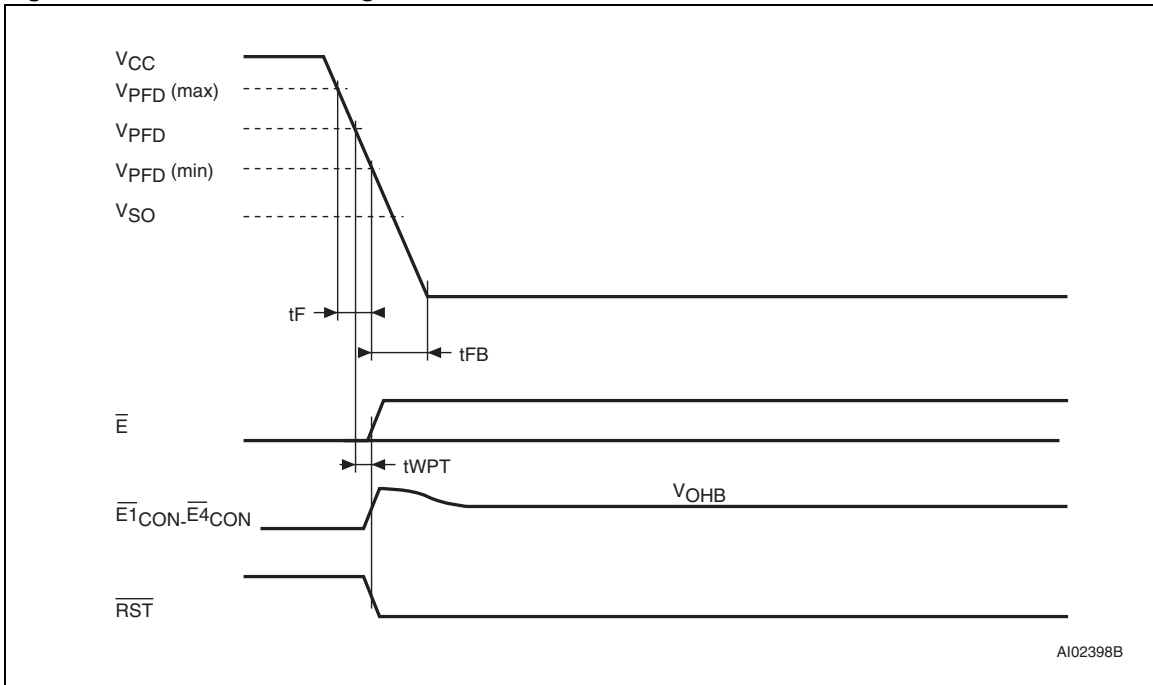
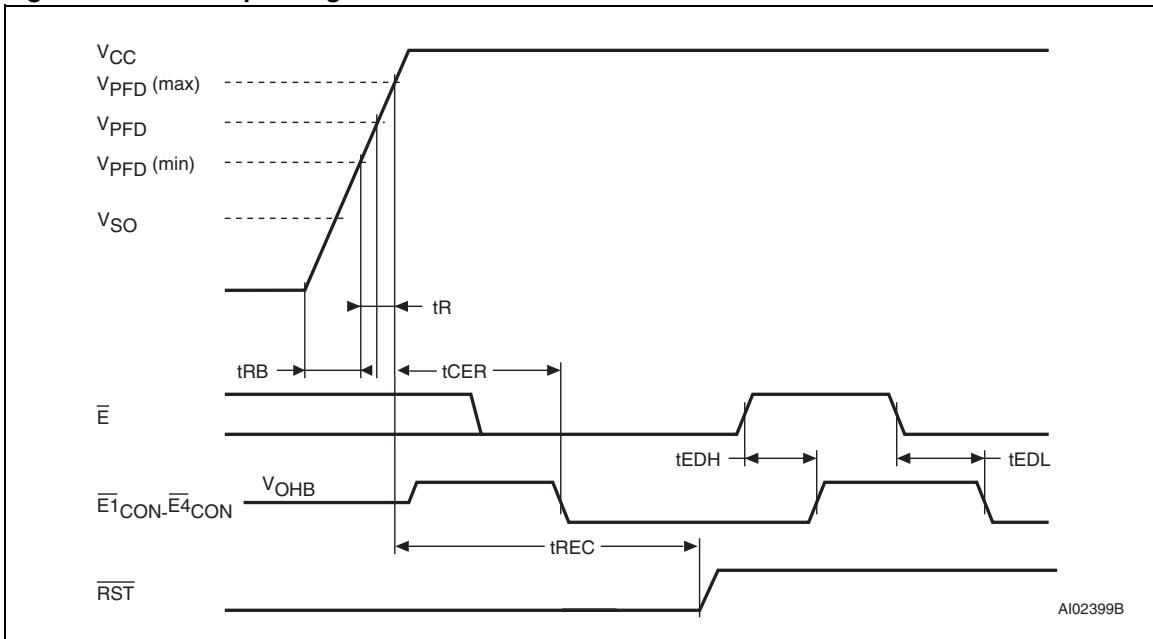


Figure 10. Power-up timing





**Table 7. Power down/up mode AC characteristics**

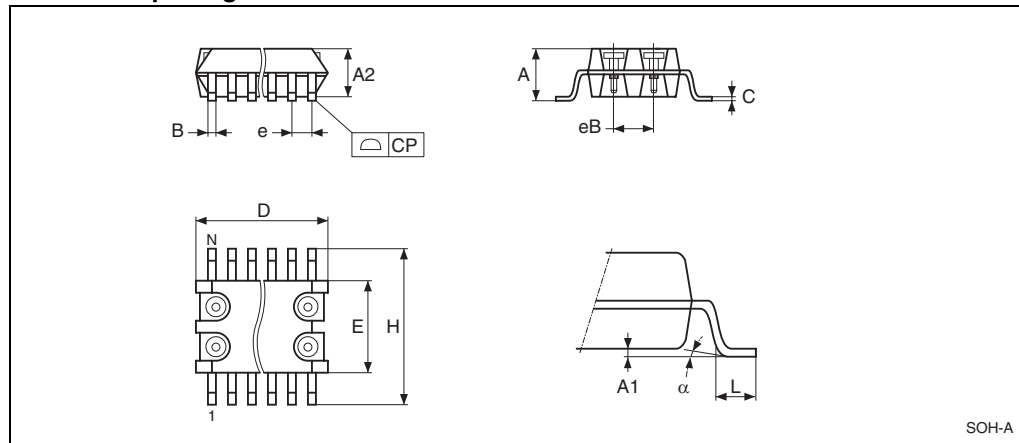
Symbol	Parameter <sup>(1)</sup>	Min	Max	Unit	
$t_F^{(2)}$	$V_{PFD}(\text{max})$ to $V_{PFD}(\text{min})$ $V_{CC}$ fall time	300		$\mu\text{s}$	
$t_{FB}^{(3)}$	$V_{PFD}(\text{min})$ to $V_{SS}$ $V_{CC}$ fall time	M40Z300	10	$\mu\text{s}$	
		M40Z300W	150	$\mu\text{s}$	
$t_R$	$V_{PFD}(\text{min})$ to $V_{PFD}(\text{max})$ $V_{CC}$ rise time	10		$\mu\text{s}$	
$t_{EDL}$	Chip enable propagation delay low	M40Z300	12	ns	
		M40Z300W	20	ns	
$t_{EDH}$	Chip enable propagation delay high	M40Z300	10	ns	
		M40Z300W	20	ns	
$t_{AS}$	A, B set up to $\overline{E}$	0		ns	
$t_{CER}$	Chip enable recovery	40	120	ms	
$t_{REC}^{(4)}$	$V_{PFD}(\text{max})$ to $\overline{RST}$ high	40	120	ms	
$t_{WPT}$	Write protect time	M40Z300	40	150	$\mu\text{s}$
		M40Z300W	40	250	$\mu\text{s}$
$t_{RB}$	$V_{SS}$ to $V_{PFD}(\text{min})$ $V_{CC}$ rise time	1		$\mu\text{s}$	

- Valid for ambient operating temperature:  $T_A = 0$  to  $70$  °C or  $-40$  to  $85$  °C;  $V_{CC} = 2.7$  to  $3.6$  V or  $4.5$  to  $5.5$  V (except where noted).
- $V_{PFD}(\text{max})$  to  $V_{PFD}(\text{min})$  fall time of less than  $t_F$  may result in deselection/write protection not occurring until  $200$   $\mu\text{s}$  after  $V_{CC}$  passes  $V_{PFD}(\text{min})$ .
- $V_{PFD}(\text{min})$  to  $V_{SS}$  fall time of less than  $t_{FB}$  may cause corruption of RAM data.
- $t_{REC}(\text{min}) = 20\text{ms}$  for industrial temperature Grade 6 device.

## 5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Figure 11. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, package outline**

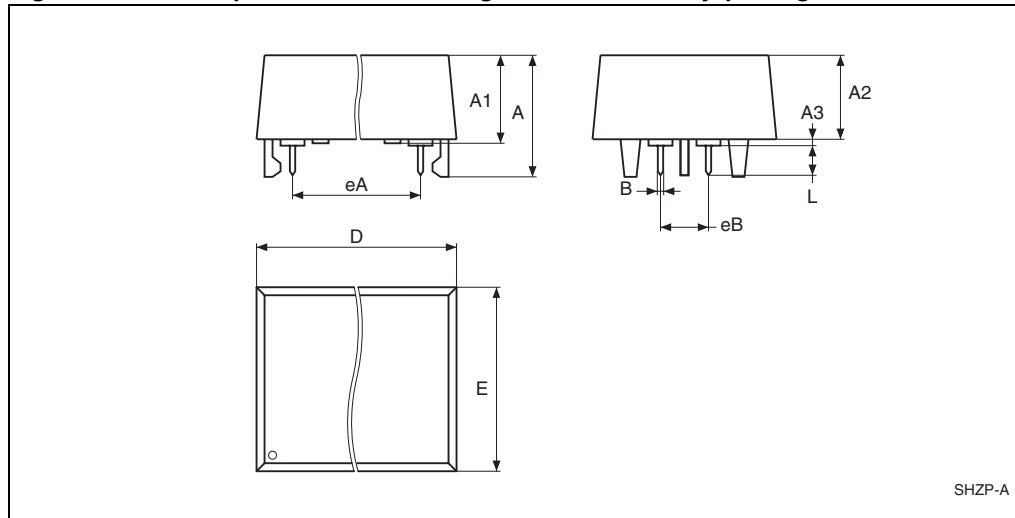


Note: Drawing is not to scale.

**Table 8. SOH28 – 28-lead plastic small outline, battery SNAPHAT, package mechanical data**

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N		28			28	
CP			0.10			0.004

Figure 12. SH – 4-pin SNAPHAT housing for 48 mAh battery, package outline

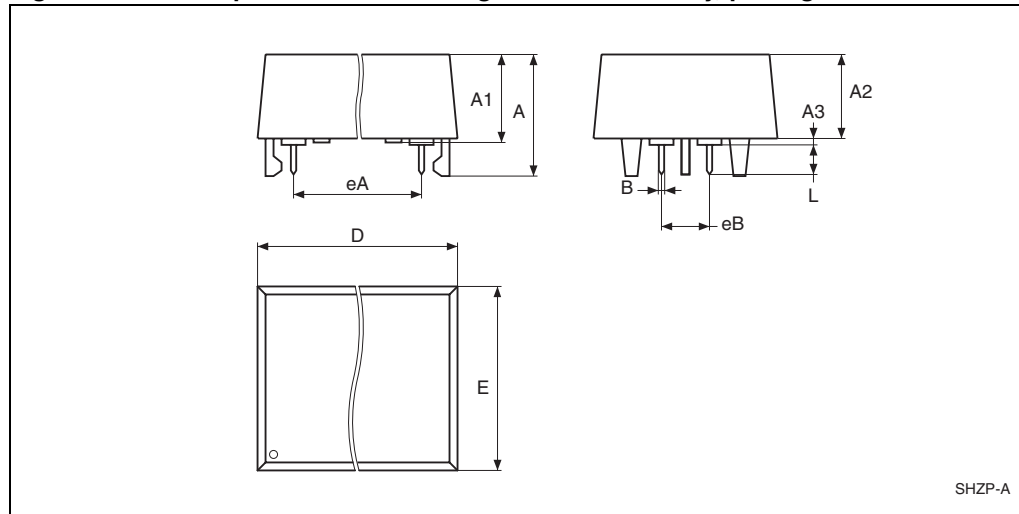


Note: Drawing is not to scale.

Table 9. SH – 4-pin SNAPHAT housing for 48 mAh battery, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

Figure 13. SH – 4-pin SNAPHAT housing for 120mAh battery, package outline

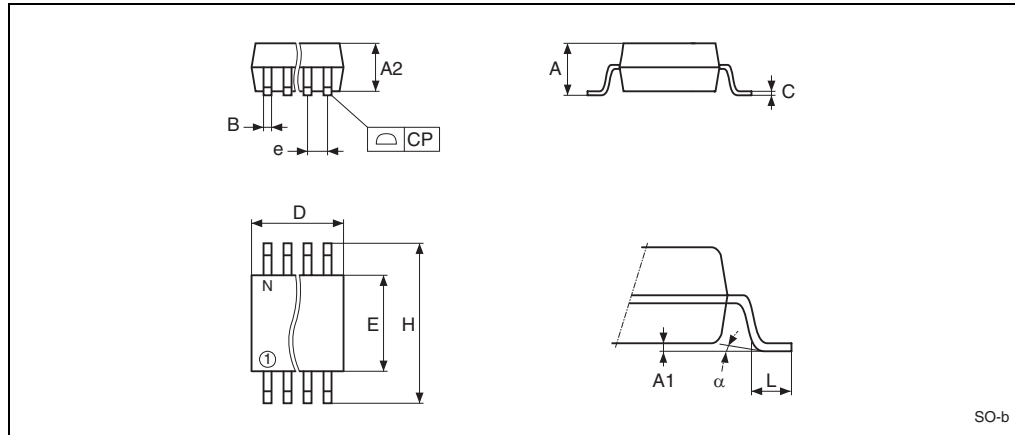


Note: Drawing is not to scale.

Table 10. SH – 4-pin SNAPHAT housing for 120 mAh battery, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	.0335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

**Figure 14. SO16 – 16-lead plastic small outline, 150 mils body width, package outline**



Note: Drawing is not to scale.

**Table 11. SO16 – 16-lead plastic small outline, 150 mils body width, package mechanical data**

Symbol	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2			1.60			0.063
B		0.35	0.46		0.014	0.018
C		0.19	0.25		0.007	0.010
D		9.80	10.00		0.386	0.394
E		3.80	4.00		0.150	0.158
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
L		0.40	1.27		0.016	0.050
a		0°	8°		0°	8°
N	16			16		
CP			0.10			0.004

## 6 Part numbering

**Table 12. Ordering information example**

Example:	M40Z	300W	MH	1	E
<b>Device type</b>					
M40Z					
<b>Supply and write protect voltage</b>					
300 <sup>(1)</sup> = $V_{CC} = 4.5$ to $5.5$ V THS = $V_{SS} = 4.5$ V $\leq V_{PFD} \leq 4.75$ V THS = $V_{OUT} = 4.2$ V $\leq V_{PFD} \leq 4.5$ V 300W <sup>(1)</sup> = $V_{CC} = 3.0$ to $3.6$ V THS = $V_{SS} = 2.8$ V $\leq V_{PFD} \leq 3.0$ V $V_{CC} = 2.7$ V to $3.3$ V THS = $V_{OUT} = 2.5$ V $\leq V_{PFD} \leq 2.7$ V					
<b>Package</b>					
MH <sup>(2)</sup> = SOH28 MQ = SO16					
<b>Temperature range</b>					
1 = 0 to 70 °C 6 = -40 to 85 °C					
<b>Shipping method for SOIC</b>					
E = Lead-free package (ECOPACK <sup>®</sup> ), tubes F = Lead-free package (ECOPACK <sup>®</sup> ), tape & reel					

1. Not recommended for new design. Contact ST sales office for availability.
2. The SOIC package (SOH28) requires the battery package (SNAPHAT<sup>®</sup>) which is ordered separately under the part number "M4Zxx-BR00SH" in plastic tubes or "M4Zxx-BR00SHTR" in tape & reel form.

**Caution:** Do not place the SNAPHAT battery package "M4Zxx-BR00SH" in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you

**Table 13. SNAPHAT<sup>®</sup> battery table**

Part number	Description	Package
M4Z28-BR00SH1	Lithium battery (48 mAh) SNAPHAT	SH
M4Z32-BR00SH1	Lithium battery (120 mAh) SNAPHAT	SH

## 7 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
Mar-1999	1.0	First issue
08-Mar-2000	1.1	Document layout changed; SO16 package added; battery capacity changed ( <a href="#">Table 13</a> )
22-Sep-2000	1.2	SO16 package measures change
23-Feb-2001	1.3	Added information for industrial temperature ( <a href="#">Table 3</a> , <a href="#">7</a> , <a href="#">12</a> )
30-May-2001	1.4	Change "Controller" references to "SUPERVISOR"
10-Jul-2001	2.0	Reformatted; added temp/voltage info. to tables ( <a href="#">Table 6</a> , <a href="#">7</a> ); Figures changed ( <a href="#">Figure 1</a> , <a href="#">3</a> , <a href="#">5</a> , <a href="#">8</a> , <a href="#">6</a> )
01-Aug-2001	2.1	E2 connections added to hookup ( <a href="#">Figure 5</a> )
15-Jan-2002	2.2	16-pin SOIC connections split, graphic added ( <a href="#">Figure 4</a> ); addition to hardware hookup ( <a href="#">Figure 5</a> )
13-May-2002	2.3	Modify reflow time and temperature footnote ( <a href="#">Table 3</a> )
31-Oct-2003	2.4	Update DC characteristics ( <a href="#">Table 6</a> )
04-Nov-2003	2.5	Correct DC characteristics ( <a href="#">Table 6</a> )
23-Feb-2005	3.0	Reformatted; IR reflow, SO package updates ( <a href="#">Table 3</a> )
05-Nov-2007	4.0	Reformatted; added lead-free second level interconnect to cover page and <a href="#">Section 5: Package mechanical data</a> ; updated <a href="#">Figure 10</a> and <a href="#">Table 3</a> , <a href="#">12</a> , <a href="#">13</a> .
19-Oct-2010	5	Devices not recommended for new design, updated document status; updated <a href="#">Table 12</a> , ECOPACK <sup>®</sup> text in <a href="#">Section 5: Package mechanical data</a> ; reformatted document.



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