IP200

Interpolation Circuit for Incremental Measuring Systems

Data Sheet

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Contents

1 Overview

The IP200 interpolation circuit is designed for connection to incremental position and angle measuring systems with sine-shaped output signals with a 90° phase shift. It can be operated at a large number of transducer systems working according to the most varied measuring principles. With a maximum interpolation rate of 200 the IC is capable to split the input signal period into up to 200 segments. A counter value can be output via parallel or serial interface, respectively.

Different interfaces and flexible configuration types enable the use of the IP200 in single-chip interpolation systems, in microcontroller-based measuring devices and in multi-channel systems alike. Proprietary automatic gain and offset control, as well as the possibility of a analogue phase correction ensure a high measuring precision under industrial conditions. The integrated two-level measuring value trigger and the additional parallel high speed output makes the IC suitable for use in real time applications.

Block Diagram

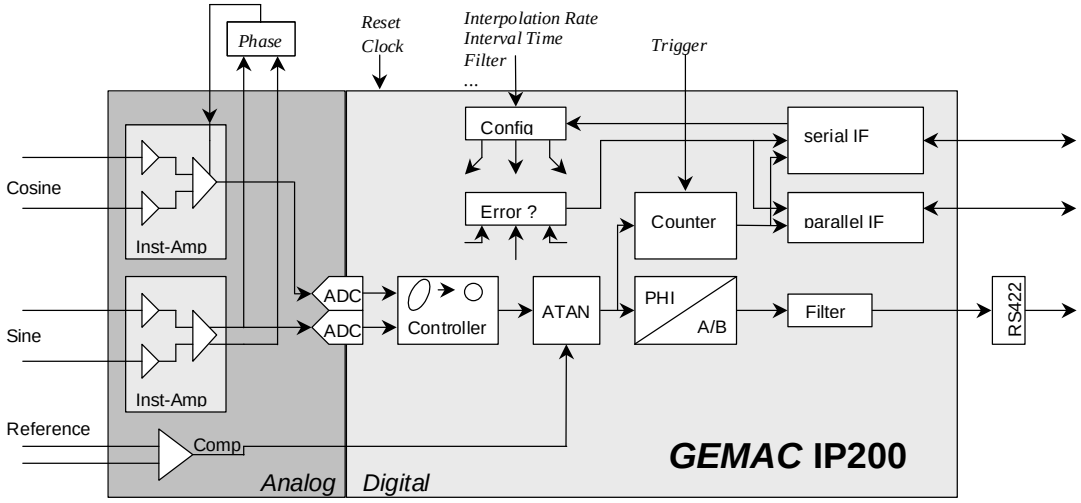


Figure 1

Inst-Amp	Instrumentation amplifier
ADC	Analogue-Digital-Converter
ATAN	ARCTAN-processing-unit
A/B	Generation of the A/B-signals
serial IF	Serial Interface
parallel IF	Parallel Interface

Features

Analogue Input	➢ 3 channels: sine/cosine/reference signal ➢ Standard connection $1V_{pp}$ (differential) ➢ Input frequency of up to 400kHz
AD converter	➢ up to 1.25MS/s ➢ Single-Ended Input $2.4V_{pp}$
Signal correction	➢ Automatic gain and offset controller ➢ External potentiometer for analogue phase correction
Interpolation rates	➢ 200, 160, 100, 80, 50, 40, 25, 20
Measuring result outputs	➢ 28 - Bit counter ➢ 90° - square wave sequences ➢ Error signal
Configuration options	➢ Via configuration pins ➢ Via serial interface (SPI)
Serial interface (SPI)	➢ For Configuration and measuring value output ➢ 16-Bit synchronous/asynchronous mode ➢ Not required for low-cost minimal applications
Parallel output	➢ For measuring value output ➢ 16-Bit wide ➢ Up to 40MBit/s bandwidth
Miscellaneous	➢ Filter for suppressing edge noise at low speed input signals ➢ Programmable interval time for adapting the circuit to low speed digital components ➢ Two-level edge-controlled measuring trigger ➢ Programmable sensor error response
Package	➢ TQFP64 (10mm x 10mm x 1mm) or DIE

2 Input Signals

The two input signals for the interpolation function are analogue voltages (sine/cosine) with a sine-shaped dependency on the measured value (position or angle respectively) with a phase shift of 90° between these two analogue voltages, related to one period of the scale. A third input signal serves as a reference signal for determining the zero or reference point of the scale. All the three input signals are processed as differential signals.

2.1 Analogue Signal Properties

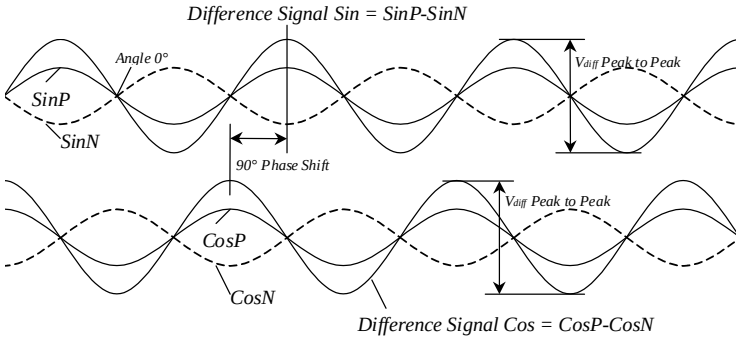


Figure 2

Differential Analogue Input Voltage[1)]	500mV$_{pp}$
Analogue Input Voltage V_{Diff} (nominal)	1V$_{pp}$
Input Range for V_{Diff}	0.8V$_{pp}$ ... 1.2V$_{pp}$
Maximum Signal Offset Error	±100mV
Sine/Cosine Phase Shift	90° (adjustable ±10°)

[1)] on pins `SINP, SINN, COSP, COSN`

2.2 Signal Correction

The input signals are subject to a automatic gain and offset control patented by GEMAC. The amplitude controller is specified for a control range of ±20% of nominal input voltage. The offset of the external signals must not exceed a value of ±10% of nominal input voltage. The phase shift of the input signals can be statically adjusted by a external analogue potentiometer in a range of ±10° (also refer to Application Notes 4300x-AN-3-0-E-IPx.pdf).

A Chip Reset results in setting the gain-offset-controller to midscale. For achieving the best interpolation performance, the gain-offset-controller needs approximately 20 signal periods for reaching a steady state. Until this time, the input signal frequency must not exceed 50% of the specified maximum signal frequency (refer to chapter 4.4).

All signal errors figures as a union in the IP200. In some special cases means decreasing of one signal error result in a wider permissible range of another signal error. For achieving the highest performance of the automatic gain-offset-controller, it is recommended to carefully adjust the phase shift on the connected sensor itself. This is important especially for high interpolation rates.

2.3 Reference Signals / Index Point

A third output of the measuring system - typically called reference, index point or zero point signal - considered to be activated, if the difference of the signals at the REFP and REFN pins becomes greater than the positive hysteresis voltage V_{RPH} and is considered to be deactivated if this voltage becomes smaller than the negative hysteresis voltage V_{RPL}.

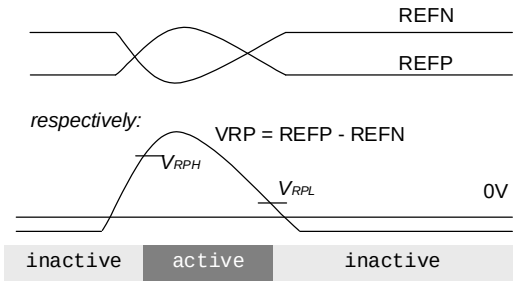


Figure 3

V_{RPL} (typical)	= -6mV
V_{RPH} (typical)	= +6mV
Hysteresis (typical)	= 12mV

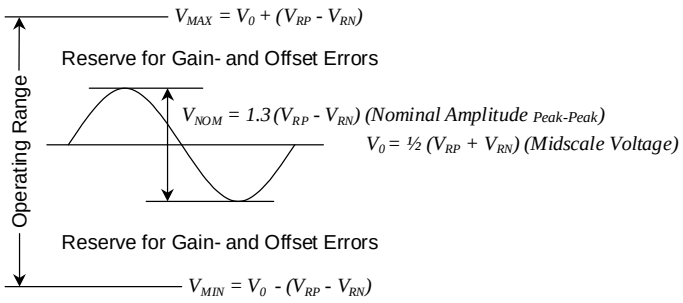
ⓘ

If a sensor without reference signals is used, defined levels on pins REFP and REFN are necessary to setting the index point always active or always inactive, respectively.

3 A/D-Converter

The IP200 contains two integrated Analogue Digital Converter with a maximum sample rate of 1.25MS/s. In some special applications, were the analogue sensor signal do not match the analogue front end (AFE) specification (nominal $1V_{pp}$), it is possible to connect the input signals to the Analogue Digital Converter inputs, bypassing the AFE. In this case, the conditioned sensor signals must be sine shaped with a amplitude of $2.4V_{pp}$ centred around the ADC common mode level V0. The IP200 includes a on-chip reference voltage circuit that generates the V0 with a nominal voltage of 2.375V.

3.1 Input Circuit Rating



V_{RP} : *positive ADC-Reference Voltage*
V_{RN} : *negative ADC-Reference Voltage*

Figure 4

The following reference voltage levels appear on external pins:

	Pin	Nominal Value
Positive Reference Voltage (V_{RP}) Sine-ADC	RSH	3.30V
Positive Reference Voltage (V_{RP}) Cosine-ADC	RCH	3.30V
Negative Reference Voltage (V_{RN}) Sine-ADC	RSL	1.45V
Negative Reference Voltage (V_{RN}) Cosine-ADC	RCL	1.45V
Midscale Voltage for external analogue circuitry	V0	2.375V
Nominal amplitude	U_{NOM}	2.405V
Maximum voltage	U_{MAX}	4.225V
Minimum voltage	U_{MIN}	0.525V

ⓘ
For information about the tolerances see chapter Electrical Characteristics.

4 Digital Operation Modes

4.1 Output Signals / Counter Value

The position/angle result is available via the integrated serial interface in a 28-bit two's-complement format. As described, the zero point can be generated using the REFP and REFN reference signal inputs, or it can be set via the serial interface. By activating the trigger input, measuring result can be kept in a 2-level deep buffer register in a manner asynchronous to the access via the interfaces.

Simultaneously, the IP200 outputs the phase shifted square wave sequences (known by incremental measuring transducers) which can be counted in single or quadruple way.

A synchronous reference pulse is generated when the angle of 0° (refer also to Fig. 2) is passed through and when the analogue differential input voltage between REFP and REFN exceed the positive comparator hysteresis level. If the differential input voltage is permanently above this level, the reference pulse is generated once during every signal period. A configuration bit can disable the generation of the reference pulse.

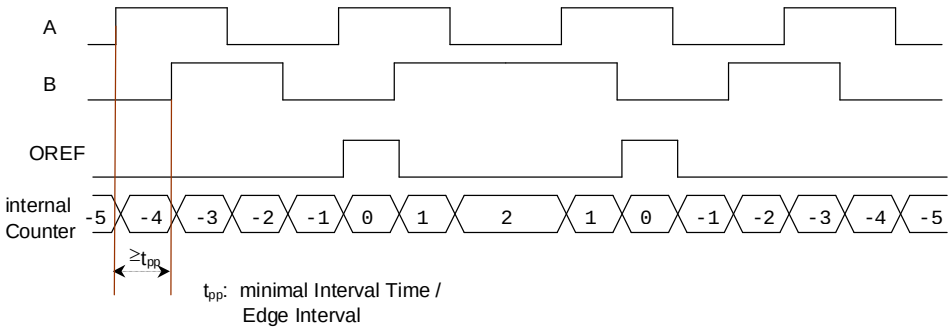


Figure 5

ⓘ

Note that the IP200 IC based on a digital interpolation method. This means that the quantization errors (the so-called ±1 errors) which are inevitable with A/D converters are superposed upon the speed-proportional A/B output signals. Analogue control systems must feature a corresponding low-pass behaviour when the IC is used in such systems.

4.2 Error Signal

An error signal is generated if the input signals are no longer plausible. The error signal is also generated if the input frequency is so high that the square-wave signals are unable to follow, and/or when the maximum input frequency is exceeded. The evaluation of the internal error sources is activated via an error mask register. The response of the square-wave outputs in the event of an error can also be configured via this register. The NERR and NRES pins can be connected in order to start a re-synchronisation process of the IC in the event of an error.

ⓘ
If the error signal was activated, and/or if one of the error bits was set in the result register, the present measuring result and all the following results must be discarded. Following elimination of the cause of the error and a reset of the error bit, the reference point must once again be passed by for absolute value measurements!

4.3 Interpolation Rate

The interpolation rate can be set at 200, 160, 100, 80, 50, 40, 25 and 20. The interpolation rate as defined for the purposes of this application is the number of increments into which one sine period of the input signal is divided. This also corresponds to the number of edge changes on the A/B output signals per input signal period. This means that the number of square-wave periods at the A and B outputs totals 1/4 of the interpolation rate per input signal period.

ⓘ
In the event that a standard interpolation counter or quadrature decoder is connected to the A/B outputs, this must work in "quadruple evaluation" mode in order to achieve the full interpolation rate.

4.4 Interval Time / Maximum Input Frequency

The interval time (IT) and the minimum edge distance t_{pp} at the output signals, respectively, can be set in binary steps at values between $1/f_{osz}$ and $128/f_{osz}$.

In counter mode (the SPEED Bit in the CFG0 Register being set), the maximum input frequency totals $f_{max}=f_{osc}/96$. In all the other modes, the maximum input frequency is limited by the minimum pulse distance at the output, where:

$$f_{max} \approx 0.9*f_{OSZ}/(IR \cdot IT) < f_{osz}/96$$

f_{osc}: Clock frequency at Pin XA
IR: Activated Interpolation Rate
IT: Activated Interval Time

The limit values are a maximum input frequency of aprox. 400kHz with a clock frequency of 40MHz on the one hand, as well as a guaranteed edge distance of 128µs at the A/B signals with a clock frequency of 1MHz on the other. Between these two limits, a large number of specific systems can be adapted by selecting a suitable clock frequency and interval time of the IP200.

ⓘ
These values apply on condition of an adjusted phase between the input signals and a steady state of the internal gain-offset-controller. Until this time, the input frequency must not exceed 50% of the specified maximum frequency.

Clock Frequency Examples

f_{OSC} = 40MHz f_{maxCNT} = 400kHz															
IR	IT	t_{pp}	f_{max}	IR	IT	t_{pp}	f_{max}	IR	IT	t_{pp}	f_{max}	IR	IT	t_{pp}	f_{max}
200	1	31ns	180k	160	1	31ns	225k	100	1	31ns	360k	80	1	31ns	400k
	2	62ns	90k		2	62ns	113k		2	62ns	180k		2	62ns	225k
	4	125ns	45k		4	125ns	56k		4	125ns	90k		4	125ns	113k
	8	250ns	22.5k		8	250ns	28k		8	250ns	45k		8	250ns	56k
	16	500ns	11.3k		16	500ns	14k		16	500ns	22.5k		16	500ns	28k
	32	1µs	5.6k		32	1µs	7k		32	1µs	11.3k		32	1µs	14k
	64	2µs	2.8k		64	2µs	3.5k		64	2µs	5.6k		64	2µs	7k
	128	4µs	1.4k		128	4µs	1.8k		128	4µs	2.8k		128	4µs	3.5k
50	1	31ns	400k	40	1	31ns	400k	25	1	31ns	400k	20	1	31ns	400k
	2	62ns	360k		2	62ns	400k		2	62ns	400k		2	62ns	400k
	4	125ns	180k		4	125ns	225k		4	125ns	360k		4	125ns	400k
	8	250ns	90k		8	250ns	113k		8	250ns	180k		8	250ns	225k
	16	500ns	45k		16	500ns	56k		16	500ns	90k		16	500ns	113k
	32	1µs	22.5k		32	1µs	28k		32	1µs	45k		32	1µs	56k
	64	2µs	11.3k		64	2µs	14k		64	2µs	22.5k		64	2µs	28k
	128	4µs	5.6k		128	4µs	7k		128	4µs	11.3k		128	4µs	14k

	marked cells:	Error FAST1 appears on speed overflow
	normal cells:	Error FAST2 appears on speed overflow

4.5 Glitch Filter

In order to avoid permanent toggling of the downstream counters as a result of analogue noise of the input signals while the measuring system is in standstill, a digital filter can be optionally activated for the square-wave outputs (pin / bit GFE). In such a case, the minimum edge distance at the output (t_{pp}) is then automatically set at 2048 / f_{osc} while the measuring system is in standstill or at smaller input frequencies.

ⓘ
Note that in the switching range to the automatic activation / deactivation of this filter, the A/B output signals are not speed-proportional in each case!

5 Interfaces

The measurement results can be read out over the integrated serial interface (SPI). It is also possible to make a more detailed configuration of the IP200 IC over this interface than over hardware. For high speed applications the additional 16-bit wide parallel port allow to read out the measurement results continuously with up to 32MBit/s.

5.1 Structure

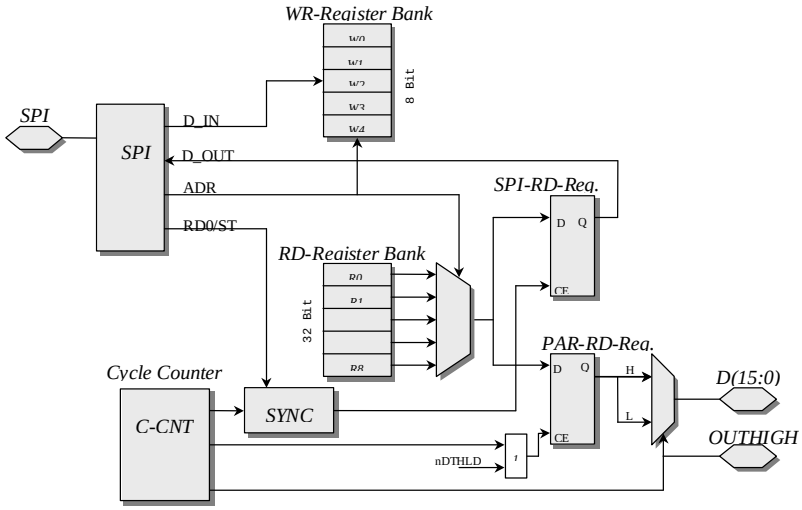


Figure 6

5.2 Serial Interface (SPI)

The serial interface contains a 16-bit shift register for read accesses and write accesses each. An additional 16-bit hold register series for the intermediate storage of the two MSB's during read accesses. An 8-bit address register is used for both read and write accesses. Writing into the IP200 takes place in a byte-oriented manner whilst reading being a word-oriented process. Transmission itself is effected as 16-bit words. A read command triggers the pertinent data output during the next access. A single-byte command is executed at the end of data transmission. Up to 16 channels can be operated at this interface. The hardware address of the IC is determined by reading the `DP(3:0)` pins by a special command.

5.2.1 Signals

The IP200 is a slave which evaluates commands and data received, but which is unable to start a communication process. The SPI protocol is executed via 4 lines:

`SDI`	Data input
`SDO`	Data output (open drain), `SDO` also serving as the `RDY` signal
`SCLK`	Clock
`SEN`	Enable

ⓘ
The used SPI-protocol is not compatible to the usual micro controller- or DSP-families.

Each transfer process is triggered by the sending of a command. To this effect, SEN is kept low during 16 SCLK clock cycles. The input data at SDI is evaluated a the rising edge of SCLK. At the same time, the shifting of the data of the hold register is triggered at every rising edge at SCLK.

SPI-Access:

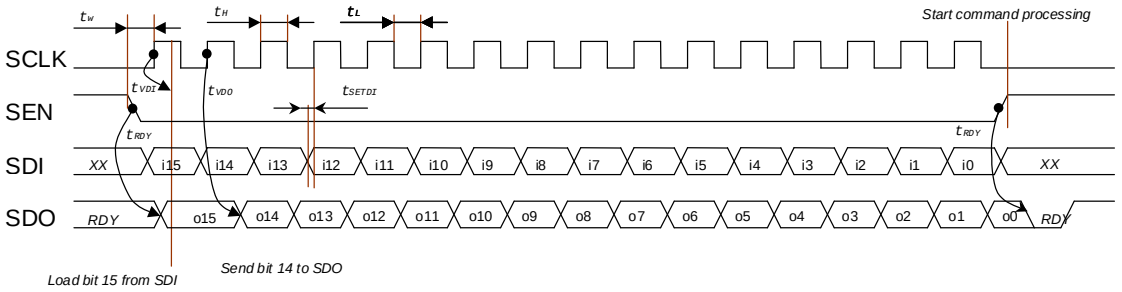


Figure 7

Name	Min	Max	Description
t_H	2 x T_{OSZ} + 15 ns[1)]		SPI clock, H time
t_L	2 x T_{OSZ} + 15 ns[1)]		SPI clock, L time
t_w	1 x T_{OSZ} + 15 ns[1)]		Waiting time between SEN falling and SCLK rising
t_{RDY}	3 x T_{OSZ} + 15 ns	4 x T_{OSZ} + 15 ns	Switching delay RDY / SDO from SEN
t_{VDI}		15 ns	Time between SCLK rising and data read
t_{SETDI}	1 x T_{OSZ} + 15 ns[1)]		Setup time SDI before SCLK
t_{VDO}	4 T_{OSZ} + 15 ns	5 T_{OSZ} + 15 ns	Time between SCLK rising and data output

5.2.2 Protocol

Bit No. at signal SDI																Name	Description
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	RES	Reserved
0	nB[2)]	0	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	A7	A6	A5	A4	A3	A2	A1	A0	WRA	Write Address
0	nB[2)]	1	0	H3[2)]	H2[2)]	H1[2)]	H0[2)]	D7	D6	D5	D4	D3	D2	D1	D0	WRD	Write Data
0	nB[2)]	1	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	C7	C6	C5	C4	C3	C2	C1	C0	WRC	Write Command
1	nB[2)]	0	0	H3[2)]	H2[2)]	H1[2)]	H0[2)]	A7	A6	A5	A4	A3	A2	A1	A0	RD0/ST	Read Byte 0 + 1 (LSB) [1)]
1	nB[2)]	0	1	H3[2)]	H2[2)]	H1[2)]	H0[2)]	X	X	X	X	X	X	X	X	RD1	Read Byte 2 + 3 (MSB)
1	nB[2)]	1	X	H3[2)]	H2[2)]	H1[2)]	H0[2)]	X	X	X	X	X	X	X	X	NOP	Output Read-Register

[1)] command load the internal data into a 32-bit hold register
[2)] bit must be set to zero in single-channel systems

Bit	Name	Description
nB	Broadcast mode (Low-active)	0: Command to all channels (for WRA/WRD/WRC only) 1: Command to the channel addressed by H(3:0)
H(3:0)	Hardware address	IP200-Channel address for single access (nB=1) Default: 0x00
A(7:0)	Register address	IP200-Register address
C(7:0)	Command	Single-word command
D(7:0)	Data word	Write data (readed data appears at SDO)

Command word examples

Set address register in all channels connected at 0x01:	0x1001
Write data 0x48 in channel 0x04:	0x6448
Read L word from register 0x07, one IC existing only:	0x8007
Configuration of the hardware address in all the channels connected:	0x3000

5.2.3 Synchronous / Asynchronous Mode

Read data is loaded into the hold register by the RD0/ST command. This takes place when the internal sequential control counter and the SYNC register have the same contents (synchronous mode) or when the ASYNC bit is set (asynchronous mode). Pin SDO is low during the waiting time (meaning of RDY) .

With the SPI working in synchronous mode, the output data can be assigned to a sample time. Equidistant measurement is possible (refer also to the application example). Higher transmission rates are achieved in asynchronous mode.

Example: 32-bit read access synchronous with internal cycle counter

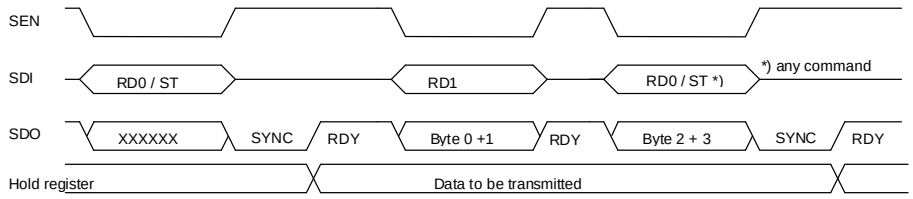


Figure 8

Example: 16-bit read access, asynchronous, 3 channels

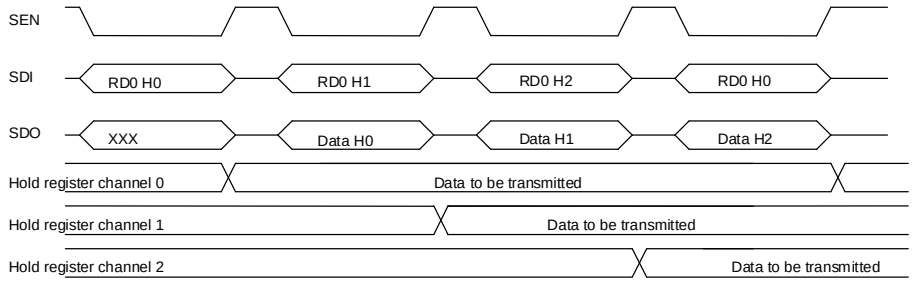


Figure 9

Example: write access 1 Channel

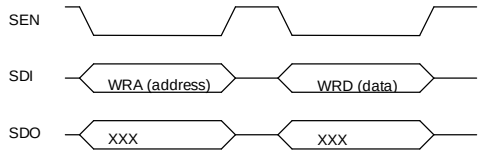


Figure 10

Example: command execution 1 channel

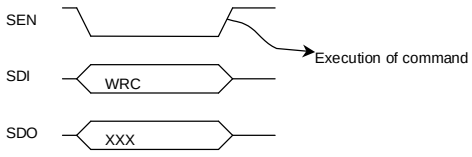


Figure 11

5.3 Parallel Data Port

This interface outputs the last activated SPI read register synchronized to the IP200 internal sequential control counter. The appearing data are separated into two 16-bit words. After reset, the data of the SPI read register address 0x00**`(MVAL)`appears on `DATA(15:0)` by default**.

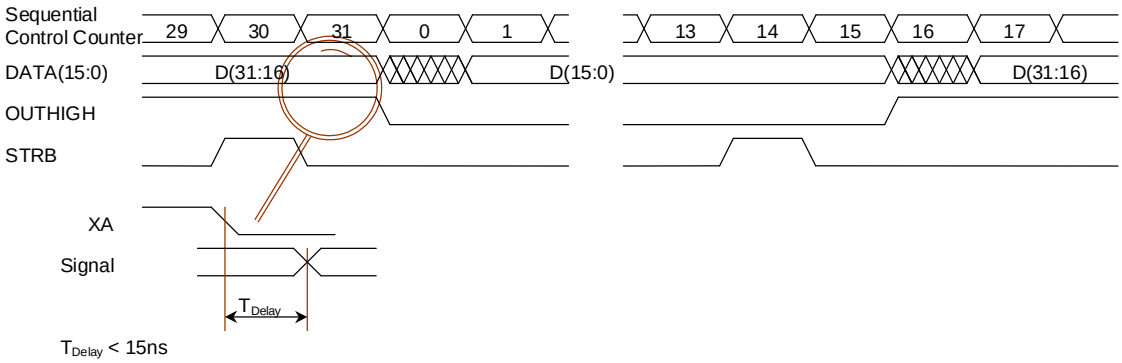


Figure 12

To reduce switching noise on the data port the Data outputs `DATA(15:8)` will be switched 1 clock cycle after the outputs `DATA(7:0)`. That's why the value at `DATA(15:8)` is undefined in the clock cycles 0 and 16. For external components the edges of `OUTHIGH` can be used to register the new valid data. The level on `OUTHIGH` show, which part of the 32-bit read value is active on the data pins (either LSB or MSB). A optional Strobe-Signal (on pin `OREF`) can be activated via `TSTRB` bit in the configuration register `TSTCFG`.

ⓘ
To get out a desired read register on parallel port, it is necessary to read this register via serial interface first. EVERY other SPI access at any time can change the behaviour of parallel port.
If the parallel interface be used solely as output port, please select carefully the corresponding attachment circuit of the configuration and the double function pins at the IP200. Please refer also application notes in the document 4300x-AN-3-0-E-IPx.pdf.

6 Registers

The IP200 contains 16-bit and 32-bit read registers, as well as 8-bit write registers. The addresses are assigned separately for the read and write registers. A third address space is reserved for commands.

6.1 Read Registers

Address	*Description*	*Byte 3*	*Byte 2*	*Byte 1*	*Byte 0*
0x00	Measurement Value / Status	MVAL			
0x01	Configuration / Status	ERRMASK	CFG1	CFG0	STAT
0x03	Interpolation results	DPHI		PHI	
0x04	Controller Sine			SOFF	SGAIN
0x05	Controller Cosine			COFF	CGAIN
0x07	Counter Value / Status	CNT			

6.2 Write Registers

Address	*Description*	*Name*
0x00	Configuration	CFG0
0x01	Configuration	CFG1
0x02	Configuration	ERRMASK
0x03	SPI-Synchronisation	SYNC
0x04	Configuration IC-Test	TSTCFG
0x07	Controller Sinus (Gain)	SGAIN
0x08	Controller Sinus (Offset)	SOFF
0x09	Controller Cosine (Gain)	CGAIN
0x0A	Controller Cosine (Offset)	COFF

6.3 Commands

Command	Name	Description
0x00	Channel	The hardware address will be read from pins DP(3:0). Send this command always as broadcast command! *In multi-channel systems this command must send and executed first after a global reset!*
0x01	Reset Counter	The parallel counter (register CNT) is reset, the error register is reset. Note, that the values of trigger hold registers remains unchanged.
0x02	Reset Controller	The gain-offset-controller will be set to midscale.

6.4 Coding

MVAL *Measurement Value / Status*

Read Address 0x00
Default 0x00

31:4	3	2	1	0
CNT	FAST1	SENSERR	TRGOVL	FROZEN

CNT Counter Value or Trigger Value respectively (28-bit - two's complement)
FAST1 Speed Error
SENSERR Sensor Error (ADC overflow, sensor breakage, gain- or offset error)
TRGOVL Trigger Overflow
FROZEN 0 CNT contains the current counter value
1 CNT contains the oldest trigger value stored

ⓘ
For more detailed information about the functions of these bits refer to chapter 7 and 8.

Examples:

0x00004200	Result 0x00000420 is current counter value
0x00004201	Result 0x00000420 is trigger value, no errors
0x00004203	Result 0x00000420 is trigger value, one or more trigger events are lost
0x00004204	Sensor error, Result invalid
0x00004205	Sensor error, Result invalid

CNT *Counter Value / Status*

Read Address 0x07
Default 0x00

31:4	3	2	1	0
CNT	GCOMP	OCOMP	AMPERR	FAST1

CNT Counter Value (28-bit - two's complement)
FAST1 Speed Error
AMPERR Sensor Error (ADC overflow or sensor breakage)
OCOMP Offset Error
GCOMP Gain Error

ⓘ
For more detailed information about the functions of these bits refer to chapter 7 and 8.

STAT *Status*

Read Address 0x01 (Byte 0)
Default 0x00

7:6	5	4	3	2	1	0
TR(1:0)	Fast2	Fast1	ADCOVL	BQLO	OCOMP	GCOMP

GCOMP Gain Error
OCOMP Offset Error
BQLOW Sensor Breakage
ADCOVL ADC Overflow
FAST1 Speed Error (Counter and A/B-Signals)
FAST2 Speed Error (A/B-Signals)
TR(1:0) Status of Trigger-Hold-Registers

ⓘ
For more detailed information about the functions of these bits refer to chapter 7 and 8.

PHI *Interpolation Result - Phase Angle*

Read Address 0x03 (Byte 1/0)

15:8	7:0
0x00	PHI

PHI Interpolated Phase Angle of Input Signals (unsigned, binary)

Scaling: 0 ... 200 = 0°... 360°, if IR(2) = 1

0 ... 160 = 0°... 360°, if IR(2) = 0

DPHI *Interpolation Result - Phase Angle Difference*

Read Address 0x03 (Byte 3/2)

15:8	7:0
0x00	DPHI

DPHI Difference to last Phase Angle (two's complement)

Scaling: -100 ... +100 = -180°... +180°, if IR(2) = 1

-80 ... +80 = -180°... +180°, if IR(2) = 0

CFG0 *Configuration Register 0*

Read Address 0x01 (Byte 1)

Write Address 0x00

Default Configuration pins will be read (IT0=0)

7	6	5:3	2:0
SPEED	GFE	IT(2:0)	IR(2:0)

IR(2:0)	Interpolation Rate	Square Wave Periods A/B
000	160	40
001	80	20
010	40	10
011	20	5
100	200	50
101	100	25
110	50	12½
111	25	6¼

IT(2:0)	Interval Time t_{pp} in 1/ f_{OSZ}
000	1
001 *)	2
010	4
011 *)	8
100	16
101 *)	32
110	64
111 *)	128

*) only selectable over SPI

GFE 0 Glitch Filter deactivated

1 Glitch Filter activated

SPEED 0 Configure speed monitoring for A/B outputs

1 Configure speed monitoring for internal counter

ⓘ

The double function pins SDI and TRG are used for initializing of the GFE and SPEED bits during reset processing. The IT0 bit can only be assigned over serial interface. For more information refere also to IP200 application notes.

CFG1 *Configuration Register 1*

Read Address 0x01 (Byte 2)
Write Address 0x01
Default 0x00

7:3	2	1	0
00000*)	DISREG	DISREF	TRSLP

*) *Bits must remain unchanged in order to guarantee the correct functioning of the IC*

DISREG 0 Internal automatic gain-offset-controller activated
1 Internal automatic gain-offset-controller deactivated

TRSLP 0 Trigger event occurs on the falling edge of pin TRG
1 Trigger event occurs on the rising edge of pin TRG

DISREF 0 Reference point processing activated
1 Reference point processing deactivated

ERRMASK *Error Mask Register*

Read Address 0x01 (Byte 3)
Write Address 0x02
Default 0x3F

7	6	5	4	3	2	1	0
Latch	Hold	Fast2	Fast1	ADCOVL	BQLO	OCOMP	GCOMP

GCOMP Enable Gain Error Detection
OCOMP Enable Offset Error Detection
BQLOW Enable Sensor Breakage Detection
ADCOVL Enable ADC Clipping Detection
FAST1 Enable Speed monitoring (Counter and A/B-Signals)
FAST2 Enable Speed monitoring (A/B-Signals)
HOLD Deactivate square-wave outputs in event of an error
LATCH Store error states

For detailed Information about the meaning of the bits refere to chapter 8.

ⓘ
For square wave operation (A/B-Signals) it is recommended to set the error mask register to 0x3F or 0xFF respectively, in counter mode use the error mask register loaded with 0xDF and set the SPEED bit in the CFG0 register.

SYNC *SPI-Synchronization Register*

Write Address 0x03
Default 0x00

7	6	5	4:0
ASYNC	0	0	SYNCVAL

ASYNC 0 Import read data with SPI-RD0/ST the next time the contents of the cycle counter and SYNCVAL are identical
1 Import read data always with SPI-RD0/ST

SYNCVAL Sequential control counter compare value for SPI synchronization

For more detailed information about the functions of these bits refer to chapter 5.2.3

TSTCFG *Configuration IC-Test*

Write Address 0x04

Default 0x00

7:3	2	1:0
00000*)	TSTRB	00*)

*) *Bits must remain unchanged in order to guarantee the correct functioning of the IC*

TSTRB
- 0 Configure pin OREF as index point output
- 1 Configure pin OREF as Strobe-Signal for the parallel Interface

SGAIN *Gain Correction Value, Sine*

CGAIN *Gain Correction Value, Cosine*

Read Address 0x04 / 0x05 (Byte 0)

Write Address 0x07 / 0x09

Default 0x80

7:0
GAIN

GAIN Current value of the gain correction registers (unsigned, binary)

Scaling:

0x00	Factor 0.5
0x80	Factor 1
0xFF	Factor 1.5

SOFF *Offset Correction Value, Sine*

COFF *Offset Correction Value, Cosine*

Read Address 0x04 / 0x05 (Byte 1)

Write Address 0x08 / 0x0A

Default 0x00

7:0
OFFSET

OFFSET Current value of the offset correction registers (two's complement)

Scaling:

0x80	Maximum Offset negative (-25% ADC Maximum)
0x00	No Offset
0x7F	Maximum Offset positive (+25% ADC Maximum)

ⓘ

Write accesses to the SOFF/COFF/SGAIN/CGAIN register serve for pre-setting - these registers are permanently updated by the internal automatic gain-offset-controller.
The scaling factor indicated applies to the behaviour of the adjustment register; it does not describe the maximum signal error possible.

7 Measurement Trigger

A signal edge event on pin TRG/GFE stores the current measurement result (counter value) in one of the two-level deep trigger hold register. The active trigger edge is configured by the configuration bit TRGSLP (register CFG1).

A read access to the register MVAL returns the “oldest” value of the trigger hold register. If the trigger register contains no active value, the current counter value returns in result of the read access. It is possible to save the results of two trigger events. While not **both** trigger register would be read out, all following trigger events are ignored. The TRGOVL bit in register MVAL is set, if a trigger event occurs and both trigger hold register contains valid data.

Every SPI read access to the register MVAL releases one trigger hold register. Only if trigger hold register 1 is empty (TR1=0), a new trigger processing is possible. If the parallel interface used solely as output port, the pin CLRTRG must be operated to confirm the reading of one trigger event result.

A logic “1” in the FROZEN bit out of the register MVAL indicates the source of the read value as trigger result. A logic “0” in this bit indicates the read access as normal read of the counter value. The actual state of the trigger is coded in the bits TR(1:0)of the status register (STAT).

TR(1:0)	TRGOVL	FROZEN	MVAL contents	next Trigger Event
00	0	0	Current counter value	Storing to Trigger Hold Register 0
01	0	1	Trigger Hold Register 0	Storing to Trigger Hold Register 1
10	0	1	Trigger Hold Register 1	Storing disabled, TRGOVL will be set
11	0	1	Trigger Hold Register 0	Storing disabled, TRGOVL will be set
10	1	1	Trigger Hold Register 1	Storing disabled, TRGOVL is set
11	1	1	Trigger Hold Register 0	Storing disabled, TRGOVL is set

ⓘ
For applications which need fast response time related to trigger events and a high data rate on the serial port as well , it could be better to read out only the 16 LSB of the MVAL register to check out if a trigger event occurred.

8 Error Processing

The IP200 has 6 sources for generating the global error signal. Each source can be activated by the corresponding bit in the error mask register. With the LatchErr bit being activated, the individual error signals are stored until the next chip reset or until the next SPI ResetCount command (command 0x01) occurs, respectively. The logic OR function of the masked and stored error signals appears as a low active signal on pin NERR. With the HoldErr bit being active, the A, B and OREF outputs freeze in the current state on error case. The NERR and NRES pins can be shorted in order to re-synchronise the IC in the event of an error. The error signal is active for 8 system clocks in this case.

Error Mask Register

Bit	Description (if bit is set)
GCOMP	Gain controller reaches his limit
OCOMP	Offset controller reaches his limit
BQLOW	Amplitude Error: the resulting Sine-Cosine-Vector is to small
ADUOVL	One or both ADC-Converter are clipping
FAST1	Signal frequency to high, no signal direction recognition possible (SPEED=1), Signal frequency to fast for proper generating A/B/OREF - Signals (SPEED=0)
FAST2	Signal frequency to fast for proper generating the A/B/OREF - Signals (depends upon IT(2:0), refer also to table “Clock Frequency Examples” in chapter 4.4)
HoldErr	The A/B/OREF - Signals freeze in error case
LatchErr	The masked error signal is stored until next SPI-reset-command or a global reset occurs, respectively

ⓘ
For square wave operation (A/B-Signals) it is recommended to set the error mask register to 0x3F or 0xFF respectively, in counter mode use the error mask register loaded with 0xDF and set the SPEED bit in the CFG0 register.

The status register STAT contains all error bits. The MVAL and CNT register contain logic combinations of counter relevant error bits:

```
SENSERR = ADUOVL or BQLOW or OCOMP or GCOMP
AMPERR = ADUOVL or BQLOW
```

Sensor breakage error:

Partial or complete tearing off of the connected sensor is detected in the IP200 *at the time of occurrence*. Thereafter, the automatic gain-offset-controller tries to compensate this error which, due to the large operating range of the gain-offset-controller, can lead to a situation where the cause of this error seems to have been eliminated.

9 Reset / Configuration

The IP200 IC **does not contain** an **internal Power-On-Reset circuit!** It is **essential** to supply the IP200 with an external reset signal on pin NRES. This reset signal must appear low until 3ms after VDD rising to a voltage level of 4.75V.

If NRES and NERR are shorted, the error signal is held through the "NERR -chain" while one of the chain flip-flops contains a "0".

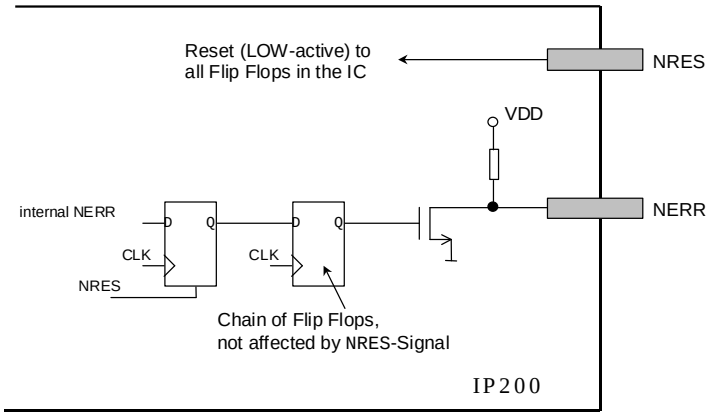


Figure 13

9.1 Reset Processing

1. Pin SDO/RDY goes to L, all register will be initialised with default values.
2. The IC is operating a self-calibration, the configuration pins are read into the CFG0 register.
3. Start of normal operation.
4. Pin SDO/RDY goes to H (external pull-up required).
5. The configuration register could be changed via SPI interface.

The time between the rising edge of NRES and the rising edge of SDO/RDY, which means the end of the reset process, amount to approximately 1365 system clocks.

9.2 Configuration

There are two different types of configuration possible:

Configuration via input pins

- The register CFG0 will be configured via the input pins IR(2:0), IT(2:1), TRG/GFE and SDI/SPEED.
- All other registers are initialised with default values.
- Suitable for low-cost single-chip and standard applications.

Configuration via SPI

- Pins DP(3:0) select SPI hardware address (for multi-channel systems only).
- Suitable for applications with SPI interface, for example microcontroller systems.

9.3 Configuration Bits Defaults

Name	*Description*	*Default*
IR(2:0)	Interpolation Rate	Pin IR(2:0)is read
IT(2:1)	Interval Time	Pin IT(2:1)is read
IT(0)	Interval Time	0
GFE	Glitch-Filter-Enable	Pin TRG/GFE is read
SPEED	Speed-Mode for internal Counter	Pin SDI/SPEED is read
DISREG	Disable automatic controller	0
DISREF	Disable Index Point	0
TRSLP	Trigger Edge	0
TSTSTRB	Enable Strobe-Signal on pin OREF	0
ERRMASK	Error Mask Register	0x3F
SGAIN	Initial value Gain Correction, Sine	0x80
SOFF	Initial value Offset Correction, Sine	0x00
CGAIN	Initial value Gain Correction, Cosine	0x80
COFF	Initial value Offset Correction, Cosine	0x00
SYNC	SPI synchronisation with internal sequential control counter	0x00

10 Signal Propagation Time

The delay time between the sampling point of the analogue input signals (sine/cosine) and the availability of the interpolation result (i.e. related to trigger) totals 90 system clocks. The delay time between sampling and updating the data registers and those values available via parallel or serial interface, respectively, totals 96 system clocks. If a external counter unit connected to the A/B/OREF outputs is used, the time between sampling and output of resulting square waves totals 122 system clocks.
Every 32nd system clock a new measurement result appears on the parallel data output. Note that the data transferring time of the used interface is added to the IP200 internal system propagation time.

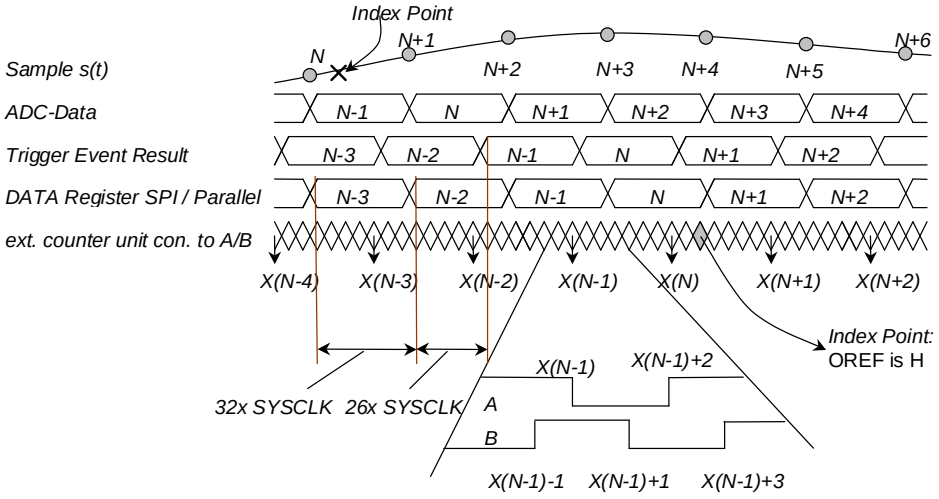


Figure 14

ⓘ
Note that the constant delay time of the IC (as with any other digital signal processing systems) result in a frequency-dependent phase shift between the analogue input signals and the output signals ($d\varphi = 2\pi \cdot f \cdot t_v$).

11 Electrical Characteristics

Absolute maximum ratings	*Min.*	*TYP*	*Max*	*Unit*
Power supply VDD	0.3		7	V
Temperature*)	-55		125	°C
storage temperature	-55		155	°C
ESD			1	kV

*) with defined circuit

Crossing these ratings can damage the IC; events of maximum supply voltage and maximum temperature at the same time have been to avoid.

Recommended Operating Conditions	*MIN*	*NOM*	*MAX*	*Unit*
Supply voltages (VDD, VDDA) with respect to Ground (VSS)	4.75	5.0	5.25	V
Supply current analogue (@20°C)	10	20	35	mA
Supply current digital (@20MHz & 20°C)		40		mA
System clock pulse duration time Low / High	12.5*)		500	ns
System clock frequency range f_{osc}	1		40*)	MHz
Operating case temperature	-20		85	°C
Digital input and output voltage V_IL	0		0.3 x VDD	V
Digital input and output voltage V_IH	0.7 x VDD		VDD	V
Digital input and output voltage V_OL***)	0		0.8	V
Digital input and output voltage V_OH***)	2		VDD	V
Crystal**) connected to XA and XB:				
Internal load capacitance (XA, XB)		6		pF
Power-On-Time			3	ms

*) Note that the system clock pulse duration time does not remain under minimum throughout the entire temperature range, if a crystal is used.

**) The IP200 circuit is intended for series resonant fundamental mode operation.

***) I_out max. 4mA

Interpolation	*MIN*	*NOM*	*MAX*	*Unit*
Input frequency range	0		f_{osz} / 96	kHz
Automatic gain control range		±20%		related to nom. amplitude
Automatic offset control range		±10%		
Interpolation Rates	20 / 25 / 40 / 50 / 80 / 100 / 160 / 200			
Minimum interval time A/B - Signals	1 / f_{osz}		128 / f_{osz}	ns
Interpolation accuracy @ I-Rate = 200, f< 100kHz		±0.7	±1.2	Inc.
Interpolation accuracy @ I-Rate = 200, 250kHz <f		±2		Inc.
Propagation delay counter		90 / f_{osc}		ns
Propagation delay square-wave outputs (A/B/0REF)		122 / f_{osc}		ns
Reference pulse position related to Sin		0°		
Data Rate parallel interface (DWORDS, 32 Bit)		f_{osc} / 32		MHz
Pulse width at TRG / CLRTRG	4 / f_{osc} + 15			ns
time constant glitch filter		2048/ f_{osc}		ns

Analogue Input Specifications	*MIN*	*NOM*	*MAX*	*Unit*
Input voltage range analog pins*)	0		VDD-1.2	V
Input current analog pins*)			<1	µA
Input impedance analog pins*)		6pF||1GΩ		
Input frequency range SIINP,SINN,COSP,COSN (< 1dB attenuation)			400	kHz
Phase offset between SIN and COS @100kHz			0.5	°
Peak to peak input voltage SINN ⇔ SINP / COSN ⇔ COSP	0.8	1.0	1.2	V_{pp}
Common Mode Level SINN ⇔ SINP / COSN ⇔ COSP	1.5	V_{CC} / 2	V_{CC} - 1.5V	V
CMRR (< 5Hz)	66			dB
PSRR (< 5Hz)	66			dB
Input Impedance		1GΩ||8pF		
Load capacitance at OUTS/OUTC @ R_S = 510Ω			1	nF
Load capacitance at OUTS/OUTC @ R_S > 2kΩ			10	µF
Source current at V0	-100		100	µA
Phase deviation	±10.5	±11.3	±12	°
Switching voltage of index point comparator	-6	0	6	mV
Hysteresis of index point comparator	8	12	20	mV

*) at the pins SINP, SINN, COSP, COSN, REFP, REFN, INPS and INPC

ADC	MIN	NOM	MAX	Unit
Input Impedance		100MΩ||20pF		
Mid voltage usable for external circuits	2.325	2.375	2.425	V
positive Reference voltage sine-ADC RSH	3.22	3.3	3.42	V
positive Reference voltage cosine-ADC RCH	3.22	3.3	3.42	V
negative Reference voltage sine-ADC RSL	1.39	1.45	1.53	V
negative Reference voltage cosine-ADC RCL	1.39	1.45	1.53	V
Signal amplitude in case of direct connection to the ADC		2.4		V_{PP}

12 Mechanical Characteristics

12.1 Pinout

Pin	Name	Type	Description	Pin	Name	Type	Description
1	DATA(0)	COUT	Data Output Port	33	SINP	AIN	Positive Signal Input Sine
2	DATA(1)	COUT	Data Output Port	34	SINN	AIN	Negative Signal Input Sine [5]
3	DATA(2)	COUT	Data Output Port	35	OUTS180	AOUT	Sine Analogue Output (Phase rev.)
4	DATA(3)	COUT	Data Output Port	36	OUTS	AOUT	Sine Analogue Output
5	DATA(4)	COUT	Data Output Port	37	INPS	AIN	ADC Input Sine
6	DATA(5)	COUT	Data Output Port	38	RSH	AIO	Pos. Reference Voltage SADC
7	DATA(6)	COUT	Data Output Port	39	RSL	AIO	Neg. Reference Voltage SADC
8	DATA(7)	COUT	Data Output Port	40	V0	AIO	Analogue Midscale Voltage
9	DATA(8)	COUT	Data Output Port	41	VSSA2	ASUP	Analogue Ground
10	DATA(9)	COUT	Data Output Port	42	VDDA2	ASUP	Analogue Supply
11	DATA(10)	COUT	Data Output Port	43	RCL	AIO	Neg. Reference Voltage CADC
12	DATA(11)	COUT	Data Output Port	44	RCH	AIO	Pos. Reference Voltage CADC
13	DATA(12)	COUT	Data Output Port	45	INPC	AIN	ADC Input Cosine
14	DATA(13)	COUT	Data Output Port	46	OUTC	AOUT	Cosine Analogue Output
15	DATA(14)	COUT	Data Output Port	47	COSN	AIN	Negative Signal Input Cosine [5]
16	DATA(15)	COUT	Data Output Port	48	COSP	AIN	Positive Signal Input Cosine
17	VSS2	DSUP	Digital Ground	49	PH	AIN	Analogue Phase Correction Input [5]
18	VDD2	DSUP	Digital Supply	50	VDDA3	ASUP	Analogue Supply
19	OUTHIGH	COUT	MSB at Parallel Data Port active	51	VSSA3	ASUP	Analogue Ground
20	CLRTRG	TTLIN	Clear Trigger [1]	52	IT2	TTLIN	Interval Time Select 3 [3]
21	XB	OSC	Crystal Input B [1]	53	IT1 / DP3	TTLIN	IT Select 1 / DProg 3 [3]
22	XA	OSC	Crystal Input B / ext. Clock	54	IR2 / DP2	TTLIN	Interpolation Rate / DProg 2 [3]
23	SCLK	TTLIN	SPI Clock [3]	55	IR1 / DP1	TTLIN	Interpolation Rate / DProg 1 [3]
24	SCEN	TTLIN	SPI Enable [2]	56	IR0 / DP0	TTLIN	Interpolation Rate / DProg 0 [3]
25	SDI / SPEED	TTLIN	SPI Data Input/ SPEED (Cfg) [1]	57	OREF	COUT	Index Point Output Signal
26	SDO/RDY	CODO	SPI Data Output [4]	58	B	COUT	Square Wave Output B
27	VDD3	DSUP	Digital Supply	59	A	COUT	Square Wave Output A
28	TM	TTLIN	Test Mode Input [1]	60	TRG/GFE	TTLIN	Trigger / Glitch-Filter-Enable [3]
29	VSSA1	ASUP	Analogue Ground	61	NERR	ODPU	Error Output
30	VDDA1	ASUP	Analogue Supply	62	NRES	TTLIN	Reset
31	REFN	AIN	Negative Reference Input [6]	63	VDD1	DSUP	Digital Supply
32	REFP	AIN	Positive Reference Input [6]	64	VSS1	DSUP	Digital Ground

COUT	CMOS - OUT 4mA	OSC	Oscillator - I/O, 6pF
CODO	CMOS - OUT 4mA / Open-Drain	AIN / AOUT / AIO	Analogue-IO
ODPU	CMOS - OUT 4mA / Open-Drain /w Pull Up	DSUP	Digital Power Supply
ODPD	CMOS - OUT 4mA / Open-Drain /w Pull Down	ASUP	Analogue Power Supply
TTLIN	Input, TTL - Level		

[1] if unused, pull Low
[2] if unused, pull High
[3] if unused, pull Low or High
[4] if unused, connect to separate pull up resistor
[5] if unused connect to V0
[6] if unused, pull the REFP and REFN inputs to different analogue voltage levels. The absolute voltage difference between these pins must exceed the maximum reference comparator input hysteresis range for a comparator safety behaviour

ⓘ
Each IC input pin requires a defined connection!

12.2 Double Function Pins

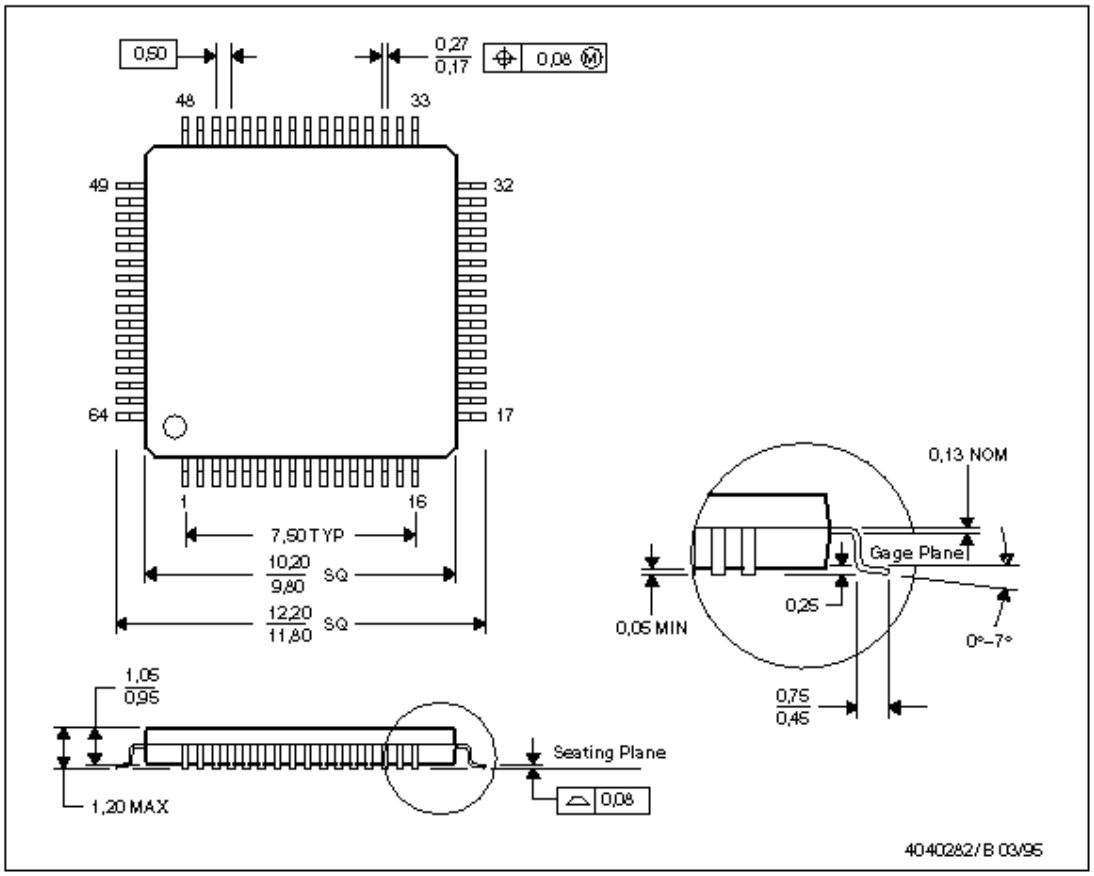
During reset process (the time between rising edge at NRES input and rising edge at SDO/RDY output) the following pins are required for IC configuration:

Name	During Reset	After Reset
IT1 / DP3	Interval Time	SPI Hardware Address (Initial value)
IR2 / DP2	Interpolation Rate	SPI Hardware Address (Initial value)
IR1 / DP1	Interpolation Rate	SPI Hardware Address (Initial value)
IR0 / DP0	Interpolation Rate	SPI Hardware Address (Initial value)
TRG / GFE	Glitch Filter Enable	Trigger Signal
SDI / SPEED	SPEED Mode Select	SPI Data Input

The attachment circuit of these pins depends upon the used interface type for measurement result output and the preferred method of configuration. Refer also to the application notes in the document " 4300x-AN-3-0-E-IPx.pdf".

12.3 Packaging

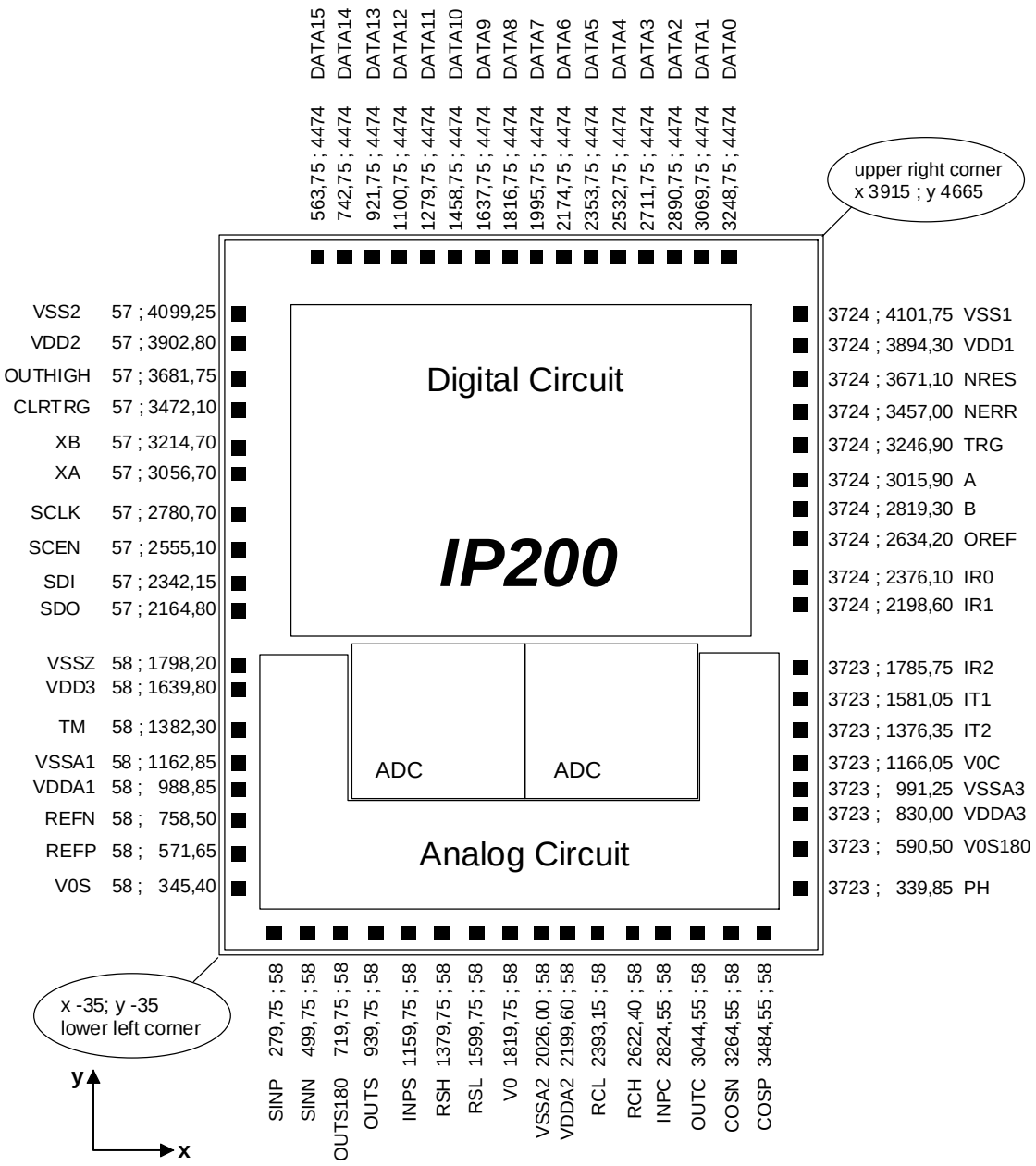
TQFP64 Package:



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-136

Figure 15

12.4 Bond Pattern



Notes:
1. All linear dimensions are in µm.
2. All pad dimensions refer to metall layer 2.
3. Pad size: 99,000 x 99,000.
4. Pad center point: X+49,500 x Y+49,500.
5. Dimension of lower left corner of bond window refer to pad dimensions: X+7,000 x Y+7,000.
6. Size of bond window: 85,000 x 85,000.

Pin	Name	Pads, lower left corner					
TQFP64		Metal 2 (99 x 99)		Bond (85 x 85)		Centre Point	
		x	y	x	y	x	y
1	DATA0	3248,75	4474,00	3255,75	4481,00	3298,25	4523,50
2	DATA1	3069,75	4474,00	3076,75	4481,00	3119,25	4523,50
3	DATA2	2890,75	4474,00	2897,75	4481,00	2940,25	4523,50
4	DATA3	2711,75	4474,00	2718,75	4481,00	2761,25	4523,50
5	DATA4	2532,75	4474,00	2539,75	4481,00	2582,25	4523,50
6	DATA5	2353,75	4474,00	2360,75	4481,00	2403,25	4523,50
7	DATA6	2174,75	4474,00	2181,00	4481,00	2224,25	4523,50
8	DATA7	1995,75	4474,00	2002,75	4481,00	2045,25	4523,50
9	DATA8	1816,75	4474,00	1823,75	4481,00	1866,25	4523,50
10	DATA9	1637,75	4474,00	1644,75	4481,00	1687,25	4523,50
11	DATA10	1458,75	4474,00	1465,75	4481,00	1508,25	4523,50
12	DATA11	1279,75	4474,00	1286,75	4481,00	1329,25	4523,50
13	DATA12	1100,75	4474,00	1167,75	4481,00	1150,25	4523,50
14	DATA13	921,75	4474,00	928,75	4481,00	971,25	4523,50
15	DATA14	742,75	4474,00	749,75	4481,00	792,25	4523,50
16	DATA15	563,75	4474,00	570,75	4481,00	613,25	4523,50
17	VSS2	57,00	4099,25	64,00	4106,25	106,50	4148,75
18	VDD2	57,00	3902,80	64,00	3909,80	106,50	3952,30
19	OUTHIGH	57,00	3681,75	64,00	3688,80	106,50	3731,25
20	CLRTRG	57,00	3472,10	64,00	3479,10	106,50	3521,60
21	XB	57,00	3214,70	64,00	3221,70	106,50	3264,20
22	XA	57,00	3056,70	64,00	3063,70	106,50	3106,20
23	SCLK	57,00	2780,70	64,00	2787,70	106,50	2830,20
24	SCEN	57,00	2555,10	64,00	2562,10	106,50	2604,60
25	SDI	57,00	2342,15	64,00	2349,15	106,50	2391,65
26	SDO	57,00	2164,80	64,00	2171,80	106,50	2214,30
27	VDD3	58,00	1639,80	65,00	1646,80	107,50	1689,30
28	TM	58,00	1382,30	65,00	1389,30	107,50	1431,80
29	VSSA1	58,00	1162,85	65,00	1169,85	107,50	1212,35
30	VDDA1	58,00	988,85	65,00	995,85	107,50	1038,35
31	REFN	58,00	785,50	65,00	792,50	107,50	835,00
32	REFP	58,00	571,65	65,00	578,65	107,50	621,15
33	SINP	279,75	58,00	286,75	65,00	329,25	107,50
34	SINN	499,75	58,00	506,75	65,00	549,25	107,50
35	OUTS180	719,75	58,00	726,75	65,00	769,25	107,50
36	OUTS	939,75	58,00	946,75	65,00	989,25	107,50
37	INPS	1159,75	58,00	1166,75	65,00	1209,25	107,50
38	RSH	1379,75	58,00	1386,75	65,00	1429,25	107,50
39	RSL	1599,75	58,00	1606,60	65,00	1649,25	107,50
40	V0	1819,75	58,00	1826,75	65,00	1869,25	107,50
41	VSSA2	2026,00	58,00	2033,00	65,00	2075,50	107,50
42	VDDA2	2199,60	58,00	2206,60	65,00	2249,10	107,50
43	RCL	2393,15	58,00	2400,15	65,00	2442,65	107,50
44	RCH	2622,40	58,00	2629,40	65,00	2671,90	107,50
45	INPC	2824,55	58,00	2831,55	65,00	2874,05	107,50
46	OUTC	3044,55	58,00	3051,55	65,00	3094,05	107,50
47	COSN	3264,55	58,00	3271,55	65,00	3314,05	107,50
48	COSP	3484,55	58,00	3491,55	65,00	3534,05	107,50
49	PH	3723,00	339,85	3730,00	346,85	3772,50	389,35
50	VDDA3	3723,00	830,00	3730,00	837,00	3772,50	879,50
51	VSSA3	3723,00	991,25	3730,00	998,25	3772,50	1040,75

Pin	Name	Pads, lower left corner					
TQFP64		Metal 2 (99 x 99)		Bond (85 x 85)		Centre Point	
		x	y	x	y	x	y
52	IT2	3723,00	1376,35	3730,00	1383,35	3772,50	1425,85
53	IT1	3723,00	1581,05	3730,00	1588,05	3772,50	1630,55
54	IR2	3723,00	1785,75	3730,00	1792,75	3772,50	1835,25
55	IR1	3724,00	2198,60	3731,00	2265,60	3773,50	2248,10
56	IR0	3724,00	2376,10	3731,00	2383,10	3773,50	2425,60
57	OREF	3724,00	2634,20	3731,00	2641,20	3773,50	2683,70
58	B	3724,00	2819,30	3731,00	2826,30	3773,50	2868,80
59	A	3724,00	3015,90	3731,00	3022,90	3773,50	3065,40
60	TRG	3724,00	3246,90	3731,00	3253,90	3773,50	3296,40
61	NERR	3724,00	3457,00	3731,00	3464,00	3773,50	3506,50
62	NRES	3724,00	3671,00	3731,00	3678,60	3773,50	3720,50
63	VDD1	3724,00	3894,30	3731,00	3901,30	3773,50	3943,80
64	VSS1	3724,00	4101,75	3731,00	4108,75	3773,50	4151,25

13 Revision History

Date	No.	Modification	Status
16.04.02	1.0	First preparation	preliminary
16.05.02	1.1	Modification page 10	preliminary
07.01.04	2.0	Diverse modifications and additions	actual
20.04.04	2.1	SPI protocol corrections, supplementation of mechanical and electrical parameters	actual