SC2440
2.5 MHz Dual Switching Regulator with Integrated 2A Switches

POWER MANAGEMENT

Description

The SC2440 is an adjustable frequency dual current-mode switching regulator with 2A integrated switches. Its high frequency operation allows the use of small inductors and capacitors, resulting in very compact power supplies. The SC2440 is suitable for next generation XDSL modems requiring operating frequencies in excess of 1.5 MHz. The two channels operate at 180° out of phase for reduced input voltage ripples. Separate soft start/shutdown pins allow independent control and output sequencing for latch-up prevention. The SC2440 can also be externally synchronized up to 2.5 MHz per channel.

Current-mode PWM control allows fast transient response with simple loop compensation. Cycle-by-cycle current limiting and hiccup overload protection reduce power dissipation during overload.

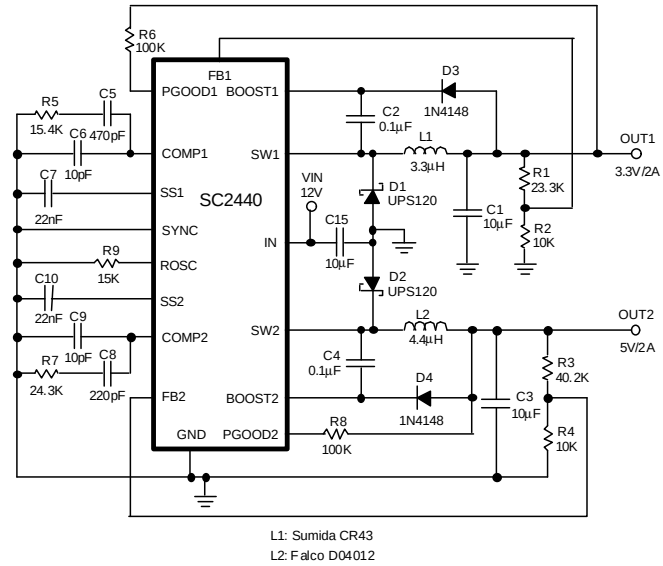
Features

- Up to 2.5 MHz/Channel Programmable Switching Frequency
- Fixed Frequency Current-mode Control
- Wide Input Voltage Range 2.8V to 20V
- Out of Phase Switching Reduces Ripple
- Cycle-by-cycle Current-limiting
- Independent Shutdown/soft-start Pins
- Independent Hiccup Overload Protection
- Independent Power-Good Indicators
- Two 2A Integrated Switches
- External Synchronization
- Thermal Shutdown
- Thermally Enhanced 16-pin TSSOP Package

Applications

- XDSL and Cable Modems
- Set-up Boxes
- Point of Load Applications
- CPE Equipment
- DSP Power Supplies
- Disk Drives

Typical Application Circuit



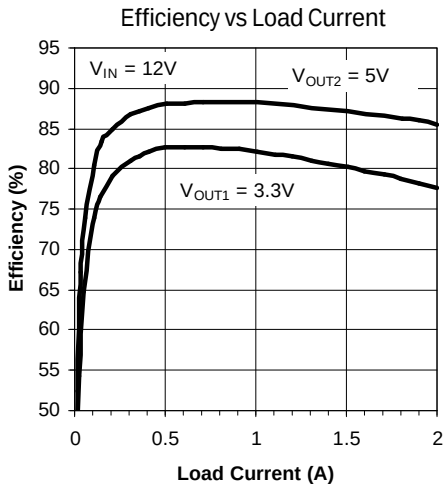


Figure 1. 1.3MHz 12V to 3.3V and 5V Step-down Converter

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Max	Units
Input Voltage	V_{IN}	-0.3 to 20	V
Boost Pin	V_{BST}	40	V
Boost Pin Above SW	V_{BST}-V_{SW}	20	V
PGOOD Pin Voltage	V_{PGOOD}	V_{IN}	V
SS Pins	V_{SS}	3	V
FB Pins	V_{FB}	-0.3 to V_{IN}	V
SYNC Pin Current	I_{SYNC}	5	mA
SW Voltage	V_{SW}	-0.6 to V_{IN}	V
SW Transient Spikes (<10ns Duration)	V_{SW}	V_{IN}+1.5	V
		-2.5	
Operating Ambient Temperature Range	T_A	-40 to 85	°C
Thermal Resistance Junction to Ambient	θ_{JA}	45	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering)10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless specified: -40°C < T_A < 85°C, -40°C < T_J < 105°C, R_{OSC} = 12.1KΩ, V_{SYNC} = 0, V_{IN} = 5V, V_{BOOST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
V_{IN} Start Voltage		2.45	2.62	2.78	V
V_{IN} Start Hysteresis			75		mV
Quiescent Current	Not switching, PGOOD Open		3.3	4.3	mA
Shutdown Current	V_{SS1} = V_{SS2} = 0V, PGOOD Open		38	60	µA
Feedback Voltage		0.980	1.000	1.020	V
Feedback Voltage Line Regulation	V_{IN} = 3V to 20V		0.005		%/V
FB Pin Input Bias Current	V_{FB} = 1V, V_{COMP} = 1.5V		-15	-30	nA
Error Amplifier Transconductance			280		$\mu\Omega^{-1}$
Error Amplifier Open-loop Gain			53		dB
COMP Source Current	V_{FB} = 0.8V, V_{COMP} = 1.5V		20		µA
COMP Sink Current	V_{FB} = 1.2V, V_{COMP} = 1.5V		20		µA
COMP Pin to Switch Current Gain			5.7		A/V

Electrical Characteristics (Cont.)

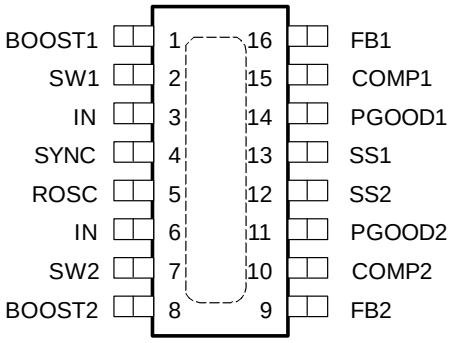
Unless specified: -40°C < T_A < 85°C, -40°C < T_J < 105°C, R_{OSC} = 12.1KΩ, V_{SYNC} = 0, V_{IN} = 5V, V_{BOOST} = 8V

Parameter	Conditions	Min	Typ	Max	Units
COMP Switching Threshold		0.7	1.1	1.3	V
COMP Maximum Voltage	V_{FB} = 0.9V		2.2		V
Channel Switching Frequecy		1.2	1.4	1.6	MHz
Maximum Duty Cycle	(Note 2)	80	90		%
Switch Current Limit	V_{FB} = 0.9V, V_{SS} = 2.3V, COMP Pin Open	2	2.6		A
Switch Saturation Voltage	I_{SW} = -2A		0.3	0.48	V
Switch Leakage Current				10	µA
Minimum Boost Voltage	I_{SW} = -2A		1.8	2.5	V
Boost Pin Current	I_{SW} = -0.5A		20	30	mA
	I_{SW} = -2A		60	80	mA
Minimum Soft-Start Voltage to Exit Shutdown	SS1 Tied to SS2	0.2	0.4	0.7	V
Soft-start Charging Current	V_{SS} = 0V		2		µA
	V_{SS} = 1.5V		1.8		µA
Soft-start Discharging Current	V_{SS} = 1.5V		0.8		µA
Minimum Soft-start Voltage to Enable Overload Shutoff	V_{SS} Rising		2		V
FB Overload Threshold	V_{SS} = 2.3V, V_{FB} Falling		0.74		V
Soft-start Voltage to Restart Switching After Overload Shutoff	V_{SS} Falling	0.7	1	1.3	V
Power Good Threshold Below FB	V_{FB} Rising	80	100	120	mV
Power Good Output Low Voltage	V_{FB} = 0.8V, I_{PGOOD} = 250µA		0.2	0.4	V
Power Good Pin Leakage Current	V_{PGOOD} = 5V		0.1	1	µA
SYNC Input High Voltage		2			V
SYNC Input Low Voltage	(Note 1)			0.8	V
SYNC Frequency	SYNC Frequency = 2 X Channel Frequency. (Note 1)	3.4		5	MHz
SYNC Pin Input Current	V_{SYNC} = 2V		60	75	µA
Thermal Shutdown Temperature			155		°C
Thermal Shutdown Hysteresis			10		°C

Notes: (1) Guaranteed by design, not tested in production.
(2) The maximum duty cycle specified corresponds to 1.4MHz switching frequency. Duty cycles higher than those specified can be achieved by lowering the operating frequency.
(3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration

TOP VIEW



(16 Pin TSSOP-EDP)

Underside metal must be soldered to ground.

Ordering Information

Part Number	Package(1)(2)
SC2440TETRT	TSSOP-16 EDP
SC2440EVB	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin #	Pin Name	Pin Function
1, 8	BOOST1, BOOST2	Supply pins to the power transistor drivers.Tie to external diode-capacitor charge pumps to generate drive voltages higher than V_{IN} in order to fully saturate the internal NPN power switches.
2, 7	SW1, SW2	Emitters of the internal power NPN transistors. Connect to the inductors, the freewheeling diodes and the boost capacitors.
3, 6	IN	Input power supply pins of the SC2440 and also the common collector of the internal power NPNs. Pins 3 and 6 are internally tied together and must be locally bypassed.
4	SYNC	Driving the SYNC pin with an external clock synchronizes both step-down converters. The external clock frequency must be at least twice the individual regulator set (or free-running) frequency. Tie this pin to ground if not used.
5	ROSC	An external resistor between this pin and the ground sets the master oscillator free-running frequency. The set frequency is twice that of the individual switching regulator.
9, 16	FB1, FB2	The inverting inputs of the error amplifiers. Each FB pin is tied to a resistive divider between its output and the ground for setting the channel output voltage.
10, 15	COMP1, COMP2	These are the outputs of the internal error amplifiers. The voltages on these pins control the peak switch currents. RC networks at these pins compensate the control loops. Pulling either pin below 0.7V stops the corresponding switching regulator.
11, 14	PGOOD1, PGOOD2	Open collector outputs of the Power Good comparators. Tie to external pull-up resistors from the input or the output of the converter. The PGOOD outputs become valid as soon as V_{IN} rises above 1 V_{BE} during power-up. PGOOD is actively pulled low until the corresponding FB pin rises to within 10% of the final regulation voltage.
12, 13	SS1, SS2	A capacitor from either SS pin to the ground provides soft-start and overload hiccup functions for that channel. Pulling either SS pin below 0.8V with an open drain or collector transistor shuts off the corresponding regulator. To completely shut off the SC2440 to low-current state, pull both SS pins to the ground. Soft-start is recommended for all applications.
Underside Metal	GND	The exposed pad at the bottom of the package is the electrical ground connection of the SC2440. It also provides a thermal contact to the circuit board. It is to be soldered to the ground plane of the board.

Block Diagrams

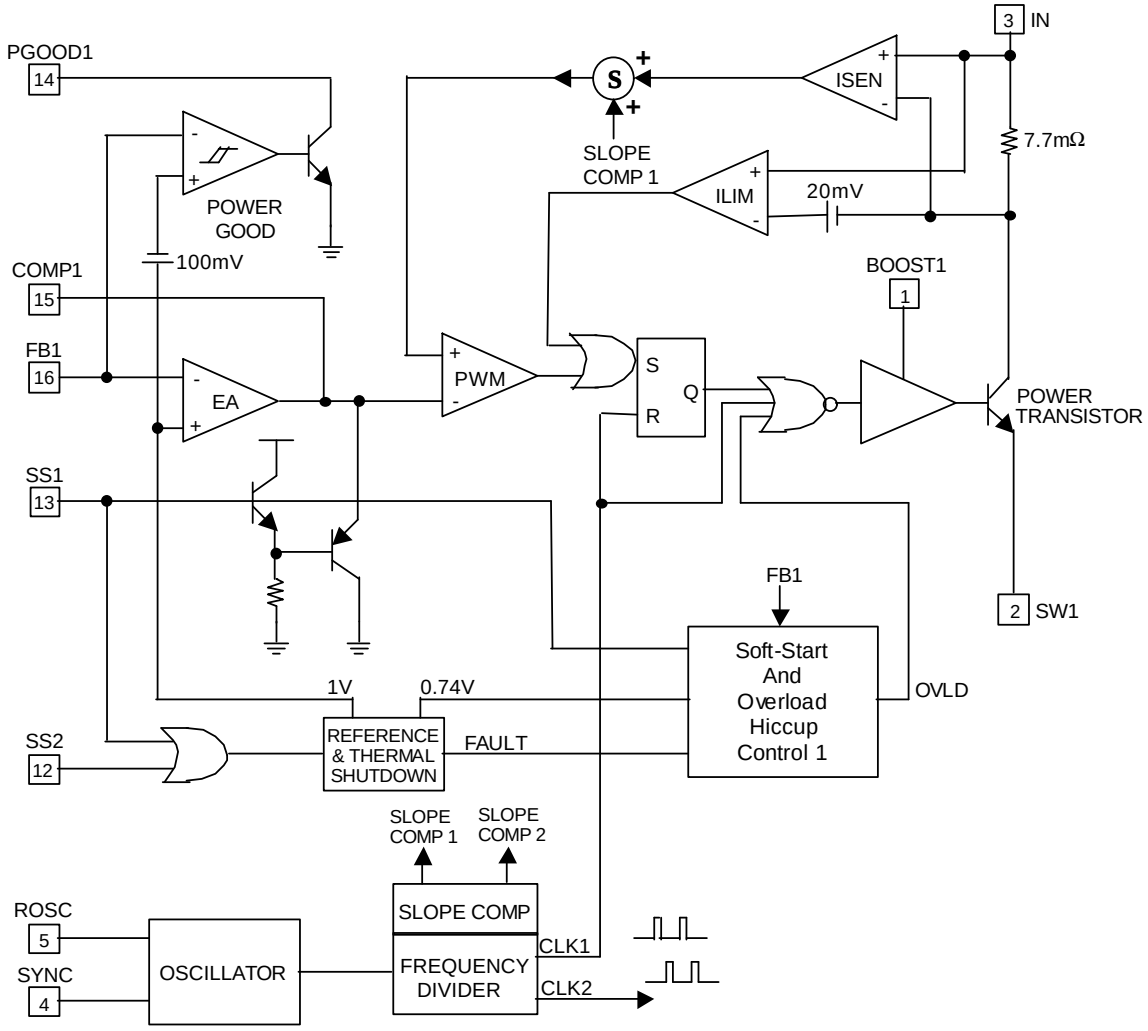


Figure 2. SC2440 Functional Diagram (One of Two Converters Shown)

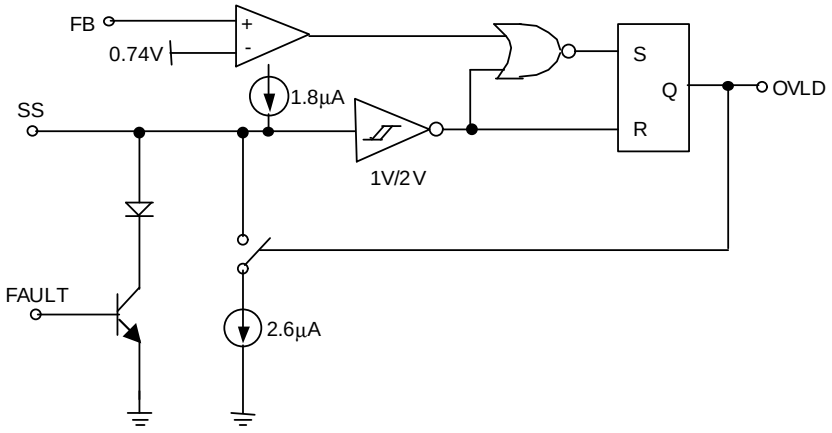
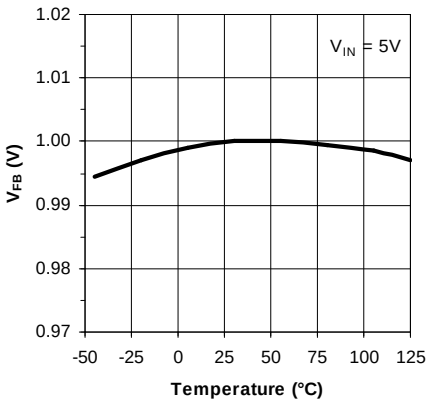


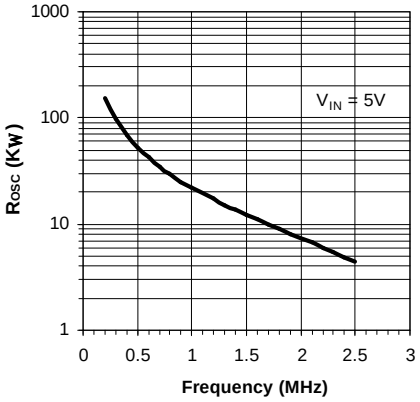
Figure 3. Details of the Soft-Start and Overload Hiccup Control Circuit

Typical Characteristics

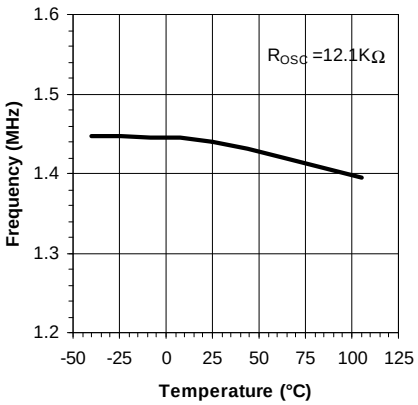
Feedback Voltage vs Temperature



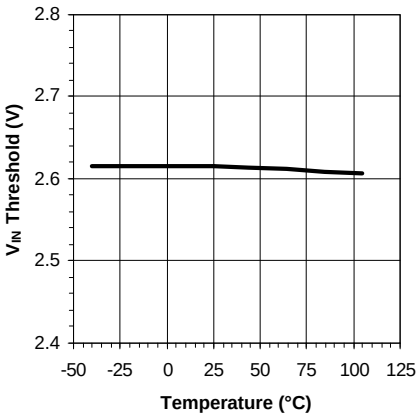
Frequency Setting Resistor vs Channel Frequency



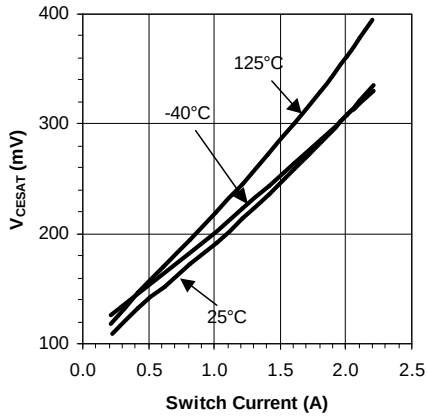
Channel Frequency vs Temperature



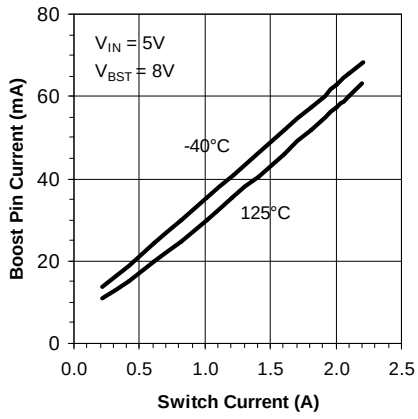
V_{IN} Start Threshold vs Temperature



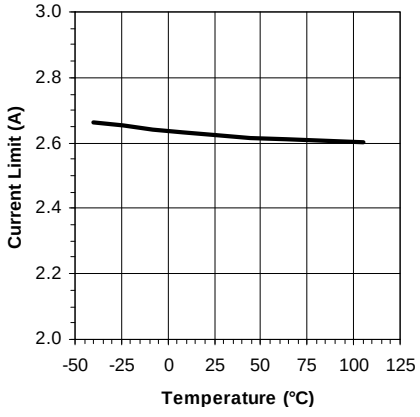
Switch Saturation Voltage vs Switch Current



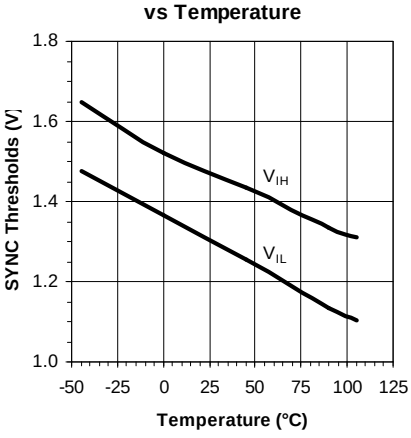
Boost Pin Current vs Switch Current



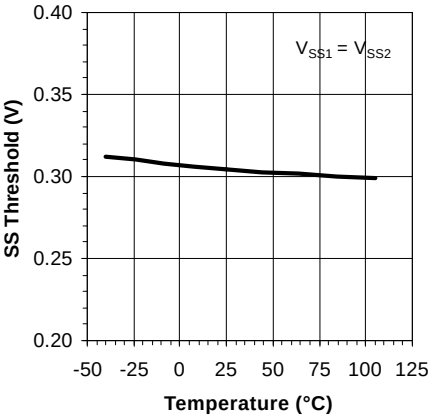
Switch Current Limit vs Temperature



SYNC Input Logic Thresholds vs Temperature

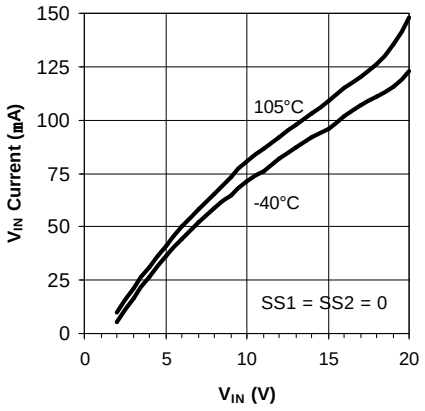


SS Shutdown Threshold vs Temperature

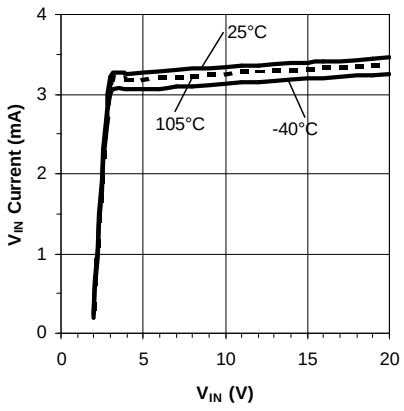


Typical Characteristics

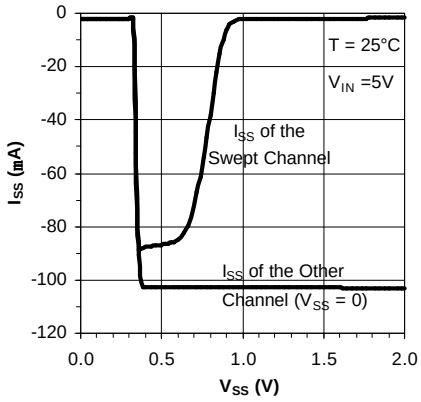
V_{IN} Shutdown Current vs V_{IN}



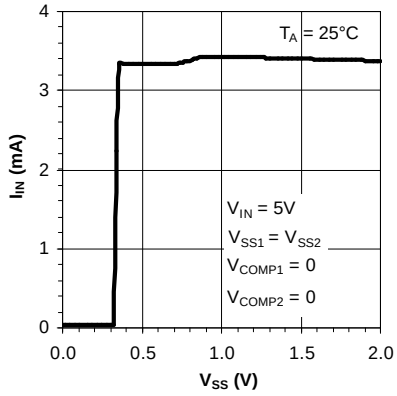
V_{IN} Quiescent Current vs V_{IN}



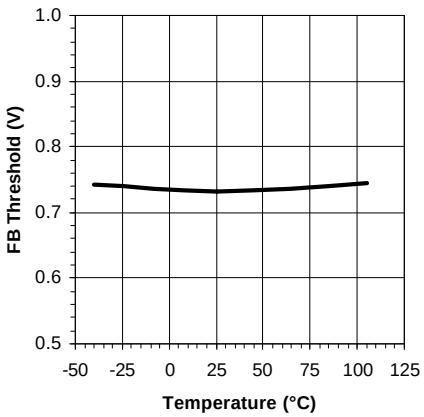
Soft-Start Pin Current vs Soft-Start Voltage



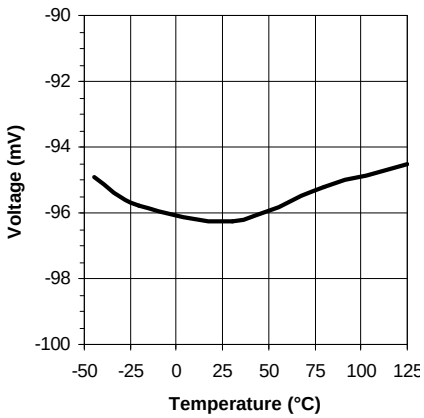
V_{IN} Supply Current vs Soft-Start Voltage



FB Overload Threshold vs Temperature



PGOOD Threshold to Feedback Difference Voltage vs Temperature



Operation

The SC2440 is a 2-channel constant-frequency peak current-mode step-down switching regulator with integrated 2A power transistors. Both regulators of the SC2440 operate from a common input power supply and share the same voltage reference, the master oscillator and the synchronizing circuit. Turn-on of the power transistors are phase-shifted by 180°. The two regulators are otherwise completely identical, independent and are capable of producing two separate outputs from the same input.

The master oscillator of the SC2440 runs at twice the channel frequency. The free-running frequency of the master oscillator can be programmed with an external resistor from the ROSC pin to ground. Frequency adjustability makes switching regulator design flexible.

Peak current-mode control is utilized for the SC2440. The double reactive poles of the output LC filter are reduced to a single real pole by the inner current loop, easing loop compensation. Fast transient response can be achieved with a simple Type-2 compensation network. Switch collector current is sensed with an integrated 7.7mΩ sense resistor. The sensed current is summed with slope-compensating ramp before it is compared with the transconductance error amplifier output. The PWM comparator tripping instant determines the switch turn-on pulse width (Figure 2). The current-limit comparator ILIM turns off the power switch when the sensed-signal exceeds the 20mV current-limit threshold. ILIM therefore provides cycle-by-cycle limit. Current-limit does not vary with duty-cycle.

Driving the base of the power transistor above the input power supply rail minimizes the power transistor turn-on voltage and maximizes efficiency. An external charge pump (formed by the capacitor C_2 and the diode D_3 in Figure 1) generates a voltage higher than the input rail at the BOOST pin. The bootstrapped voltage generated becomes the supply voltage for the power transistor driver.

The SS pin is a multiple-function pin. An external capacitor connected from the SS pin to the ground together with the internal 1.8µA and 2.6µA current sources set the soft-start and overload shutoff times of the regulator (Figure 3). The SS pin can also be used to shut off the corresponding regulator. When either SS pin is pulled below 0.8V, that regulator is turned off. If both SS pins are pulled below 0.2V, then the SC2440 undergoes overall shutdown. The current draw from the input power supply reduces to 38µA. When either SS pin is released, the corresponding soft-start capacitor is charged with a 2µA current source (not shown in Figure 3). As either SS voltage exceeds 0.3V, the internal bias circuit of the SC2440 is enabled. The SC2440 draws 3.3mA from V_{IN}. An internal fast charge circuit quickly charges the soft-start capacitor to 1V. At this juncture, the fast charge circuit turns off and the 1.8µA current source slowly charges the soft-start capacitor. The output of the error amplifier is forced to track the slow soft-start ramp at the SS pin. When the COMP voltage exceeds 1.1V, the switching regulator starts to switch. During soft-start, the current limit of the converter is gradually increased until the converter output comes into regulation.

Hiccup overload protection is utilized in the SC2440. Overload shutdown is disabled during soft-start (V_{SS} < 2V). In Figure 3 the reset input of the overload latch will remain high if the SS voltage is below 2V. Once the soft-start capacitor is charged above 2V, the overload shutdown latch is enabled. As the load draws more current from the regulator, the current-limit comparator will limit the peak inductor current. This is cycle-by-cycle current limiting. Further increase in load current will cause the output voltage to decrease. If the output voltage falls below 74% of its set point, then the overload latch will be set and the soft-start capacitor will be discharged with a net current of 0.8µA. The switching regulator is shut off until the soft-start capacitor is discharged below 1V. At this moment, the overload latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start. The regulator will go through soft-start, overload shutdown and restart until it is no longer overloaded.

Each regulator of the SC2440 has its own power good comparator. The open collector output of the power good comparator will be actively pulled low if the corresponding feedback voltage is below 0.9V.

Applications Information

Setting the Output Voltage

The regulator output voltage is set with an external resistive divider (Figure 4) with its center tap tied to the FB pin.

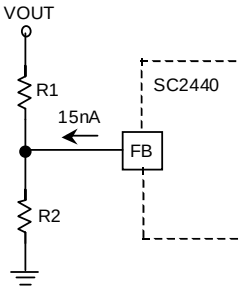


Figure 4. V_{OUT} is set with a Resistive Divider

$$R_1 = R_2(V_{OUT} - 1) \quad (1)$$

The percentage error due the input bias current of the error amplifier is

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (R_1 || R_2)}{1V}.$$

Example: Determine the output voltage error of a $V_{OUT} = 5V$ converter with $R_2 = 51.1K\Omega$.

From (1),

$$R_1 = 51.1K\Omega \cdot (5-1) = 205K\Omega$$

$$\frac{\Delta V_{OUT}}{V_{OUT}} = \frac{-15nA \cdot 100 \cdot (51.1K || 205K)}{1V} = -0.061\%.$$

This error is at least an order of magnitude lower than the ratio tolerance resulting from the use of 1% resistors in the divider string.

f (MHz)	R_9 (KΩ)	L_2 (µH)	R_7 (KΩ)	C_8 (pF)	C_9 (pF)
0.5	53.6	10 (Coiltronics DR73-100)	12.4	470	22
1.3	15.0	4.44 (Falco D04012)	24.3	220	10
2.5	4.02	2.7 (Sumida CR43-2R7)	32.4	220	10

Table 1. The 12V to 5V Converter in Figure 1 is modified to run at Different Frequencies.

Choosing the Operating Frequency

The free-running frequency of the **master** oscillator is set with an external resistor from the ROSC pin to ground. Channel frequency is one-half of that of the master oscillator. A graph of **channel** frequency against R_{OSC} is shown in the "Typical Performance Characteristics". Before choosing the operating frequency, tradeoffs among efficiency, operating duty cycle, component size and EMI interferences must be considered. High frequency operation reduces the size of passive components but switching losses are higher. Lowering the switching frequency improves efficiency. However the required inductor and capacitor are larger. Channel frequencies between 1 and 2MHz are good compromises.

In order to quantify the tradeoff between switching frequency and efficiency, the 12V to 5V DC-DC converter in Figure 1 is modified to run at 500KHz and 2.5MHz while keeping the inductor ripple current constant. The modified component values are tabulated in Table 1 and efficiencies at these frequencies are shown in Figure 5. The efficiency of the 1.3MHz 5V regulator in Figure 1 is also plotted for the ease of comparison. The efficiency at 500KHz is only marginally higher than that at 1.3MHz. The peak efficiency at 2.5MHz is only 2% lower compared to those at lower frequencies.

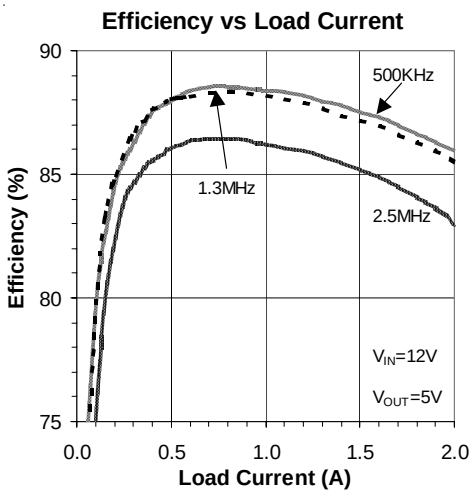


Figure 5. Efficiencies of 500KHz, 1.3MHz and 2.5MHz 12V to 5V Step-down Converters.

Applications Information

Minimum On Time Consideration

The operating duty cycle of a step-down switching regulator with diode rectifier in continuous-conduction mode (CCM) is given by

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{CESAT}} \quad (2)$$

where V_{CESAT} is the switch saturation voltage and V_D is voltage drop across the rectifying diode.

Duty cycle decreases with increasing $\frac{V_{IN}}{V_{OUT}}$ ratio. In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The intersection of this ramp with the output of the voltage feedback error amplifier determines the switch pulse width. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum switch on time ($T_{ON(MIN)}$). Closed-loop measurement of the SC2440 with low $\frac{V_{OUT}}{V_{IN}}$ ratios shows that the minimum on time is about 105ns at room temperature. $T_{ON(MIN)}$ also exhibits a slight positive temperature coefficient (Figure 6). The power switch in the SC2440 is either not turned on at all or for at least $T_{ON(MIN)}$. If the required switch on time ($=\frac{D}{f}$) is shorter than the minimum on time, the regulator will either skip cycles or it will jitter.

Example: Determine the maximum operating frequency of a dual 12V to 1.0V and 12V to 3.3V switching regulator using the SC2440.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 13.2V (10% high line), the corresponding duty ratios, D_1 and D_2, of the 1.0V and 3.3V converters can be calculated using (2).

$$D_1 = \frac{1 + 0.45}{13.2 + 0.45 - 0.25} = 0.11$$

$$D_2 = \frac{3.3 + 0.45}{13.2 + 0.45 - 0.25} = 0.28$$

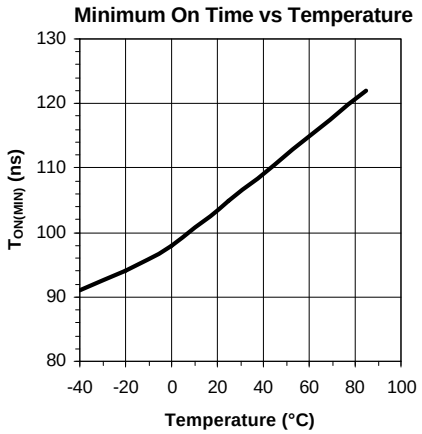


Figure 6. Variation of Minimum On Time with Temperature.

If the ambient temperature can be as high as 85°C, then the maximum operating frequencies of the 1.0V and the 3.3V converters will be $\frac{D_1}{120ns} = 920KHz$ and $\frac{D_2}{120ns} = 2.3MHz$ respectively.

Channel frequency should be set below 920KHz to allow margin for load transient.

Minimum Off Time Limitation

The PWM latch in Figure 2 is reset every period by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. Measurement shows that the power transistor needs to be turned off for at least 120ns every switching period to properly reset the latch and to refresh the bootstrap capacitor. For a step-down converter, D increases with increasing $\frac{V_{OUT}}{V_{IN}}$ ratio. If the required duty cycle is higher than the attainable maximum, then the

output voltage will not be able to reach its set value in continuous-conduction mode.

Example: Determine the maximum operating frequency of a dual 3.3V to 1.8V and 3.3V to 2.5V switching regulator using the SC2440.

Assuming that V_D = 0.45V, V_{CESAT} = 0.25V and V_{IN} = 2.97V (10% low line), the duty ratios D_1 and D_2 of the 1.8V and 2.5V converters can be calculated using (2).

$$D_1 = \frac{1.8 + 0.45}{2.97 + 0.45 - 0.25} = 0.71$$

$$D_2 = \frac{2.5 + 0.45}{2.97 + 0.45 - 0.25} = 0.93.$$

The maximum operating frequencies of the 1.8V and the 2.5V converters are therefore $\frac{1 - D_1}{120ns} = 2.4MHz$ and $\frac{1 - D_2}{120ns} = 580KHz$ respectively.

Transient headroom requires that channel frequency be lower than 580KHz.

External Synchronization

The SYNC input buffer is positive-edge triggered and TTL-compatible ($V_{IL} < 0.8V$ and $V_{IH} > 2V$). The free-running master oscillator generates a periodic sawtooth ramp between two threshold voltages. A faster external clock applied to the SYNC pin discharges the internal ramp before it reaches its upper threshold, thus locking the internal oscillator. As shown in Figure 2, the master oscillator is being synchronized not the individual phases (see Figure 2). The synchronizing frequency should be **twice** the desired **channel** frequency. Bench test shows that an external clock with frequency ranging from slightly below twice to at least 3.5 times the **channel** free-running frequency is capable of locking the master oscillator. To ensure frequency locking, the external clock frequency should be at least **twice** the **highest** free-running **channel** frequency. The frequency of the synchronizing clock should not be higher than 1.6 times the set frequency of master oscillator because the amplitudes of the internal sawtooth ramp and slope compensation ramp will both be significantly reduced.

Example: Choose the value of R_{OSC} to externally synchronize the SC2440 to 2MHz per **channel**.

The required synchronizing clock frequency = 2 times the channel frequency = 4MHz.

For a given R_{OSC}, the free-running **channel** frequency has a tolerance of ±15%.

Set the nominal free-running **channel** frequency to $\frac{2MHz}{1.15} = 1.73MHz$ to ensure locking.

Looking up the graph "Channel Frequency vs. R_{OSC}" in the Typical Characteristics, R_{OSC} = 9.31KΩ for a set frequency of 1.73MHz.

With ±15% tolerance, the set channel frequency can vary from $0.85 \cdot (1.73) = 1.47MHz$ to $1.15 \cdot (1.73) = 2MHz$. Therefore

$$\frac{\text{Synchronizing Frequency}}{\text{Lowest Free} - \text{running Frequency}} = \frac{2}{1.47} = 1.36.$$

Inductor Selection

The inductor ripple current ΔI_L for a non-synchronous step-down converter in continuous-conduction mode is

$$\Delta I_L = \frac{(V_{OUT} + V_D)(1 - D)}{fL} = \frac{(V_{OUT} + V_D)(V_{IN} - V_{OUT} - V_{CESAT})}{(V_{IN} + V_D - V_{CESAT})fL} \quad (3)$$

where f is the switching frequency and L is the inductance.

In current-mode control, the slope of the modulating (sensed switch current) ramp should be steep enough to lessen jittery tendency but not so steep that large flux swing decreases efficiency. Inductor ripple current ΔI_L between 25-40% of the peak inductor current limit is a good compromise. Inductors so chosen are optimized

in size and DCR. Setting $\Delta I_L = 0.3(2) = 0.6A$, $V_D = 0.45V$ and $V_{CESAT} = 0.25V$ in (3),

$$L = \frac{(V_{OUT} + 0.45)(V_{In} - V_{OUT} - 0.25)}{(V_{IN} + 0.2)(0.6)f} \quad (4)$$

where L is in µH and f is in MHz.

Equation (3) shows that for a given V_{OUT}, ΔI_L increases as D decreases. If V_{IN} varies over a wide range, then choose L based on the nominal input voltage. Always verify converter operation at the input voltage extremes.

The peak current limits of both SC2440 power transistors are internally set at 2.6A. The peak current limits are duty-cycle invariant and are guaranteed higher than 2A. The maximum load current is therefore conservatively

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = 2A - \frac{\Delta I_L}{2} \quad (5)$$

If $\Delta I_L = 0.3 \cdot I_{LM}$, then

$$I_{OUT(MAX)} = I_{LM} - \frac{\Delta I_L}{2} = I_{LM} - \frac{0.3 I_{LM}}{2} = 0.85 \cdot I_{LM}.$$

The saturation current of the inductor should be 20-30% higher than the peak current limit (2A). Low-cost powder iron cores are not suitable for high-frequency switching power supplies due to their high core losses. Inductors with ferrite cores should be used.

Input Capacitor

A buck converter draws pulse current with peak-to-peak amplitude equal to its output current I_{OUT} from its input supply. An input capacitor placed between the supply and the buck converter filters the AC current and keeps the current drawn from the supply to a DC constant. The input capacitance C_{IN} should be high enough to filter the pulse input current. Its equivalent series resistance (ESR) should be low so that power dissipated in the capacitor does not result in significant temperature rise and degrade reliability. For a single channel buck converter, the RMS ripple current in the input capacitor is

$$I_{RMS(CIN)} = I_{OUT}\sqrt{D(1-D)}. \quad (6)$$

Power dissipated in the input capacitor is $I^2_{RMS(CIN)} \cdot (ESR)$. Equation (6) has a maximum value of $\frac{I_{OUT}}{2}$ (at $D = \frac{1}{2}$), corresponding to the worst-case power dissipation $\frac{I^2_{OUT} \cdot ESR}{4}$ in C_{IN}.

A dual-channel step-down converter with interleaved switching reduces the RMS ripple current in the input capacitor to a fraction of that of a single-phase buck converter. If both power transistors in the SC2440 were to switch on in phase, the current drawn by the SC2440 would consist of current pulses with amplitude equal to the sum of the channel output currents. If each channel were delivering I_{OUT} and operating at 50% duty cycle, then the input current would switch from zero to $2I_{OUT}$. The RMS ripple current in the input capacitor would then be I_{OUT}. Power dissipated in C_{IN} would be $I^2_{OUT} \cdot ESR$, 4 times that of a single-channel converter. The SC2440 produces the highest RMS ripple current in C_{IN} when only one channel is running and delivering the maximum output current ($\approx 1.5 - 2A$). The input capacitor therefore should have a RMS ripple current rating of at least 1A.

Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple current, are the ideal choice for input filtering. A single 4.7µF or 10µF X5R ceramic capacitor is adequate. For high voltage applications, a small ceramic (1µF or 2.2µF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

Output Capacitor

The output ripple voltage ΔV_{OUT} of a buck converter can be expressed as

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (7)$$

where C_{OUT} is the output capacitance.

Inductor ripple current ΔI_L increases as D decreases (Equation (3)). The output ripple voltage is therefore the highest when V_{IN} is at its maximum. The first term in (7)

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results from the ESR of the output capacitor while the second term is due to the charging and discharging of C_{OUT} by the inductor ripple current. Substituting ΔI_L = 0.6A, f = 1MHz and C_{OUT} = 10µF ceramic with ESR = 3mΩ in (7),

$$\Delta V_{OUT} = 0.6A \cdot (3m\Omega + 12.5m\Omega)$$
$$= 1.8mV + 7.5mV = 9.3mV$$

Depending on operating frequency and the type of capacitor, ripple voltage resulting from charging and discharging of C_{OUT} may be higer than that due to ESR. A 10µF or 22µF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds C_{OUT}, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and high voltage coefficients.

Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery input current spikes, easing high-side current sensing in the SC2440. These diodes should have a RMS current rating between 1A and 2A and a reverse blocking voltage of at least 5V higher than the input voltage. For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher RMS current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The freewheeling diodes should be placed close to the SW pins of the SC2440 to minimize ringing due to trace inductance. Surface-mount equivalents of 1N5817 and 1N5819, MBRM120LT3 (ON Semi), UPS120 and UPS140 (Micro-Semi) are all suitable.

Bootstrapping the Power Transistors

To maximize efficiency, the turn-on voltage across the internal power NPN transistors should be minimized. If these transistors are to be driven into saturation, then their bases will have to be driven from a power supply higher in voltage than V_{IN}. The required driver supply voltage (at least 2.5V higher than the SW voltage over the industrial temperature range) is generated with a bootstrap circuit (the diode D_{BST} and the capacitor C_{BST} in Figure 8). The bootstrapped output (the common node between D_{BST} and C_{BST}) is connected to the BOOST pin of the SC2440. The power transistor in the SC2440 is first switched on to build up current in the inductor. When the transistor is switched off, the inductor current pulls the SW node low, allowing C_{BST} to be charged through D_{BST}. When the power switch is again turned on, the SW voltage goes high. This brings the BOOST voltage to $V_{SW} + V_{C_{BST}}$, thus back-biasing D_{BST}. C_{BST} voltage increases with each subsequent switching cycle, as does the bootstrapped voltage at the BOOST pin. After a number of switching cycles, C_{BST} will be fully charged to a voltage approximately equal to that applied to the anode of D_{BST}. Figure 7 shows the typical minimum BOOST to SW voltage required to fully saturate the power transistor. This differential voltage ($= V_{C_{BST}}$) must be at least 1.8V at room temperature. This is also specified in the "Electrical Characteristics" as "Minimum Bootstrap Voltage". The minimum required $V_{C_{BST}}$ increases as temperature decreases. The bootstrap circuit reaches equilibrium when the base charge drawn from C_{BST} during transistor on time is equal to the charge replenished during the off interval.

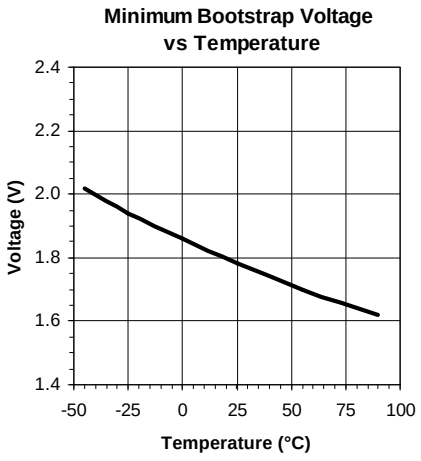

Figure 7. Typical Minimum Bootstrap Voltage Required to Maintain Saturation at I_{SW} = 2A.

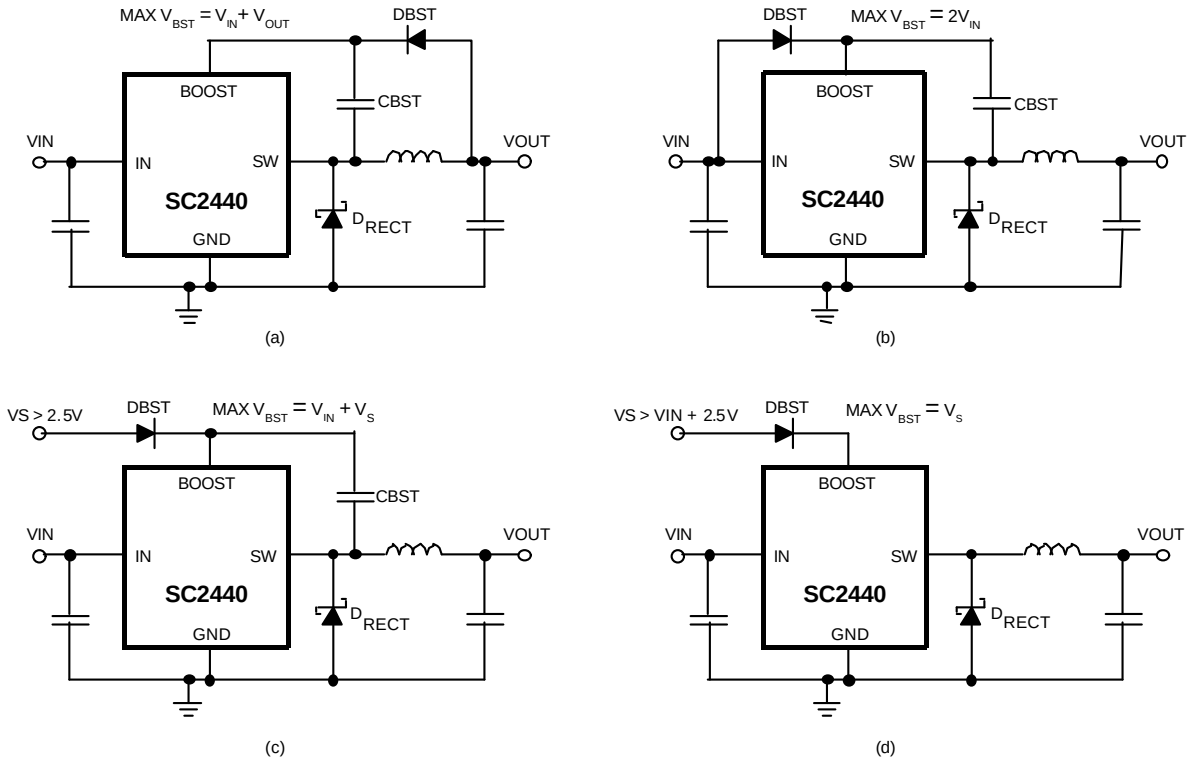

Figure 8. Methods of Bootstrapping the SC2440.

The switch base current $= \frac{I_{SW}}{\hat{a}+1} \approx \frac{I_{SW}}{\hat{a}}$, where I_{SW} and β are the switch emitter current and current gain respectively, is drawn from the bootstrap capacitor C_{BST}. Charge $\frac{I_{SW}T_{ON}}{\hat{a}}$ is drawn from C_{BST} during the switch on time, resulting in a voltage droop of $\frac{I_{SW}T_{ON}}{\hat{a}C_{BST}}$. If I_{SW} = 2A, T_{ON} = 1µs, β = 35 and C_{BST} = 0.1µF, then the $V_{C_{BST}}$ droop will be 0.57V. C_{BST} is refreshed to $V_A - V_{D_{BST}} + V_{D_{RECT}}$ every cycle, where V_A is the applied D_{BST} anode voltage. Switch base current discharges the bootstrap capacitor to $V_A - V_{D_{BST}} + V_{D_{RECT}} - \frac{I_{SW}T_{ON}}{\beta C_{BST}}$ at the end of conduction. The difference between this voltage and that at SW must be higher than the minimum shown in Figure 7 to maximize efficiency. D_{BST} can be tied either to the input or to the output of the DC/DC converter.

If D_{BST} is tied to the input, then the charge drawn from the input power supply will be $\frac{I_{SW}T_{ON}}{\beta}$ (the base charge of the switch). The energy loss due to base charge per cycle is $\frac{I_{SW}V_{IN}T_{ON}}{\beta}$ for a power loss of $\frac{DI_{SW}V_{IN}}{\beta} \approx \frac{I_{SW}V_{OUT}}{\beta}$.

If D_{BST} is tied to the output, then the charge drawn from the output capacitor will still be $\frac{I_{SW}T_{ON}}{\beta}$. The energy loss due to base charge per cycle is $\frac{I_{SW}V_{OUT}T_{ON}}{\beta}$ for a power

loss of $\frac{DI_{SW}V_{OUT}}{\beta}$.

Since $V_{OUT} < V_{IN}$, D_{BST} should always be tied to V_{OUT} (if >2.5V) to maximize efficiency. Measurement of the 2-channel regulator in Figure 1 shows that the efficiency penalties are about 1.3% (V_{OUT} = 5V) and 2.2% (V_{OUT} = 3.3V) with input bootstrapping. In general efficiency penalty increases as D decreases.

Figure 8 summarizes various ways of bootstrapping the SC2440. A fast switching PN diode (such as 1N4148 or 1N914) and a small (0.1µF – 0.47µF) ceramic capacitor can be used. In Figure 8(a) the power switch is bootstrapped from the output. This is the most efficient configuration and it also results in the least voltage stress at the BOOST pin. The maximum BOOST pin voltage is about $V_{IN}+V_{OUT}$. If the output is below 2.8V, then D_{BST} will preferably be a small Schottky diode (such as BAT-54) to maximize bootstrap voltage. A 0.33-0.47µF bootstrap capacitor may be needed to reduce droop. Bench measurement shows that using Schottky bootstrapping diode has no noticeable efficiency benefit.

The SC2440 can also be bootstrapped from the input (Figure 8(b)). This configuration is not as efficient as Figure 8(a). However this may be only option if the output voltage is less than 2.5V and there is no other supply with voltage higher than 2.5V. Voltage stress at the BOOST pin can be somewhat higher than $2V_{IN}$. The BOOST pin voltage should not exceed its absolute maximum rating of 40V.

Figures 8(c) and (d) show how to bootstrap the SC2440 from a second independent power supply V_S with voltage > 2.5V. D_{BST} in Figure 8(d) prevents start up difficulty if V_{IN} comes up before V_S.

Since the inductor current charges C_{BST}, the bootstrap circuit requires some minimum load current to get going. Figures 9(a) and 9(b) show the dependence of the minimum input voltage required to properly bootstrap a 5V and a 3.3V converters on the load current. Once started the bootstrap circuit is able to sustain itself down to zero load.

Shutdown and Soft-Start

Each regulating channel of the SC2440 has its own soft-start circuit. Pulling its soft-start pin below 0.8V with an open-collector NPN or an open-drain NMOS transistor turns off the corresponding regulator. The other regulator continues to operate. With one channel turned off, the internal bias circuit is kept alive. In the "Typical Characteristics", the soft-start pin current is plotted against the soft-start voltage with V_{IN} = 5V. When one of

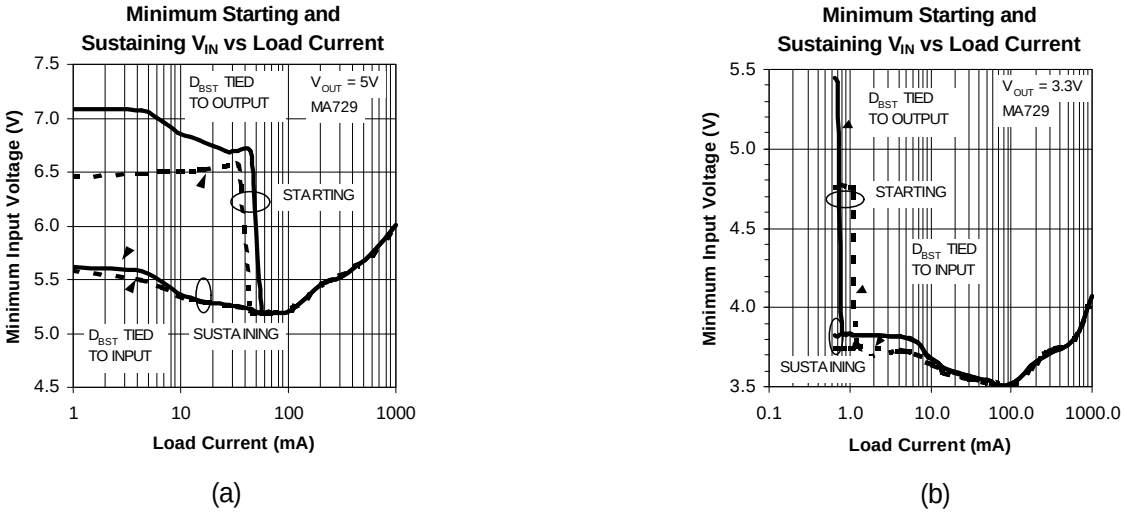

Figure 9. Minimum Input Voltage Required to Start and to Maintain Bootstrap.(T_A = 25°C).

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the soft-start pins is pulled low, 105µA flows out of that pin. Pulling both soft-start pins below 0.2V shuts off the internal bias circuit of the SC2440. The total V_{IN} current decreases to 38µA. In shutdown either SS pin sources only 2µA. A fast charging circuit (enabled by the internal bias circuit), which charges the soft-start capacitor below 1V, causes the difference in the soft-start pin currents.

If either SS pin is released in shutdown, the internal current source pulls up on the SS pin. When this SS voltage reaches 0.3V, the SC2440 turns on and the V_{IN} quiescent current increases to 3.3mA. The current flowing out of the other SS pin (which is still pulled low) increases to 105µA. The fast charging circuit quickly pulls the released soft-start capacitor to 1V (slightly below the switching threshold). The fast charging circuit is then disabled. A 1.8µA current source continues to charge the soft-start capacitor (Figure 3). The soft-start voltage ramp at the SS pin clamps the error amplifier output (Figure 2). During regulator start-up, COMP voltage follows the SS voltage. The converter starts to switch when its COMP voltage exceeds 1.1V. The peak inductor current gradually increases until the converter output comes into regulation. Proper soft-start prevents output overshoot during start-up. Current drawn from the input supply is also well controlled. Notice that the inductor current, not the converter output voltage, is ramped during soft-start.

Both soft-start capacitors are charged to a final voltage of about 2.4V.

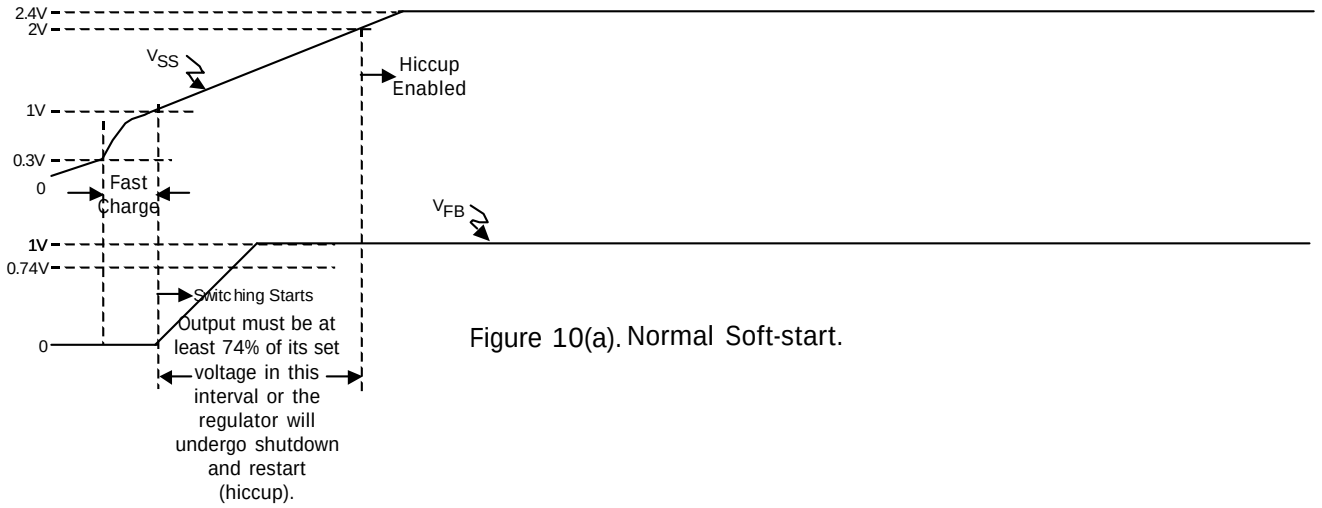

Figure 10(a). Normal Soft-start.

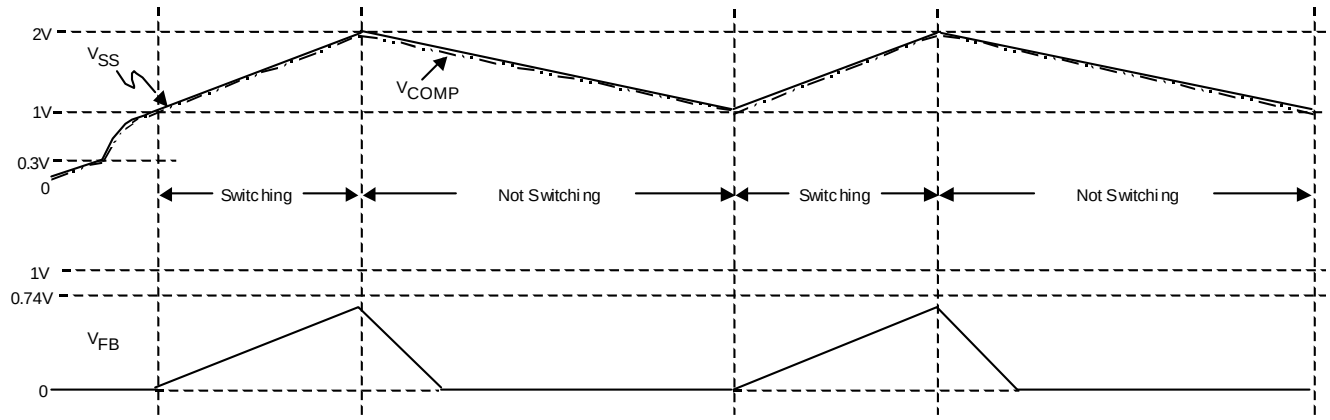

Figure 10(b). Start-up Fails due to (i) Short Soft-start Duration or (ii) Output Overload or (iii) Output Short-circuited.

Overload / Short-Circuit Protection

Each current limit comparator in the SC2440 limits the peak inductor current to 2.6A. The regulator output voltage will fall if the load is increased above the current limit. If overload is detected (the output voltage falls below 74% of the set voltage), then the regulator will be shut off. An internal 0.8µA current sink starts to discharge the soft-start capacitor. As the soft-start capacitor is discharged below 1V, the discharge current source turns off and the soft-start capacitor is recharged with a 1.8µA current source. The regulator undergoes soft-start. During soft-start ($1V < V_{SS} < 2V$), the overload shutdown latch in Figure 3 cannot be set. When V_{SS} exceeds 2V, the set input of the overload latch is no longer blanked. If V_{FB} is still below 0.74V, then the regulator will undergo shutdown and restart. The soft-start process should allow the output voltage to reach 74% of its final value before C_{SS} is charged above 2V. Figures 10(a) and 10(b) show the timing diagrams of successful and failed start-up waveforms respectively. The soft-start interval should also be made sufficiently long so that the output voltage rises monotonically and it does not overshoot its final voltage by more than 5%. When starting into a shorted output, the SC2440 will repeatedly start and shut off ("hiccup"). V_{SS} and V_{COMP} will appear as asymmetrical triangular waves [Figure 10(b)].

Power Good Indicators

The PGOOD pins (Pins 11 and 14) are the open-collector outputs of the power good comparators. These slow comparators are incorporated with small amount of hysteresis. The FB low-to-high trip voltage of the power good comparators is 90% of the final regulation voltage. A pull-up resistor from each PGOOD pin to the input supply or the regulator output set the logic high level of the comparator.

The power good comparator output becomes valid provided that V_{IN} is above 0.9V. In shutdown the power good output is actively pulled low. A power good pull-up resistor tied to the input will therefore increase current drain during shutdown. Tying the power good pull-up resistor to the regulator output is preferred, as this will minimize the shutdown supply current. In shutdown there

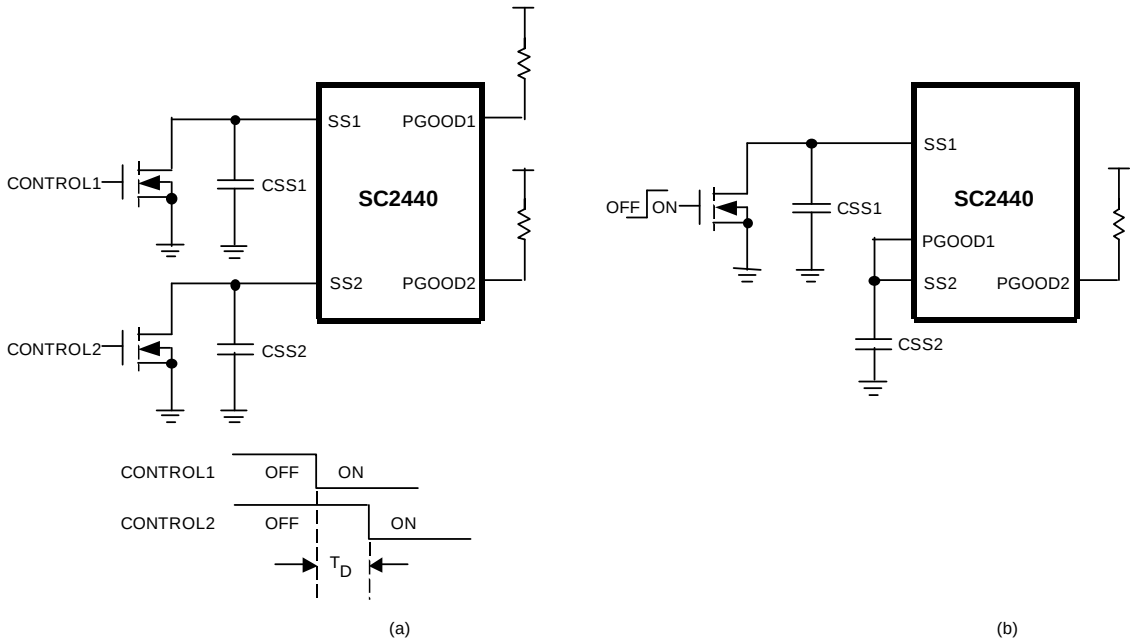

Figure 11. Sequencing the Outputs by (a) Delaying Release of one Channel Relative to the Other and (b) Using the PGOOD of one Channel to Control the Other.

is no voltage at the switching regulator output or current in the PGOOD pull-up resistor. If the PGOOD output high level (= V_{OUT}) is unacceptably low, then power good pull-up from the input or a separate power supply will be the only choice.

Sequencing the Outputs

As mentioned above, pulling either soft-start pin low with an external transistor shuts off the corresponding regulator (Figure 11). Releasing the soft-start pin enables that channel and allows it to start. Delaying the release of the soft-start pin of one channel with respect to the other is a straightforward way of sequencing the outputs. Figure 11(a) shows this method using two external transistors M_1 and M_2. M_1 is turned off first, allowing channel 1 to start. Channel 2 is then enabled after time T_D.

The PGOOD output of one channel can also be used in conjunction with the soft-start pin of the other channel to delay start of that regulator. This method is depicted in Figure 11(b). SS2 is pulled low and channel 2 is kept off until channel 1 output rises to 90% of its set voltage. A drawback of this approach is that only PGOOD2 is available as a logic output.

Loop Compensation

Figure 12 shows a simplified equivalent circuit of a step-down converter. The power stage, which consists of the current-mode PWM comparator, the power switch, the freewheeling diode and the inductor, feeds the output network. The power stage can be modeled as a voltage-controlled current source, producing an output current proportional to its controlling input V_{COMP}. Its transconductance G_{MP} is $5.7\Omega^{-1}$. With the current loop closed, the control-to-output transfer function $\frac{V_{OUT}}{V_{COMP}}$ has a dominant-pole p_2 located at a frequency slightly higher than that of the output filter pole.

$$\omega_{p2} \approx -\frac{nI_{OUT}}{V_{OUT}C_1} = -\frac{n}{R_{OUT}C_1} \quad (8)$$

where C_1 is the output capacitor, R_{OUT} is the equivalent load resistance and n (depending on duty ratio, slope compensation, frequency and passive components) is usually between 1 and 2.

If C_1 is ceramic, then its ESR zero can be neglected as it situates well beyond half the switching frequency. The low frequency gain of the control-to-output transfer function is simply the product of power stage transconductance and the equivalent load resistance (Figure 13).

The transfer functions of the feedback network and the error amplifier are:

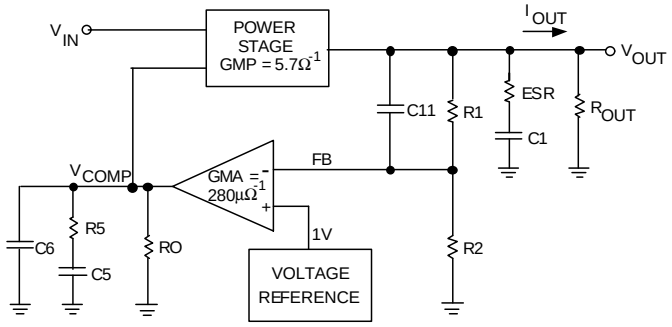

Figure 12. Simplified Control Loop Equivalent Circuit

$$\frac{V_{FB}}{V_{OUT}} = \left(\frac{R_2}{R_1+R_2}\right)\left[\frac{1+sC_{11}R_1}{1+s(R_1||R_2)C_{11}}\right] \quad (9)$$

and

$$\frac{V_{COMP}}{V_{FB}} \approx \frac{G_{MA}R_O(1+sC_5R_5)}{(1+sC_5R_O)\cdot(1+sC_6R_5)} \quad (10)$$

provided that $C_5 >> C_6$ and $R_O >> R_5$.

In Equation (10), C_5 forms a low frequency pole p_1 with the output resistance R_O of the error amplifier and C_6 forms a high frequency pole p_3 with R_5. Using the component values shown in Figure 1 for the 12V to 3.3V regulator (1.3MHz),

$$R_O = \frac{\text{Amplifier Open Loop Gain}}{\text{Transconductance}} = \frac{53dB}{280\mu\Omega^{-1}} = 1.6M\Omega$$

$$\omega_{p1} = -\frac{1}{R_OC_5} = -\frac{1}{1.6M\Omega \bullet 470pF}$$
$$= -1.3Krads^{-1} = -210Hz$$

$$\omega_{p3} = -\frac{1}{R_5C_6} = -\frac{1}{15.4K\Omega \bullet 10pF}$$
$$= -6.5Mrads^{-1} = -1.0MHz$$

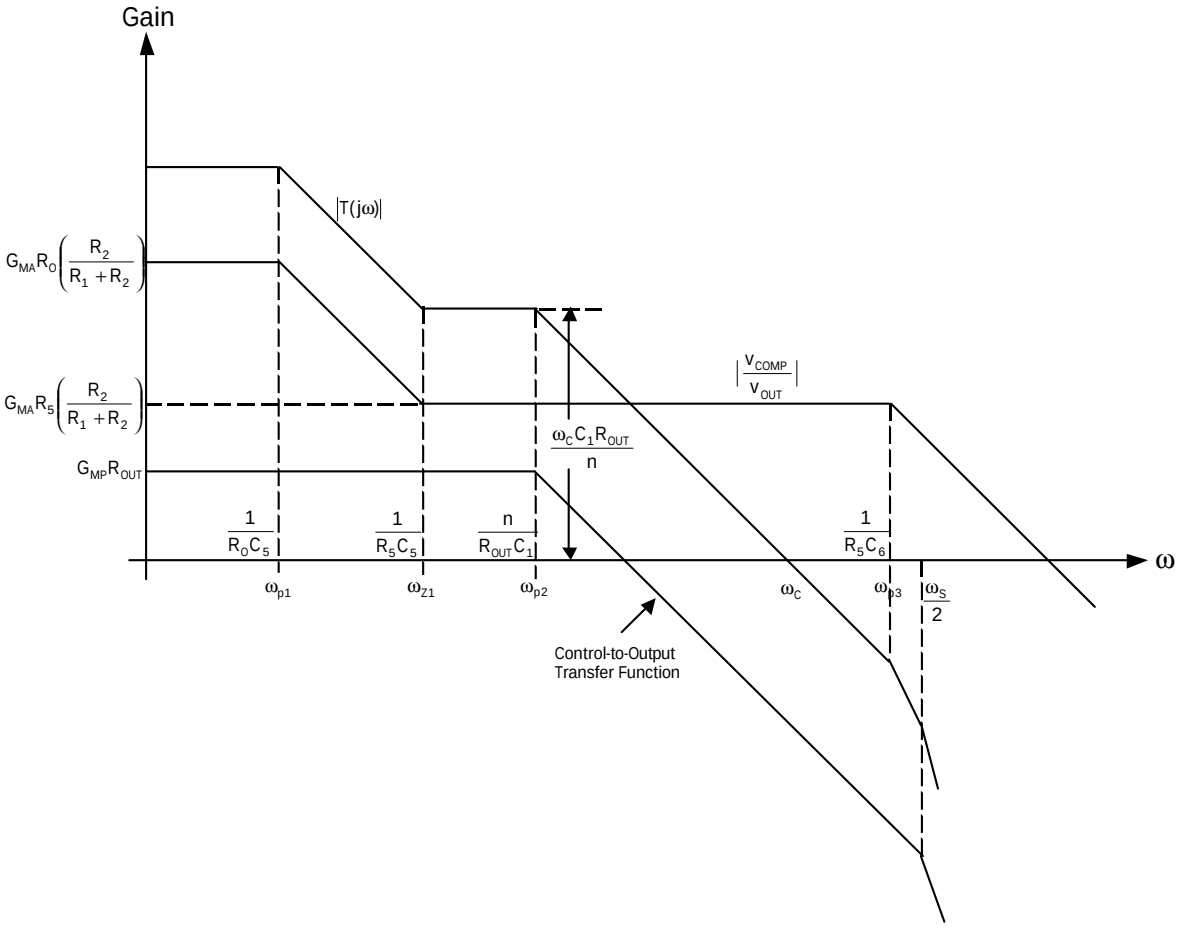

Figure 13. Bode Plots of Control-to-Ouput, Output-to-Control and the Overall Loop Gain. Control-to-output transfer function is shown with two poles near half the switching frequency ω_S.

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In addition C_5 and R_5 form a zero with angular frequency:

$$\omega_{Z1} = -\frac{1}{R_5 C_5} = -\frac{1}{15.4K\Omega \cdot 470pF}$$
$$= -140\,Krads^{-1} = -22KHz$$

The output-to-control transfer function $\frac{v_{COMP}}{v_{OUT}} = \frac{v_{COMP}}{v_{FB}} \cdot \frac{v_{FB}}{v_{OUT}}$ is also shown in Figure 13. Its mid-band gain (between z_1 and p_3) is $G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right)$. The overall loop gain T(s) is the product of the control-to-output and the output-to-control transfer functions. To simplify $|T(j\omega)|$ Bode plot, the feedback network is assumed to be resistive. If the overall loop gain is to cross 0dB at one tenth of the switching frequency ($\omega_C = \frac{\omega_S}{10} = \frac{\pi f}{5}$) at –20dB/decade, then its mid-band gain (between z_1 and p_2) will be

$$\frac{\omega_c}{\omega_{p2}} = \frac{\frac{\omega_S}{10}}{\frac{n}{C_1 R_{OUT}}} = \frac{\omega_S C_1 R_{OUT}}{10n}.$$

This is also equal to $G_{MP}R_{OUT}G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right)$. Therefore

$$G_{MP}R_{OUT}G_{MA}R_5\left(\frac{R_2}{R_1+R_2}\right) = \frac{\omega C_1 R_{OUT}}{10n}.$$

Re-arranging,

$$R_5 = \left(1+\frac{R_1}{R_2}\right)\frac{\omega_S C_1}{10nG_{MP}G_{MA}} \quad (11)$$

ω_{z1} is shown to be less than ω_{p2} in Figure 13. Making $\omega_{z1} = \omega_{p2}$ gives a first-order estimate of C_5:

$$C_5 = \frac{C_1 R_{OUT(MIN)}}{nR_5} \quad (12)$$

Notice that R_5 determines the mid-band loop gain of the converter. Increasing R_5 increases the mid-band gain and the crossover frequency. However it reduces the phase margin. An estimate of R_5 and C_5 can be obtained from (11) and (12) with n=1. The compensation is then checked by measuring the loop gain and the phase or by observing the inductor current and the output voltage during load transient. Choose the largest R_5 and the smallest C_5 to give at least 45° of phase margin. The corresponding load transient should not show any ringing or excessive overshoot (see Figures 14(c), 14(d), 17(b) and 17(c)). C_6 is a small ceramic capacitor (10-47pF) to roll off the loop gain at high frequency. Feedforward capacitor C_{11} boosts phase margin over a limited frequency range and is sometimes used to improve loop response. C_{11} will be more effective if $R_1 >> R_1 || R_2$.

Example: Determine the compensation components for the 1.3MHz 12V to 5V and 3.3V converter in Figure 1. For both channels, $\omega_S = 8.2Mrads^{-1}$, $I_{OUT(MAX)} = 2A$ and $C_1 = 10\mu F$. n is assumed to be 1 in (11) and (12).

For the 3.3V output:

$$R_5 = \left(1+\frac{23.3K}{10K}\right)\frac{8.2\times10^6 \cdot 10^{-5}}{10\cdot(1)\cdot(5.7)\cdot(2.8\times10^{-4})}$$
$$= 16.9K\Omega$$

$$C_5 = \frac{10^{-5}\cdot 3.3V}{(1)\cdot 16.9K\cdot(2A)} = 1nF$$

For the 5V channel:

$$R_7 = \left(1+\frac{40.2K}{10K}\right)\frac{8.2\times10^6 \cdot 10^{-5}}{10\cdot(1)\cdot(5.7)\cdot(2.8\times10^{-4})}$$
$$= 25.5K\Omega$$

$$C_8 = \frac{10^{-5}\cdot 5V}{(1)\cdot 25.5K\cdot(2A)} = 1nF$$

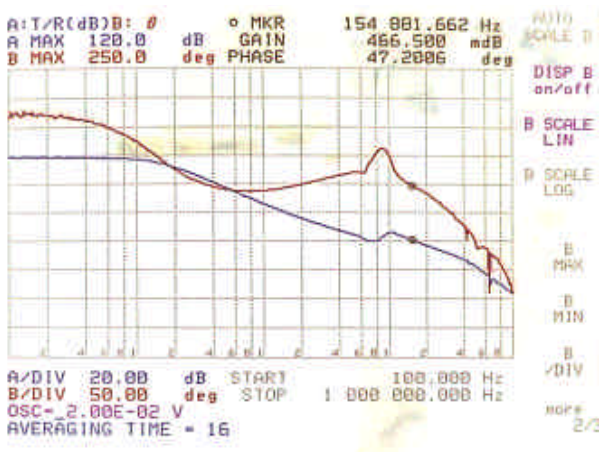
C_6 and C_9 (both 10pF) are then added to increase gain margin. Load transient responses of both channels are observed using these values. There is very little inductor current overshoot even with C_5 and C_8 reduced to 470pF and 220pF respectively (Figure 14). The measured overall loop gain and phase plots of the converter are also shown.

Applications Information

Board Layout Considerations

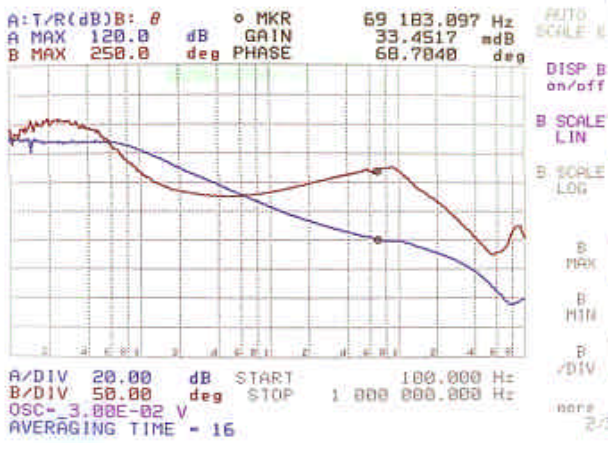
In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry switched currents with high $\frac{di}{dt}$ (Figure 15). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switches are already integrated within the SC2440, connecting the anodes of both freewheeling diodes close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitors should also be placed close to the

V_{IN}=12V, V_{OUT}=3.3V at 1.7A,
C_5=470pF, R_5=15.4KΩ and C_6=10pF

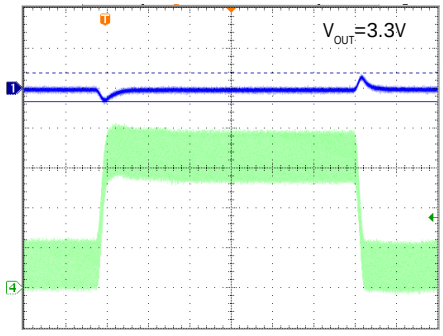


(a)

V_{IN}=12V, V_{OUT}=5V at 1.7A,
C_7=220pF, R_8=24.3KΩ and C_9=10pF



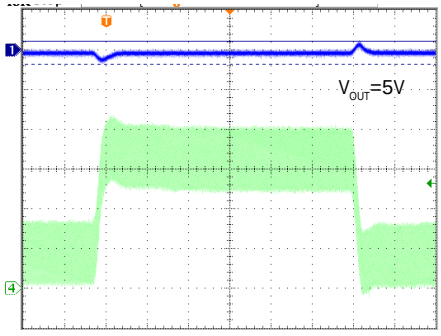
(b)



40µs/div

Upper Trace : OUT1 Voltage, AC Coupled, 0.5V/div
Lower Trace : L_1 Inductor Current, 0.5A/div

(c)



40µs/div

Upper Trace : OUT2 Voltage, AC Coupled, 0.5V/div
Lower Trace : L_2 Inductor Current, 0.5A/div

(d)

Figure 14. Overall Loop Gain and Phase versus Frequency for (a) Channel 1 and (b) Channel 2 of the Dual DC-DC Converter in Figure 1. (c) Channel 1 Load Transient Response, I_{OUT1} is switched between 0.3A and 1.7A. (d) Channel 2 Load Transient Response, I_{OUT2} is switched between 0.45A and 1.7A.

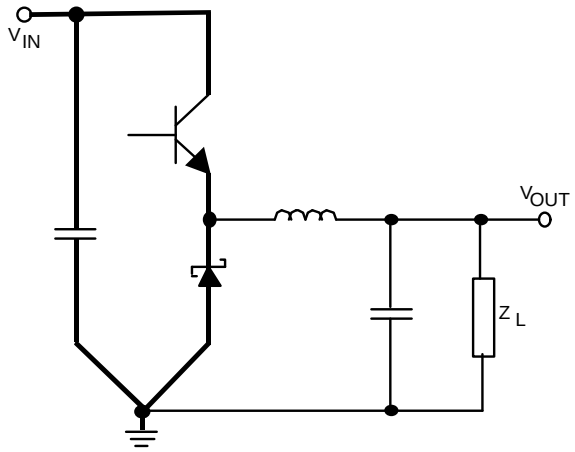
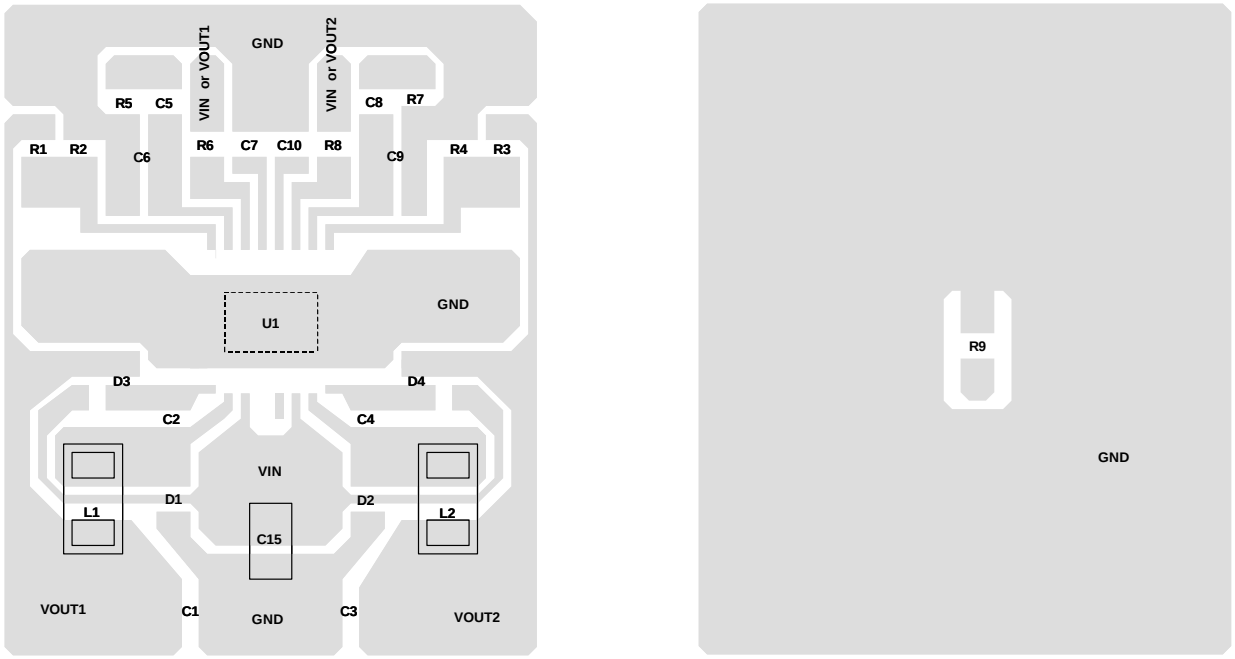


Figure 15. Fast Switching Current Paths in a Buck Regulator. Minimize the size of this loop to reduce parasitic trace inductance.

input pins. Shortening the traces of the SW and BOOST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

Figures 16(a) and 16(b) shows how various external components are placed around the SC2440. The frequency-setting resistor is placed next to the ROSC pin on the backside. The resistor is grounded to the ground plane, which is then tied to anodes of the freewheeling diodes with vias. These precautions reduce switching noise pickup at the ROSC pin.

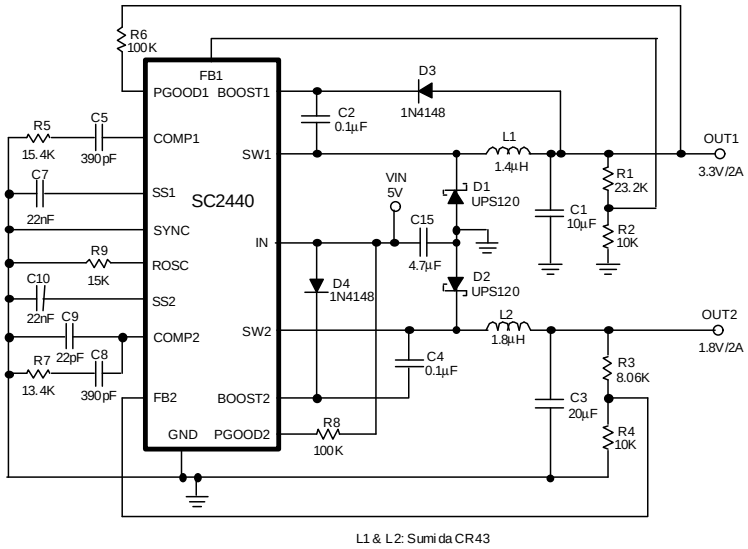
To ensure proper adhesion to the ground plane, avoid using vias directly under the device. In figure 15 two 12mil vias are placed at the edge of the underside pad.



(a) (b)

Figure 16. Suggested PCB Layout for the SC2440. Notice that there is no via directly under the device and that the only component on the backside is the frequency-setting resistor. All vias are 12mil in diameter.

Typical Application Circuits



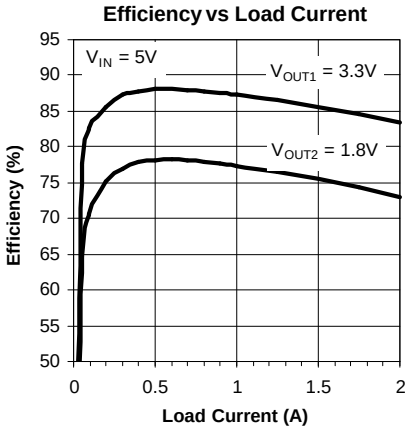
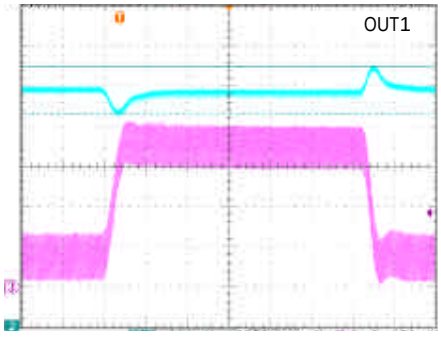


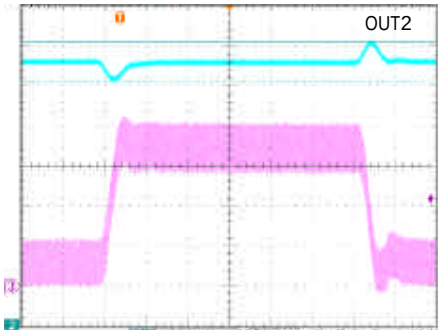
Figure 17(a). 1.3MHz 5V to 3.3V and 1.8V Step-down Converter



20µs/div

Upper Trace : OUT1 Voltage, AC Coupled, 0.2V/div
Lower Trace : L_1 Inductor Current, 0.5A/div

(b)

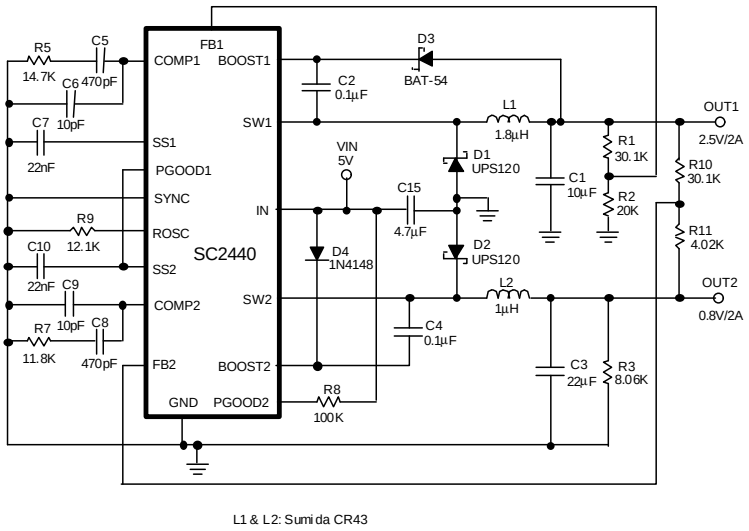


20µs/div

Upper Trace : OUT2 Voltage, AC Coupled, 0.2V/div
Lower Trace : L_2 Inductor Current, 0.5A/div

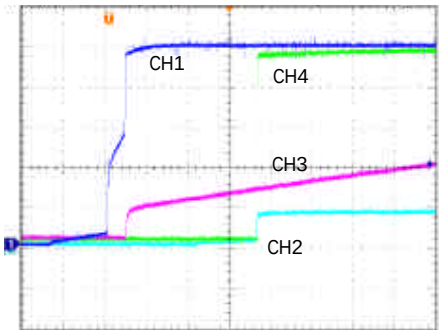
(c)

Figures 17(b) and 17(c). Load Transient Response. I_{OUT} is switched between 0.3A and 1.75A.



L1 & L2: Sumida CR43

Figure 18(a). Producing an Output Lower than FB Voltage. 1.5MHz 5V to 2.5V and 0.8V Step-down Converter R_3 is a pre-load to shunt the current from R_{10} and R_{11} before PGOOD1 releases SS2.



2ms/div

CH1 : OUT1 Voltage, 0.5V/div
CH2 : OUT2 Voltage, 1V/div
CH3 : SS2 Voltage, 1V/div
CH4 : PGOOD2, 1V/div

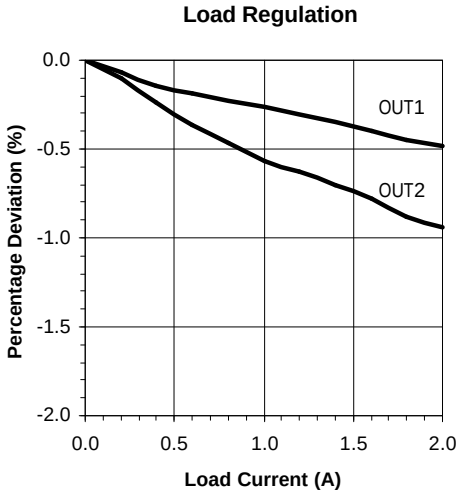


Figure 18(b). V_{IN} Start-up Transient (I_{OUT1} = I_{OUT2} = 1A).

Typical Application Circuits

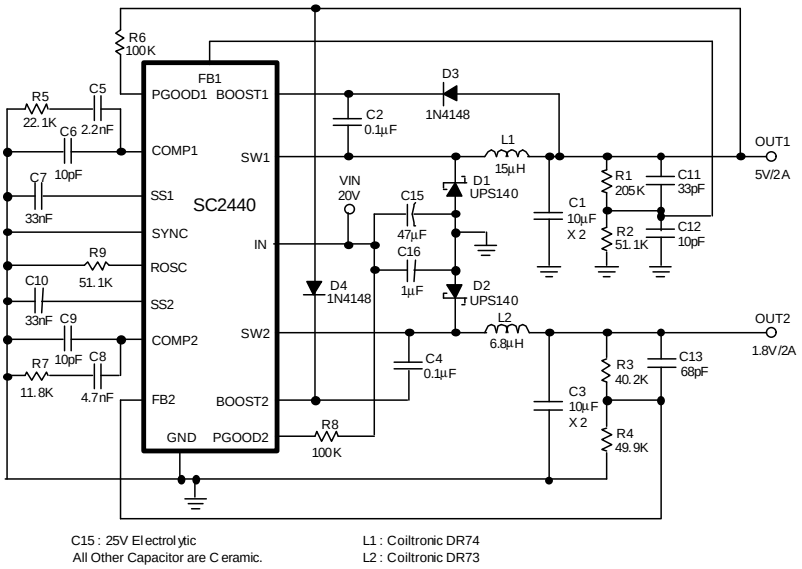
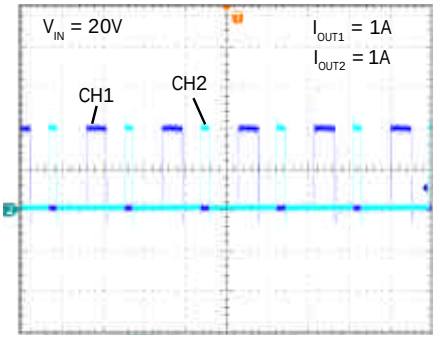


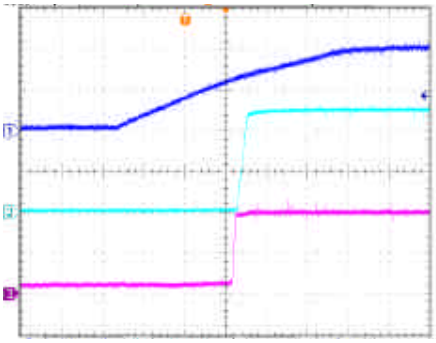
Figure 19(a). 540KHz 20V to 5V and 1.8V Step-down Converter. Notice that Channel 2 is Bootstrapped from OUT1. This Bootstrapping Scheme Requires OUT1 to be Present at All Times (i.e. No Hiccup or Shutdown). Channel 2 will still Run if OUT1 is Absent. However its Power Disspation will be High.



1µs/div

CH1 : SW1 Voltage, 10V/div
CH2 : SW2 Voltage, 10V/div

Figure 19(b). Switching Waveforms.

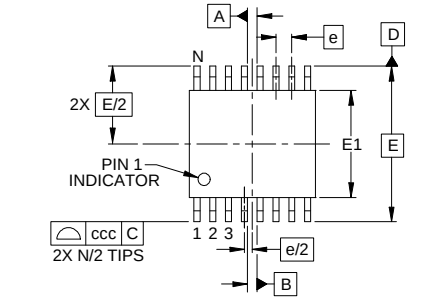


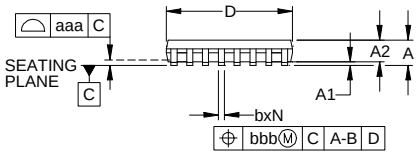
4ms/div

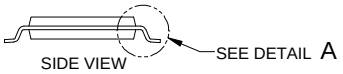
Upper Trace : V_{IN}, 10V/div
Middle Trace : V_{OUT1}, 2V/div
Lower Trace : V_{OUT2} , 1V/div

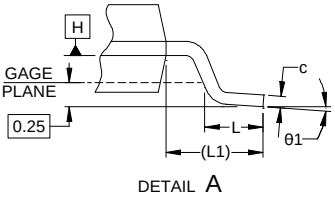
Figure 19(c). V_{IN} Start Up Transient. I_{OUT1}= I_{OUT2}= 1.5A.

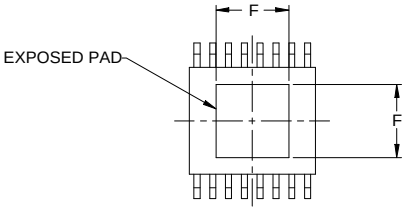
Outline Drawing - TSSOP-16 w/EDP









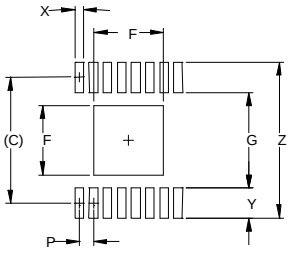


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.193	.197	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
F	.112	.118	.122	2.85	3.00	3.10
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	16			16		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AB.

Land Pattern - TSSOP-16 w/EDP



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.126	3.20
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

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Phone: (805)498-2111 FAX (805)498-3804