SC1218
High Speed Synchronous MOSFET Driver

POWER MANAGEMENT

Description

The SC1218 is a high speed, robust, dual output driver to drive high-side and low-side N-MOSFETs in synchronous buck converters. Combined with Semtech's multi-phase PWM controller SC2649, one can build high performance, versatile voltage regulators for next generation microprocessors.

SC1218 is built upon a CMOS technology which provides enough voltage capacity to handle computer applications. In addition, the advanced timing circuitry is adopted to filter out very narrow PWM pulses at the input of the driver. The latched UVLO and enhanced adaptive shoot-through protection further enhance the robustness of the SC1218.

With integrated bootstrap diode, the SC1218 is offered in both SOIC-8 package and MLPQ-8 3x3mm package. These features further reduce the thermal stress and BOM cost.

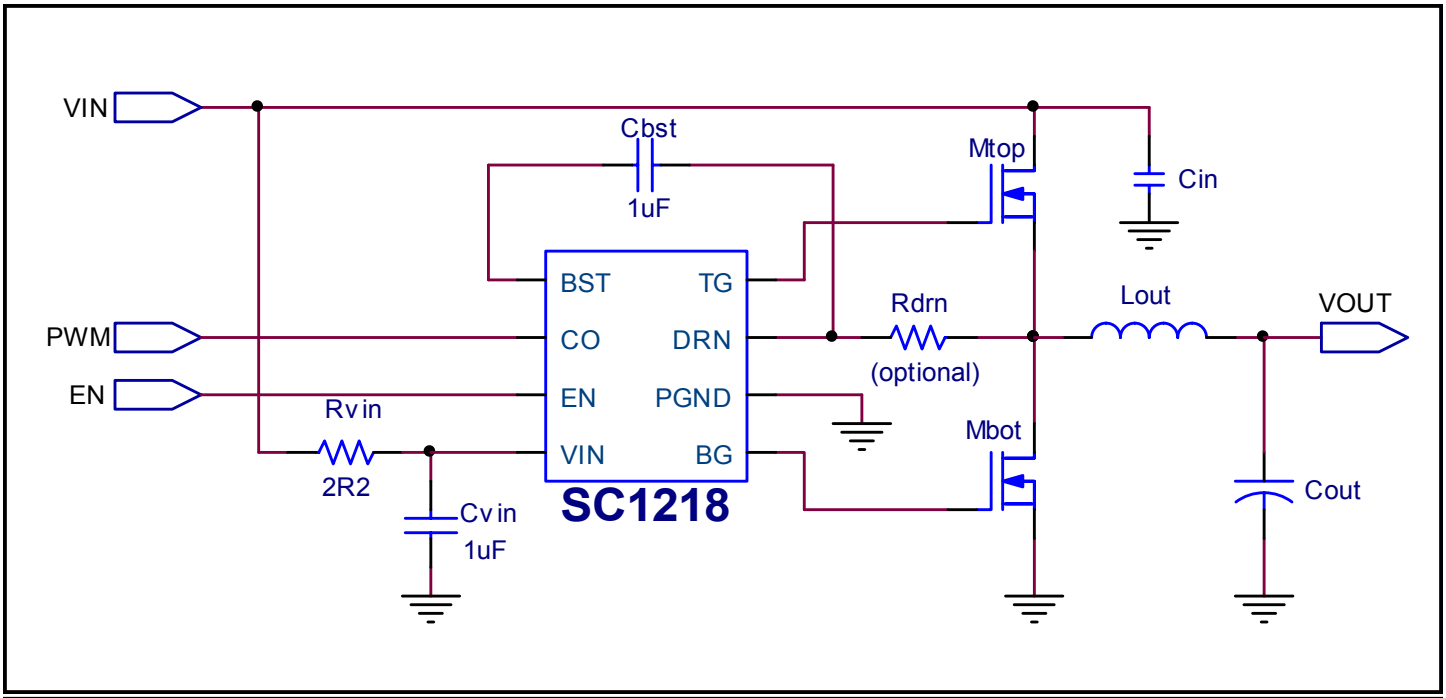
Features

- Advanced Digital Timing to Filter Out Very Narrow PWM Pulses
- +12V Gate Drive Voltage
- Integrated Bootstrap Diode
- High Peak Drive Current
- Adaptive Non-overlapping Gate Drives Provide Shoot-through Protection
- Support Dynamic VID operation
- Ultra-low Propagation Delay
- Floating Top Gate Drive
- Crowbar Function for Over Voltage Protection
- High Frequency (up to 2 MHz) Operation Allows Use of Small Inductors and Low Cost Ceramic Capacitors
- Under Voltage Lockout
- Low Quiescent Current
- Enable Function for Both Gate OFF Shut Down
- Lead-free Part and Fully WEEE and RoHS Compliant

Applications

- Intel® Next Generation Processor Power Supplies
- AMD® Athlon™ and AMD-K8™ Processor Power Supplies
- High Current Low Voltage DC-DC Converters

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V_{IN} Supply Voltage	V_{IN}		-0.3 to 16	V
BST to DRN	$V_{BST-DRN}$		-0.3 to 16	V
BST to V_{IN}	$V_{BST-VIN}$		-0.3 to 16	V
TG to DRN	V_{TG-DRN}		-0.3 to 16	V
TG to DRN Pulse	$V_{TG-DRN-PULSE}$	V_{PEAK} with t_{PULSE} < 20ns(1)	-2	V
BST to PGND	$V_{BST-PGND}$		-0.3 to V_{IN}+16	V
BST to PGND Pulse	$V_{BST-PGND-PULSE}$	t_{PULSE} <20ns	38	V
DRN to PGND	$V_{DRN-PGND}$	V_{BST}-V_{DRN} = 10V	-2 to V_{IN}+16	V
DRN to PGND Pulse	$V_{DRN-PGND-PULSE}$	V_{PEAK} with t_{PULSE} < 200ns(1)	-5 to 35	V
		V_{PEAK} with t_{PULSE} < 20ns(1)	-8 to 35	V
BG to PGND	$V_{BG-PGND}$		-0.3 to V_{IN}+0.3	V
BG to PGND Pulse	$V_{BG-PGND-PULSE}$	V_{PEAK} with t_{PULSE} < 20ns(1)	-3.5	V
PWM Input	CO		-0.3 to V_{IN}+0.3	V
Enable Input	EN		-0.3 to V_{IN}+0.3	V
Continuous Power Dissipation T_A=25°C, T_J=125°C	P_D	SOIC-8	0.5	W
		MLPQ-8	2.56	
Thermal Resistance Junction to Case	θ_{JC}	SOIC-8	40	°C/W
		MLPQ-8	8	
Junction Temperature Range	T_J		0 to 150	°C
Storage Temperature Range	T_{STG}		-65 to 150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	SOIC-8	300	°C
		MLPQ-8	260	°C

Notes:
(1) Pulse width measured at 10% of the triangular spike waveform.
(2) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Electrical Characteristics

Unless specified: T_A = 25°C; V_{IN} = 12V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{IN}		5	12	14	V
V_{IN} Quiescent Current	I_Q	EN=5V; CO=0V		3.35	4.4	mA
		EN=5V; CO=5V		2.9	4	mA
		EN=0V		1.35	2.5	mA

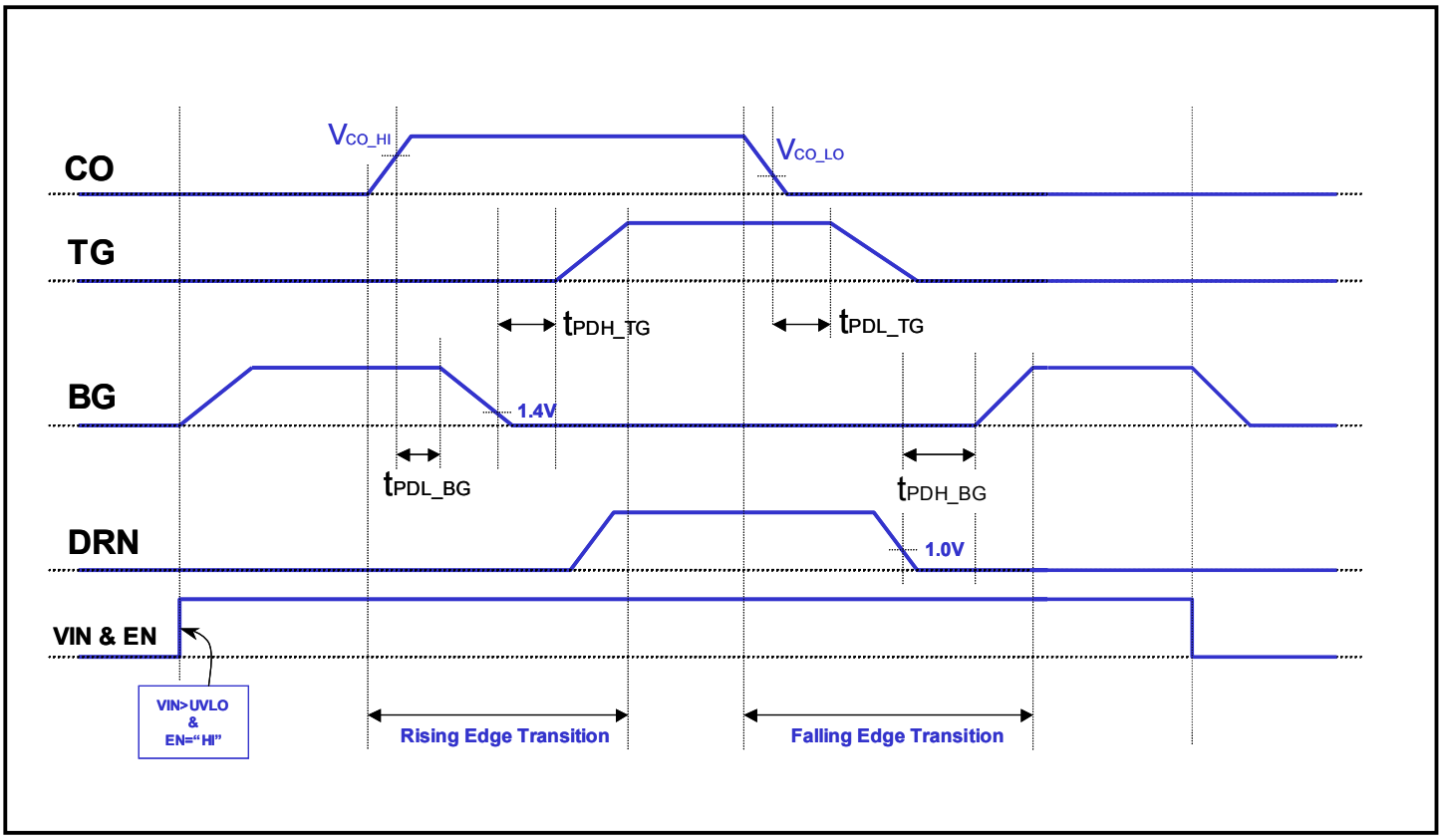
Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C; V_{IN} = 12V.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under Voltage Lockout						
Start Threshold of V_{IN} Voltage	V_{IN_START}			4	4.3	V
Hysteresis	$Vhys_{UVLO}$			250		mV
EN						
Logic High Input Voltage	V_{EN_H}		2.65			V
Logic Low Input Voltage	V_{EN_L}				0.8	V
CO						
Logic High Input Voltage	V_{CO_H}		2.9			V
Logic Low Input Voltage	V_{CO_L}				0.8	V
Internal Pull-down Resistor				40		Kohm
High Side Driver (TG)						
Output Impedence	R_{SRC_TG}	V_{BST}-V_{DRN}= 12V		1.68	2.1	Ohm
	R_{SINK_TG}			0.52	0.78	Ohm
Output Peak Current	$I_{SRC\_TG\_PK}$	V_{IN}=12V, C_{TG}=10nF		2.8		A
	$I_{SINK\_TG\_PK}$	V_{IN}=12V, C_{TG}=10nF		6.5		A
Propagation Delay, TG Going High	t_{PDH_TG}	V_{BST}-V_{DRN}= 12V		37		ns
Propagation Delay, TG Going Low	t_{PDL_TG}	V_{BST}-V_{DRN}= 12V		50		ns
TG Minimum On-time(1)	$t_{ON\_MIN\_TG}$	For CO pulse width < 40ns		40		ns
Low Side Driver (BG)						
Output Impedence	R_{SRC_BG}	V_{IN} = 12V		1.36	2.0	Ohm
	R_{SINK_BG}			0.52	0.78	Ohm
Output Peak Current	$I_{SRC\_BG\_PK}$	V_{IN}=12V, C_{BG}=10nF		3.5		A
	$I_{SINK\_BG\_PK}$	V_{IN}=12V, C_{BG}=10nF		7.5		A
Propagation Delay, BG Going High	t_{PDH_BG}	V_{IN} = 12V		20		ns
Propagation Delay, BG Going Low	t_{PDL_BG}	V_{IN} = 12V		27		ns
BG Minimum OFF-time(1)	$t_{OFF\_MIN\_BG}$	For CO pulse width < 40ns		140		ns
BG Maximum Turn ON Delay(1)	$t_{DH\_MAX\_BG}$	From CO=Low, V_{DRN}>1V		175		ns

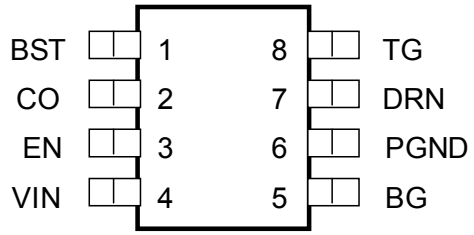
NOTE: (1). Guaranteed by design.

Timing Diagrams

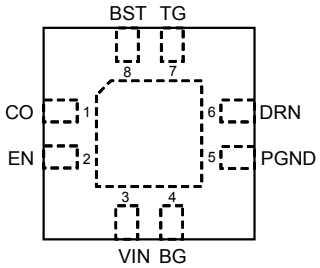


Pin Configuration

SOIC-8 Top View



MLPQ-8 3x3mm Top View



EXPOSED PAD MUST BE SOLDERED TO POWER GROUND PLANE

Pin Descriptions

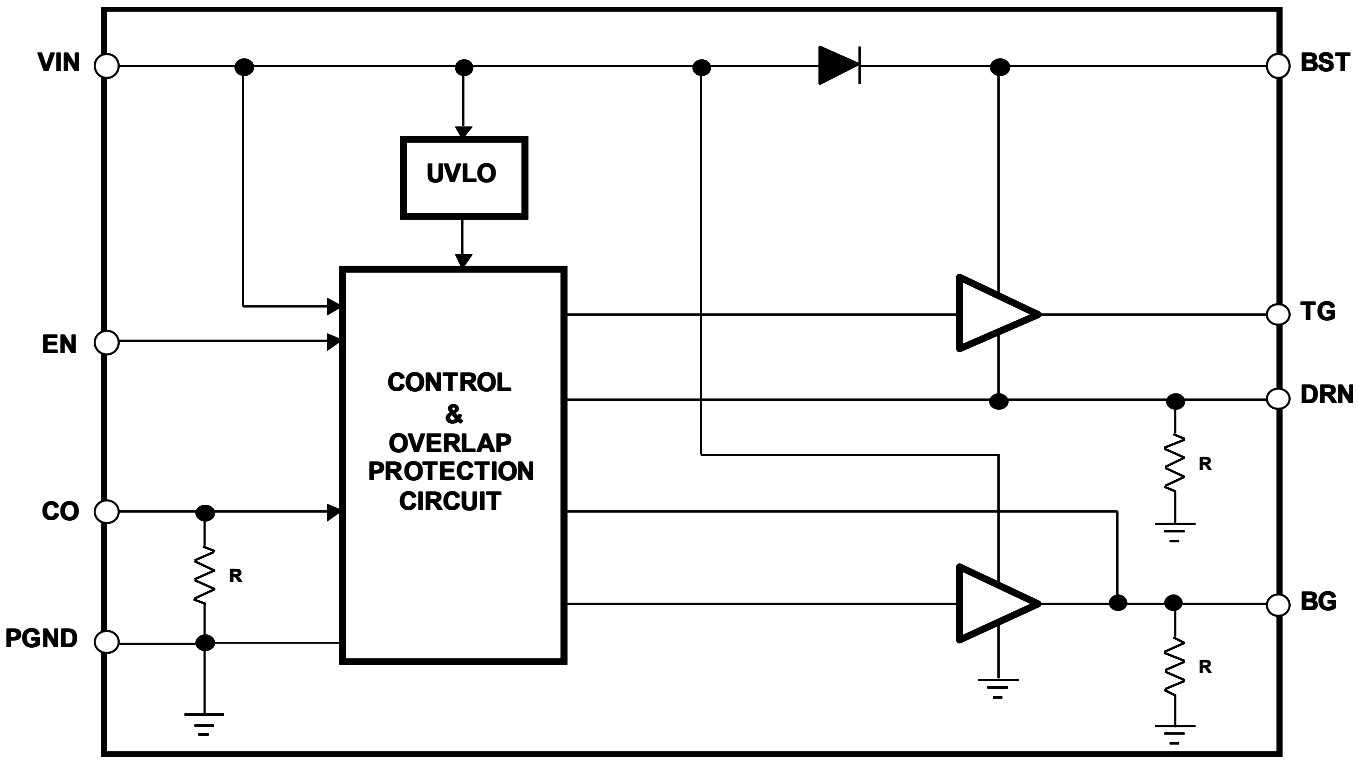
SOIC-8	MLPQ-8	Pin Name	Pin Function
1	8	BST	Bootstrap supply pin for the top gate drive. Connect a 1uF ceramic capacitor between BST and DRN pin to develop a floating bootstrap voltage for the high side driver.
2	1	CO	PWM input signal from external controller. An internal 40Kohm resistor is connected from this pin to the PGND.
3	2	EN	When high, this pin enables the internal circuitry of the device. When low, TG and BG are forced low.
4	3	VIN	Supply power for the bottom gate driver and the internal control circuitry. Connect to input power rail of the converter and dcouple with a 1µF ceramic with lead length no more than 0.2" (5mm).
5	4	BG	Output gate drive for the bottom (synchronous) MOSFET. An internal 20Kohm resistor is connected from this pin to PGND.
6	5	PGND	Supply power ground return. Keep this pin close to the bottom MOSFET source during layout.
7	6	DRN	Connect this pin to the power phase node of the synchronous buck converter (source of top MOSFET and drain of bottom MOSFET). The DRN pin provides a return path for top gate drive. Its voltage is deteced for adaptive shoot-through protection. This pin is subjected to a negative spike of -8V relative to PGND without affecting the operation. An internal 20Kohm resistor is connected from this pin to PGND.
8	7	TG	Output gate drive for the top (switching) MOSFET.

Ordering Information

Device	Package	Temp Range (T_J)
SC1218STRT (1)(3)	SOIC-8	0° to 150°C
SC1218MLTRT (2)(3)	MLPQ-8	0° to 150°C

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Only available in tape and reel packaging. A reel contains 3000 devices.
(3) Devices are lead-free and fully WEEE and RoHS compliant.

Block Diagram



Typical Performance Characteristics

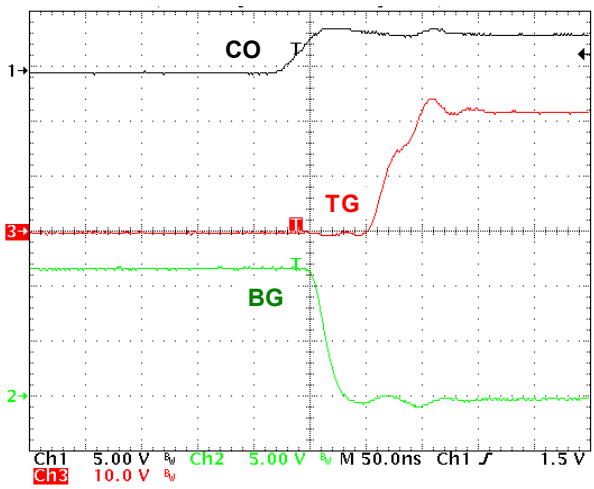


Fig. 1. TG Rise and BG Fall Times

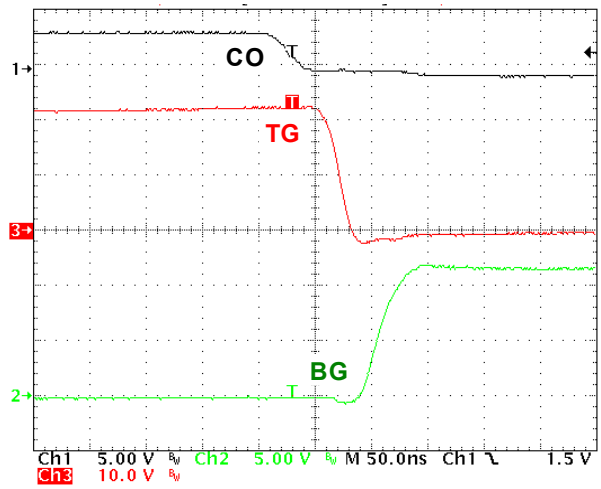


Fig. 2. TG Fall and BG Rise Times

Typical Performance Characteristics (Cont.)

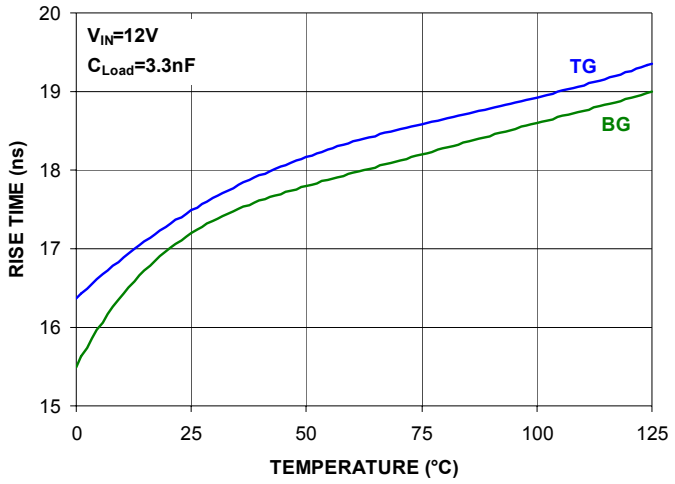


Fig. 3. TG and BG Rise Times vs. Temperature.

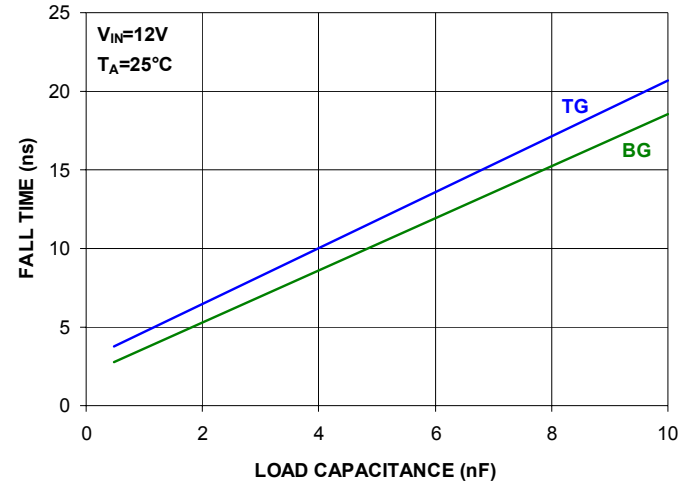


Fig. 6. TG and BG Fall Times vs. Load Capacitance.

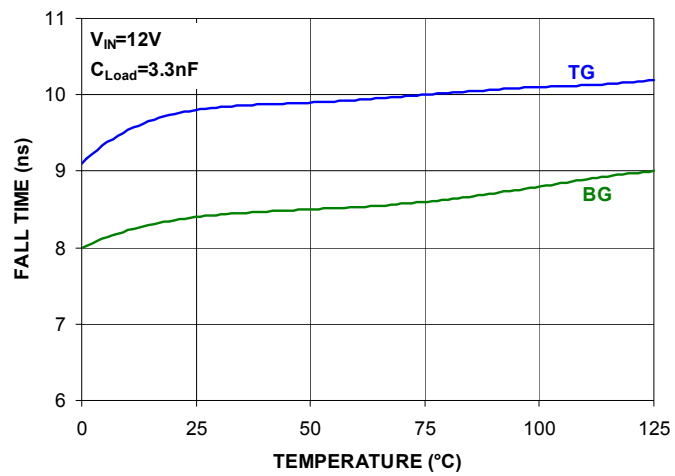


Fig. 4. TG and BG Fall Times vs. Temperature.

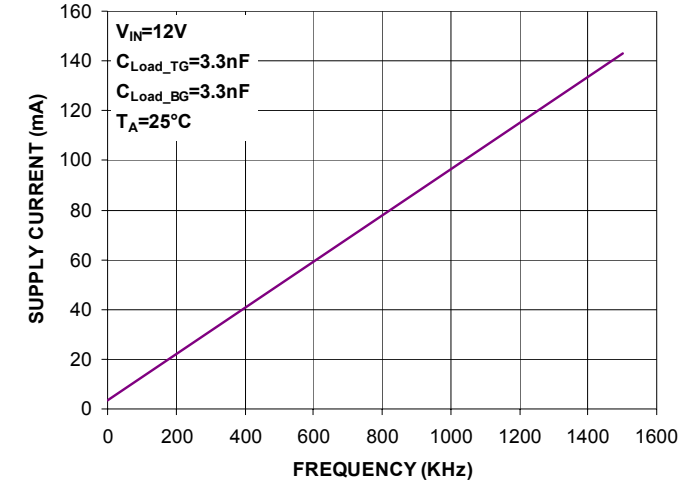


Fig. 7. Supply Current vs. Frequency.

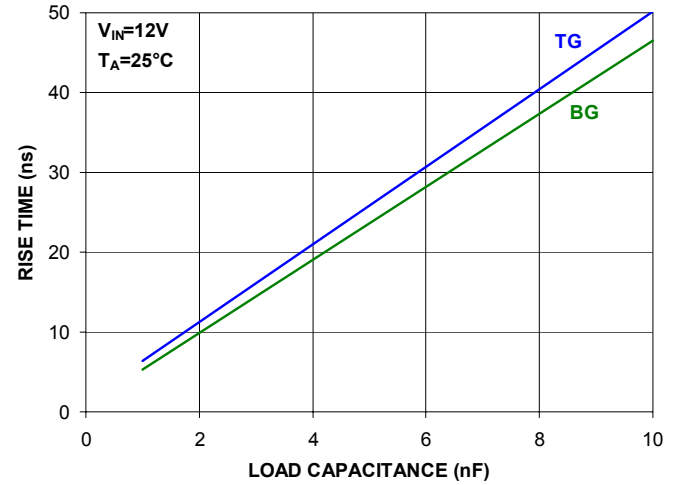


Fig. 5. TG and BG Rise Times vs. Load Capacitance.

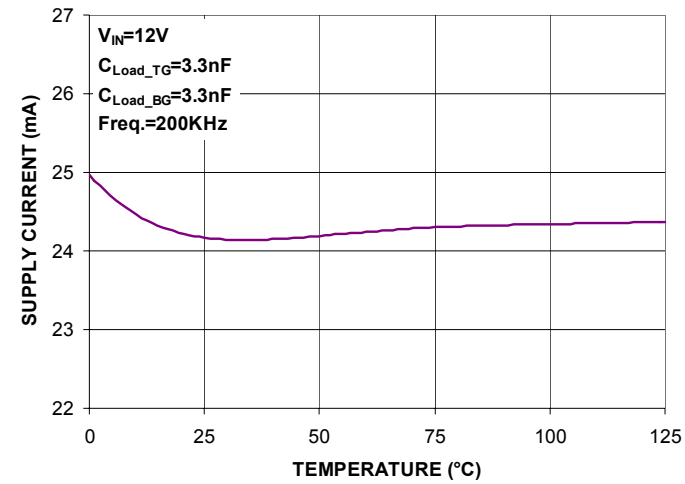


Fig. 8. Supply Current vs. Temperature.

Typical Performance Characteristics (Cont.)

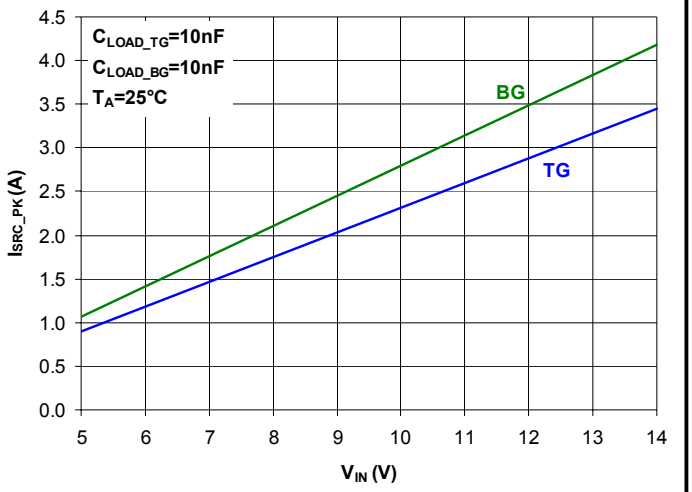


Fig. 9. Peak Sourcing Current vs. Supply Voltage.

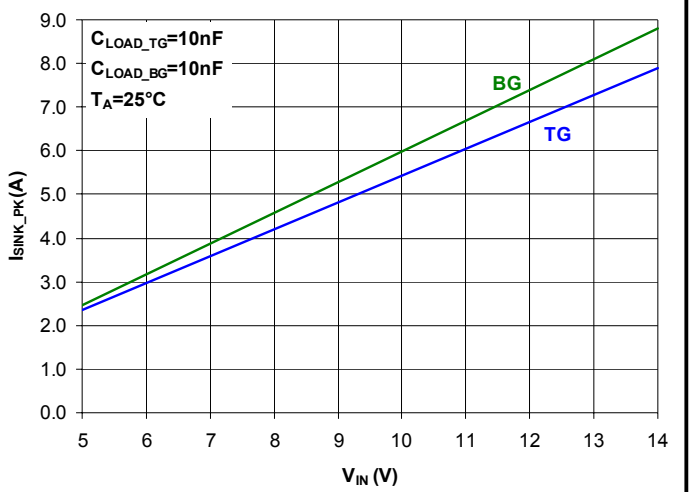


Fig. 10. Peak Sinking Current vs. Supply Voltage.

Applications Information

THEORY OF OPERATION

The SC1218 is a high speed, robust, dual output driver designed to drive top and bottom MOSFETs in a synchronous Buck converter. It features internal bootstrap diode, adaptive delay for shoot-through protection, 12V gate drive voltage, and disable shutdown. It also supports dynamic VID operation and CROWBAR function. This driver combined with PWM controller SC2649 forms a multi-phase voltage regulator for advanced microprocessors.

Startup and UVLO

To startup the driver, a supply voltage is applied to the VIN pin of the SC1218. The top and bottom gates are held low until VIN exceeds the UVLO threshold of the driver, typically 4.0V. The UVLO threshold has hysteresis, typically -250mV, to improve the nosie immunity from the VIN pin.

Gate Transition and Shoot-through Protection

Refer to the Timing Diagrams section, the rising edge of the PWM input initiates the turn-off of bottom FET and the turn-on of top FET. After a short propagation delay (t_{PDL_BG}) from PWM rising edge, the bottom gate falls (t_{F_BG}). The adaptive circuit in the SC1218 detects the bottom gate voltage. It holds the top gate off until the bottom gate voltage drops below 1.4V for a preset delay time (t_{PDH_TG}). This prevents the top FET from turning on until the bottom FET is off. During the transition, the inductor current is freewheeling through the body diode of either bottom FET or top FET, depended on the direction of the inductor current. The phase node could be low (ground) or high (V_{IN}).

The falling edge of the PWM input controls the turn-off of top FET and the turn-on of bottom FET. After a short propagation delay (t_{PDL_TG}) from PWM falling edge, the top gate falls (t_{F_TG}). As the inductor current commutates from the top FET to the body diode of the bottom FET, the phase node falls. The adaptive circuit in the SC1218 detects the phase node voltage. It holds the bottom FET off until the phase node voltage drops below 1.0V. This prevents the top and bottom FETs from conducting simultaneously (shoot-through). If the phase node voltage remains high during the transition for a preset maximum BG turn on delay ($t_{DH\_MAX\_BG}$) , then the bottom gate will be turned on. This supports the CROWBAR function and the sinking current capacity required from dynamic VID operation.

Narrow PWM Pulse Filtering

During a load transient, soft start, or soft shutdown of the voltage regulator, the PWM controller may generate a very narrow pulse for the driver. The pulse is so narrow that it reaches the rising edge threshold of the SC1218 at one point then immediately falls below the falling edge threshold. To prevent the SC1218 from reacting to such narrow PWM pulses, which may cause driver output ringing or shoot through, advanced PWM timing circuitry is added to ease the gate transitions. A minimum off-time (typically 140ns) for the bottom gate and a minimum on-time (typically 40ns) for the top gate are enforced to make the operation safe under such conditions.

Dynamic VID Operation

Some processors changes VID dynamically during operation (Dynamic VID operation). A dynamic VID can occur under light load or heavy load conditions. At light load, it can force the converter to sink current. After turn-off of the top FET, the reversed inductor current flows through the body diode of the top FET instead of the bottom FET. As a result, the phase node voltage remains high and voids the adaptive circuit. SC1218 features a maximum BG turn on delay ($t_{DH\_MAX\_BG}$) to override the adaptive delay to turn the bottom FET on. The preset maximum BG turn on delay time ($t_{DH\_MAX\_BG}$) from the PWM falling egde to the bottom gate turn-on is set to be 175ns.

Switching Frequency, Inductor and MOSFETs

The SC1218 is capable of providing more than 3.5A peak drive current, and operating up to 2MHz PWM frequency without causing thermal stress on the driver. The selection of switching frequency, together with inductor and FETs is a trade-off between the cost, size, and thermal management of a multi-phase voltage regulator. Typically, these parameters could be in the range of:

a) Switching Frequency: 100kHz to 500kHz per phase
b) Inductor Value: 0.2uH to 2uH
c) MOSFETs: 4mOhm to 20mOhm $R_{DS(ON)}$ and 20nC to 100nC total gate charge

Bootstrap and Chip Decoupling Capacitors

The top gate driver of the SC1218 is a DRN refered gate drive whose supply voltage is derived from a bootstrap circuit comprising a capacitor,C_{BST}, and a built-in diode. The capacitor value can be calculated based on the total gate charge of the top FET, Q_{TOP}, and an allowed voltage ripple on the capacitor, ΔV_{BST}, in one PWM cycle:

$$C_{BST} > \frac{Q_{TOP}}{\Delta V_{BST}}$$

Applications Information (Cont.)

Typically, a 1uF/16V ceramic capacitor is used. In addition, a small resistor (one ohm) is recommended in between DRN pin of the SC1218 and the phase node. The resistor is used to alleviate the stress of the SC1218, resulting from the negative spike at the phase node, and also to control the switching speed. A negative spike could occur at the phase node during the top FET turn-off due to parasitic inductance in the switching loop. The spike could be minimized with a careful PCB layout. In the applications with TO-220 package FETs, it is suggested to use a clamping diode on the DRN pin to mitigate the impact of the excessive phase node negative spikes.

For VIN pin of the SC1218, it is recommended to use a 1uF/16V ceramic capacitor for decoupling.

Driver Dissipation and Junction Temperature

The driver power dissipation is a function of chip quiescent current I_Q, switching frequency F_{SW}, and supply voltage V_{IN}. It is approximated as:

$$P_D = (I_Q + Q_{TOTAL} \cdot F_{SW}) \cdot V_{IN}$$

where Q_{TOTAL} is the total gate charge of the top-side and bottom-side FETs. The power dissipation vs total gate charge at the given switching frequency is plotted in Fig.11. The driver junction temperature can be calculated based on the juntion to case thermal resistance and Printed Circuit Board (PCB) temperature.

LAYOUT GUIDELINES

The switching regulator is a high di/dt and dv/dt power circuit. PCB layout is critical. A good layout can achieve optimum circuit performance with minimized component stress, resulting in better system reliability. For a multiphase voltage regulator, the SC1218 driver, FETs, inductor, and supply decoupling capacitors in each phase have to be considered as a unit. For the SC1218 driver, the following guidelines are typically recommended during PCB layout:

a) Place the SC1218 close to the FETs for shortest gate drive traces and ground return paths;
b) Connect decoupling capacitor as close as possible to the VIN pin and the PGND pin. The trace length of the capacitor on the VIN pin should be no more than 0.2" (5mm); and
c) Locate the bootstrap capacitor close to the SC1218.

The typical layout examples of SC1218 based on above guidelines are shown in Fig.12 and Fig.13.

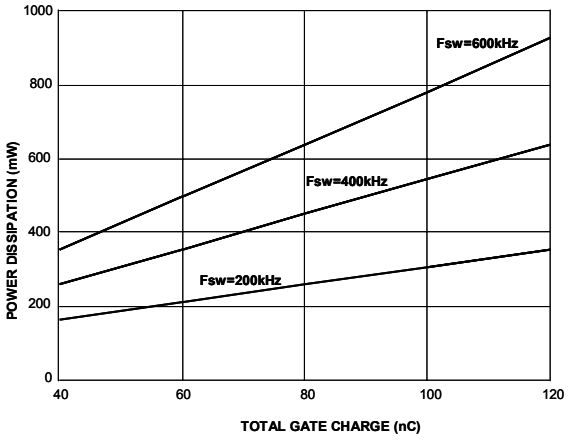


Fig. 11. Power dissipation.

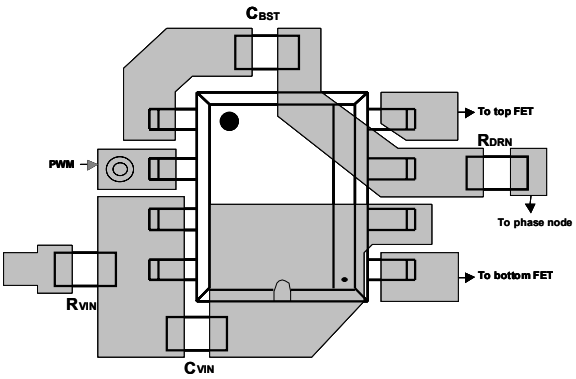


Fig. 12. Component placement for SOIC-8

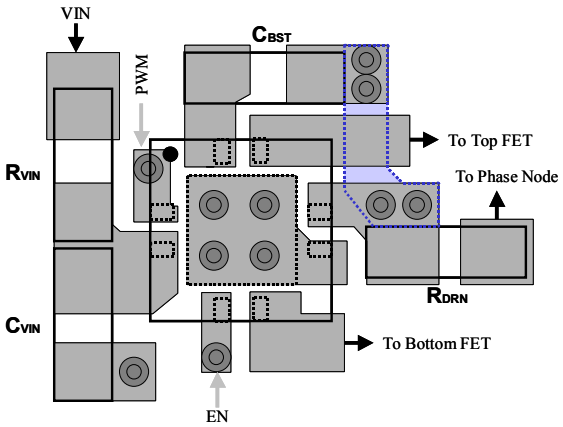
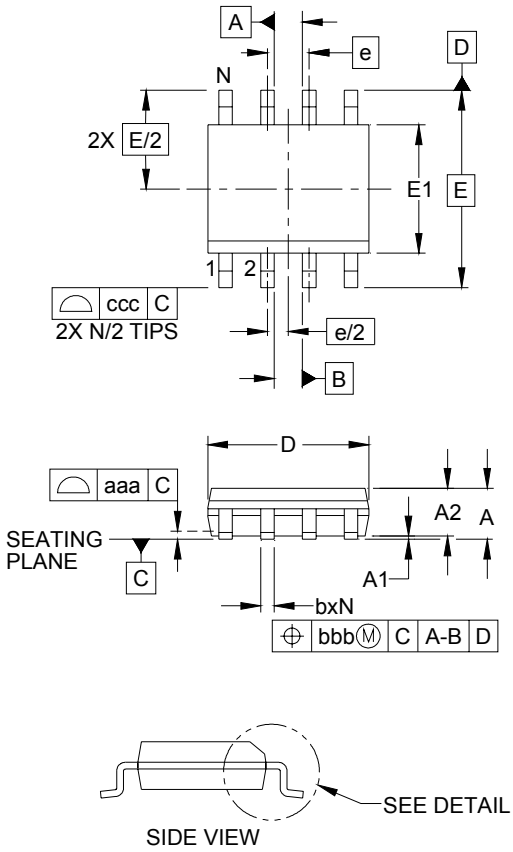


Fig. 13. Component placement for MLPQ-8.

Outline Drawing - SOIC-8

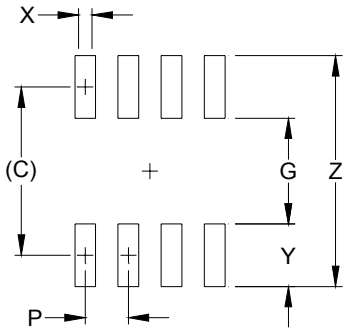


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SOIC-8

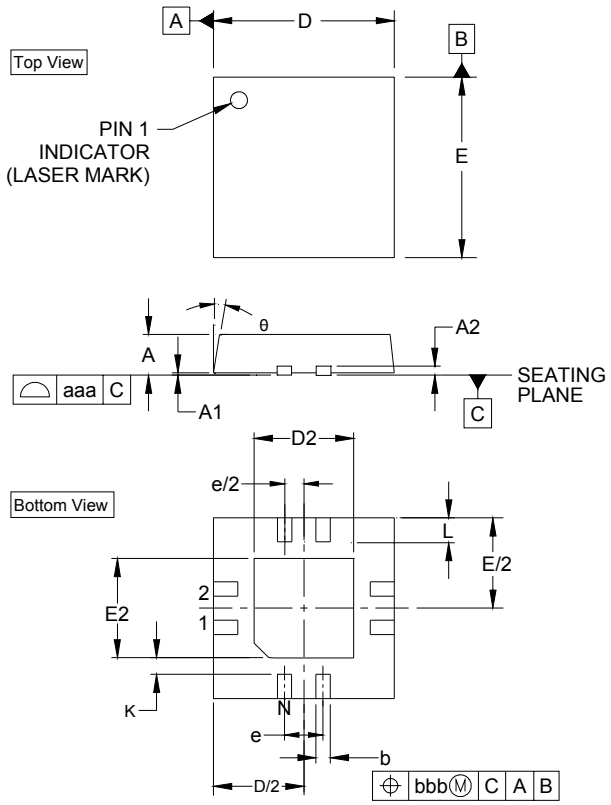


DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

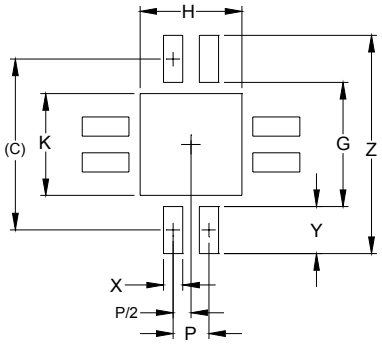
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Outline Drawing - MLPQ-8, 3 x 3mm



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.032	-	.040	0.08	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	.008 BSC			0.20 REF		
b	.007	-	.012	0.19	-	0.30
D	.118 BSC			3.00 BSC		
D2	.059	-	.071	1.50	-	1.80
E2	.059	-	.071	1.50	-	1.80
E	.118 BSC			3.00 BSC		
e	.026 BSC			0.65 BSC		
L	.012	.016	.020	0.30	0.40	0.50
K	.008	-	-	0.20	-	-
N	8			8		
θ	0°	-	12°	0°	-	12°
aaa	.003			0.08		
bbb	.008			0.20		

Land Pattern - MLPQ-8, 3 x 3mm



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.122)	(3.10)
G	.089	2.25
H	.073	1.85
K	.073	1.85
P	.026	0.65
X	.014	0.35
Y	.033	0.85
Z	.156	3.95

NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. THE VIAS ON THE CENTER PAD SHOULD MAINTAIN THE GOOD THERMAL CONTACT OF THE DEVICE TO THE PCB GROUND PLANE.

Contact Information

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