

# XC612 Series

2 Channel Voltage Detectors



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- ◆ CMOS Low Power Consumption
- ◆ 2 Voltage Detectors Built-in
- ◆ Detect Voltage Accuracy :  $\pm 2\%$
- ◆ Detect Voltage Range : 1.5V ~ 5.0V
- ◆ SOT-25 Package

## General Description

The XC612 series consist of 2 voltage detectors, in 1 mini-molded, SOT-25 package.

The series provides accuracy and low power consumption through CMOS processing and laser trimming and consists of a highly accurate voltage reference source, 2 comparators, hysteresis and output driver circuits.

The input ( $V_{IN1}$ ) for voltage detector 1 ( $V_{D1}$ ) dually functions as the power supply pin for both detector 1 ( $V_{D1}$ ) and detector 2 ( $V_{D2}$ ).

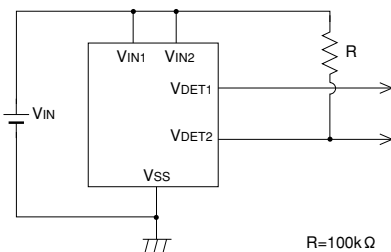
## Applications

- Memory battery back-up circuitry
- Microprocessor reset circuits
- Power failure detection
- System power-on reset circuits
- System battery life monitors and re-charge voltage monitors
- Delay circuitry

## Features

- Highly accurate** : Set-up voltage accuracy  $\pm 2\%$
- Low-power consumption** : Typ. 2.0 $\mu$ A ( $V_{IN1}=V_{IN2}=2.0V$ , quiescent state)
- Detect voltage** : 1.5V ~ 5.0V programmable in 0.1V steps. Detector's voltages can be set-up independently
- Conditionally,  
XC612N :  $V_{DET1} > V_{DET2}$   
XC612D, XC612E :  $V_{DET1} \geq V_{DET2}$ ,  
 $V_{DET1} < V_{DET2}$
- Operating Voltage Range** : 1.0V ~ 10.0V
- Temperature characteristics** :  $\pm 100$ ppm/ $^{\circ}$ C
- Output configuration** : N-channel open drain
- Small package** : SOT-25 (150mW) mini-mold
- \* CMOS Output is under development

## Typical Application Circuit

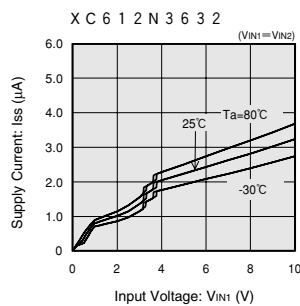


$V_{DET1}$  : CMOS,  $V_{DET2}$  : N-ch Open drain

## Typical Performance

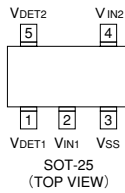
### Characteristic

SUPPLY CURRENT vs. INPUT VOLTAGE



## XC612 Series

### Pin Configuration



### Pin Assignment

PIN NUMBER	PIN NAME	FUNCTION
1	VDET1	Voltage Detector 1 output
2	VIN1	Detector 1 input, Power Supply.
3	VSS	Ground
4	VIN2	Voltage Detector 2 Input
5	VDET2	Voltage Detector 2 Output

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### Product Classification

#### Selection Guide

Type	VDET1	VDET2
XC612N	N-ch Open drain	N-ch Open drain
XC612D	N-ch Open drain	CMOS
XC612E	CMOS	N-ch Open drain

#### Ordering Information

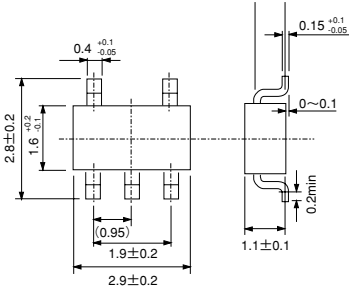
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DESIGNATOR	DESCRIPTION	DESIGNATOR	DESCRIPTION
a	<u>Output Configuration:</u> N=N-Channel Open Drain D=VDET1 N-ch Open Drain, VDET2 CMOS E=VDET1 CMOS, VDET2 N-ch Open Drain	d	<u>Package Type:</u> M=SOT-25
b	<u>Detect Voltage (VDET1)</u> e.g.25=2.5V 38=3.8V	e	<u>Device Orientation</u> R=Embossed Tape (Orientation of Device: Right) L=Embossed Tape (Orientation of Device: Left)
c	<u>Detect Voltage (VDET2)</u> e.g.33=3.3V 50=5.0V		

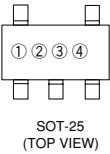
**■Packaging Information**

●SOT-25



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**■Marking**



① Represents the output configuration

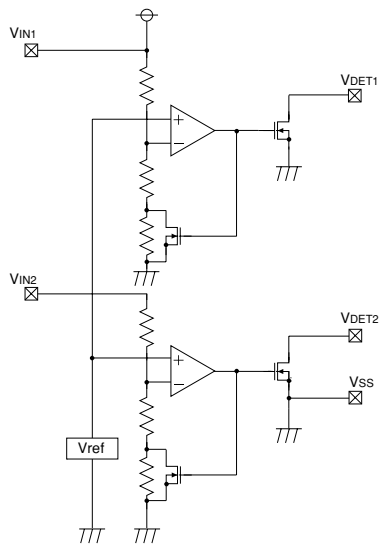
DESIGNATOR	CONFIGURATION		PRODUCT NAME
	V <sub>DET1</sub>	V <sub>DET2</sub>	
N	N-ch Open drain	N-ch Open drain	XC612N****M*
D	N-ch Open drain	CMOS	XC612D****M*
E	CMOS	N-ch Open drain	XC612E****M*

②③ Represents the entry order.  
④ Denotes the production lot number  
0 to 9, A to Z repeated. (G.I.J.O.Q.W excepted)

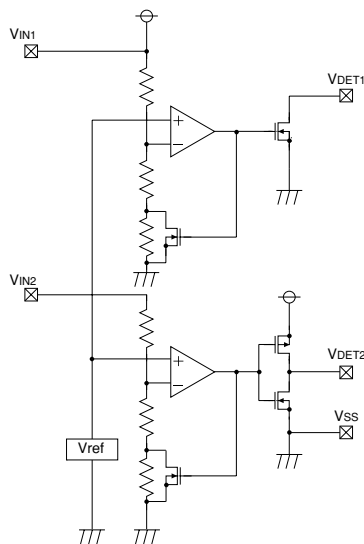
## XC612 Series

### Block Diagram

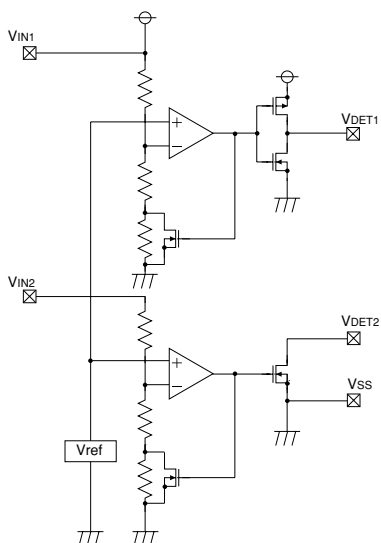
XC612N Series



XC612D Series



XC612E Series



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■ Absolute Maximum Ratings

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	UNITS
Input Voltage VIN1	VIN1	12	V
Input Voltage VIN2	VIN2	12	V
Output Voltage VDET1(N-ch Open drain)	VVDET1	VSS-0.3~12	V
Output Voltage VDET1(CMOS)	VVDET1	VSS-0.3~VIN1+0.3	V
Output Current VDET1	IVDET1	50	mA
Output Voltage VDET2(N-ch Open drain)	VVDET2	VSS-0.3~12	V
Output Voltage VDET2(CMOS)	VVDET2	VSS-0.3~VIN1+0.3	V
Output Current VDET2	IVDET2	50	mA
Power Dissipation	Pd	150	mW
Operating Ambient Temperature	Topr	-30~+80	°C
Storage Temperature	Tstg	-40~+125	°C

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## XC612 Series

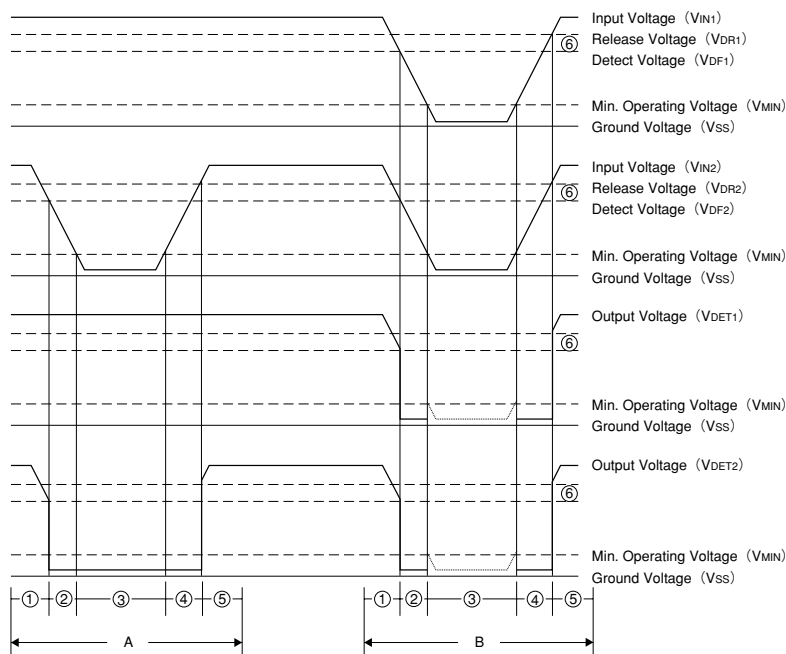
### Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	CIRCUIT
Detect Voltage V <sub>DET1</sub>	V <sub>DF1</sub>	Voltage when V <sub>DET1</sub> changes from H to L following a reduction of V <sub>IN1</sub>	V <sub>DF1</sub> x 0.98	V <sub>DF1</sub>	V <sub>DF1</sub> x 1.02	V	1
Detect Voltage V <sub>DET2</sub>	V <sub>DF2</sub>	Voltage when V <sub>DET2</sub> changes from H to L following a reduction of V <sub>IN2</sub>	V <sub>DF2</sub> x 0.98	V <sub>DF2</sub>	V <sub>DF2</sub> x 1.02	V	1
Hysteresis Range 1	V <sub>HYS1</sub>	Voltage (V <sub>DR1</sub> ) - V <sub>DF1</sub> when V <sub>DET1</sub> changes from L to H following an increase of V <sub>IN1</sub>	V <sub>DF1(T)</sub> x 0.02	V <sub>DF1(T)</sub> x 0.05	V <sub>DF1(T)</sub> x 0.08	V	1
Hysteresis Range 2	V <sub>HYS2</sub>	Voltage (V <sub>DR2</sub> ) - V <sub>DF2</sub> when V <sub>DET2</sub> changes from L to H following an increase of V <sub>IN2</sub>	V <sub>DF2(T)</sub> x 0.02	V <sub>DF2(T)</sub> x 0.05	V <sub>DF2(T)</sub> x 0.08		1
Supply Current (Input Current V <sub>IN1</sub> )	I <sub>SS</sub>	V <sub>IN1</sub> =1.5V 2.0V 3.0V 4.0V 5.0V		1.35 1.50 1.95 2.40 3.00	3.90 4.50 5.10 5.70 6.30	μA	2
Input Current V <sub>IN2</sub>	I <sub>IN2</sub>	V <sub>IN1</sub> =1.5V 2.0V 3.0V 4.0V 5.0V		0.45 0.50 0.65 0.80 1.00	1.30 1.50 1.70 1.90 2.10	μA	2
Operating Voltage	V <sub>IN1</sub>	V <sub>DF</sub> (T) = 1.5V to 6.0V	1.5		10	V	-
Output Current*	I <sub>VDET</sub>	N-ch V <sub>DS</sub> = 0.5V V <sub>IN1</sub> =1.0V V <sub>IN1</sub> =2.0V V <sub>IN1</sub> =3.0V V <sub>IN1</sub> =4.0V V <sub>IN1</sub> =5.0V  P-ch V <sub>DS</sub> = -2.1V V <sub>IN1</sub> =8.0V (CMOS)	0.3 3.0 5.0 6.0 7.0	2.2 7.7 10.1 11.5 13.0		mA	3
Temperature Characteristics*	$\frac{\Delta V_{DF}}{\Delta T_{opr} \cdot V_{DF}}$	-30°C ≤ T <sub>opr</sub> ≤ 80°C		±100	-	ppm/°C	-
Transient Delay Time* (Release Voltage → Output Conversion)	t <sub>DLY</sub>	(V <sub>DR</sub> → V <sub>OUT</sub> conversion)			0.2	ms	5

1. V<sub>DF1(T)</sub>, V<sub>DF2(T)</sub> : User specified detect voltage.
2. Release voltage (V<sub>DR</sub>) = V<sub>DF</sub> + V<sub>HYS</sub>
3. Those parameters marked with an asterisk apply to both V<sub>DET1</sub> and V<sub>DET2</sub>.
4. Input Voltage : please ensure that V<sub>IN1</sub> > V<sub>IN2</sub>  
(Input voltage of XC612D and XC612E series : please ensure that V<sub>IN1</sub> ≥ V<sub>IN2</sub>, V<sub>IN1</sub> < V<sub>IN2</sub>.)
5. V<sub>IN1</sub> pin serve both I<sub>SS</sub> and power supply pin so that V<sub>IN2</sub> operates V<sub>IN1</sub> as a power supply source. For normal operation of V<sub>IN2</sub>, operating voltage higher than the minimum is needed to be applied to power supply pin V<sub>IN1</sub>.
6. For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of V<sub>IN</sub>.

## Operating Explanation

### Timing Chart (Pull up voltage = Input voltage $V_{IN1}$ )



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### Operational Notes (N-ch Open drain)

#### Timing Chart A ( $V_{IN1}$ =voltages above release voltage, $V_{IN2}$ =sweep voltage)

Because a voltage higher than the minimum operating voltage is applied to the voltage input pin ( $V_{IN}$ ), ground voltage will be output at the output pin ( $V_{DET}$ ) during stage 3. (Stages 1, 2, 4, 5 are the same as in B below).

#### Timing Chart B ( $V_{IN1}=V_{IN2}$ )

- ① When a voltage greater than the release voltage ( $V_{DR}$ ) is applied to the voltage input pin ( $V_{IN1}$ ,  $V_{IN2}$ ), input voltage ( $V_{IN1}$ ,  $V_{IN2}$ ) will gradually fall.  
When a voltage greater than the detect voltage ( $V_{DF}$ ) is applied to the voltage input pin ( $V_{IN1}$ ,  $V_{IN2}$ ), a state of high impedance will exist at the output pin ( $V_{DET1}$ ,  $V_{DET2}$ ), so should the pin be pulled up, voltage will be equal to pull up voltage.
- ② When input voltage ( $V_{IN1}$ ,  $V_{IN2}$ ) falls below detect voltage ( $V_{DF}$ ), output voltage ( $V_{DET1}$ ,  $V_{DET2}$ ) will be equal to ground level ( $V_{SS}$ ).
- ③ Should input voltage ( $V_{IN1}$ ,  $V_{IN2}$ ) fall below the minimum operational voltage ( $V_{MIN}$ ), output will become unstable. Should  $V_{IN2}$  fall below  $V_{MIN}$ , voltage at the output pin ( $V_{DET2}$ ) will be equal to ground level ( $V_{SS}$ ) if the power supply ( $V_{IN1}$ ) is within the operating voltage range.  
\*In general the output pin is pulled up so output will be equal to pull up voltage.
- ④ Should input voltage ( $V_{IN1}$ ,  $V_{IN2}$ ) rise above ground voltage ( $V_{SS}$ ), output voltage ( $V_{DET1}$ ,  $V_{DET2}$ ) will equal ground level until the release voltage level ( $V_{DR}$ ) is reached.
- ⑤ When input voltage ( $V_{IN1}$ ,  $V_{IN2}$ ) rises above release voltage, the output pin's ( $V_{DET1}$ ,  $V_{DET2}$ ) voltage will be equal to the voltage dependent on pull up.

Note : The difference between release voltage ( $V_{DR}$ ) and detect voltage ( $V_{DF}$ ) is the Hysteresis Range ⑥.

## XC612 Series

### Directions for use

#### Notes on Use

1. Please use this IC within the specified maximum absolute ratings.
2. Please ensure that input voltage  $V_{IN2}$  is less than  $V_{IN1} + 0.3V$ . (refer to N.B. 1 below)
3. With a resistor connected between the  $V_{IN1}$  pin and the input, oscillation is liable to occur as a result of through current at the time of release. (refer to N.B. 2 below)
4. With a resistor connected between the  $V_{IN1}$  pin and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the  $V_{IN1}$  pin.
5. In order to stabilise the IC's operations, please ensure that the  $V_{IN1}$  pin's input frequency's rise and fall times are more than  $5 \mu \text{ sec/V}$ .
6. Should the power supply voltage  $V_{IN1}$  exceed 6V, voltage detector 2's detect voltage ( $V_{DF2}$ ) and the release voltage ( $V_{DR2}$ ) will shift somewhat.
7. For CMOS output products, high level output voltage which is generated when the transient response is released becomes input voltage of  $V_{IN}$ .

#### N.B.

1. Voltage detector 2's input voltage ( $V_{IN2}$ )  
An input protect diode is connected from input detector 2's input ( $V_{IN2}$ ) to input detector 1's input. Therefore, should the voltage applied to  $V_{IN2}$  exceed  $V_{IN1}$ , current will flow through  $V_{IN1}$  via the diode. (refer to diagram 1)
2. Oscillation as a result of through current  
Since the XC612 series are CMOS ICs, through current will flow when the IC's internal circuit switching operates (during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor ( $R_{IN}$ ) during release voltage operations. (refer to diagram 2)  
Since hysteresis exists during detect operations, oscillation is unlikely to occur.

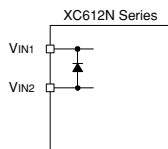


Diagram 1. Voltage detector 2's input voltage  $V_{IN2}$

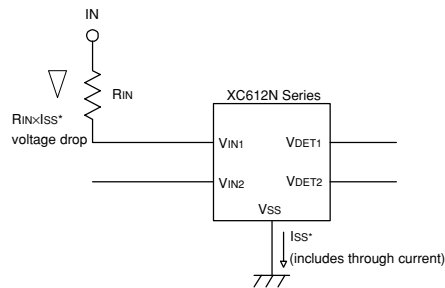
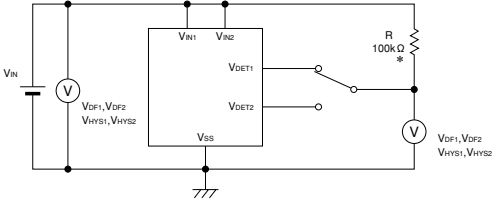


Diagram 2. Through current oscillation



**Test Circuits**

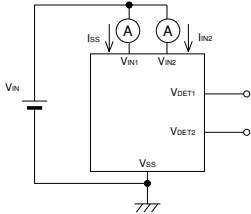
Circuit 1.



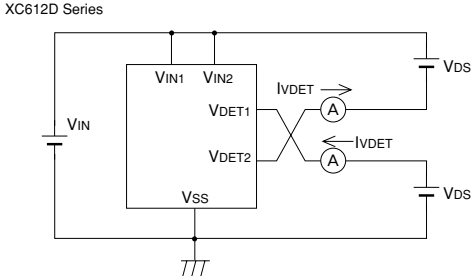
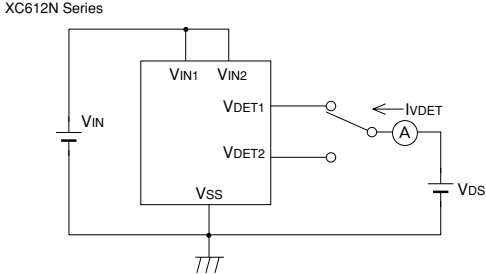
\* A resistor is not needed if the product is CMOS output type.

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Circuit 2.

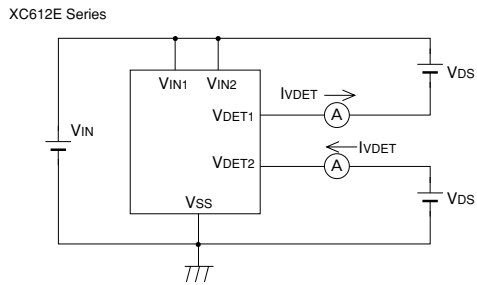


Circuit 3.

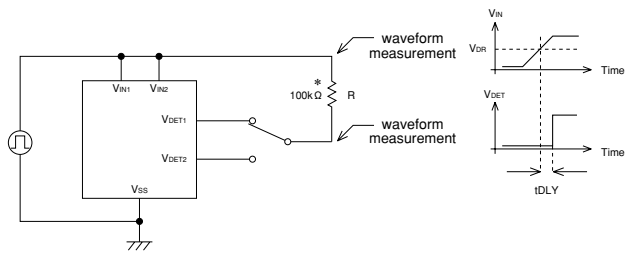


## XC612 Series

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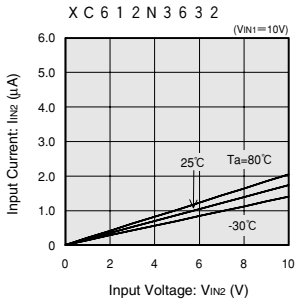
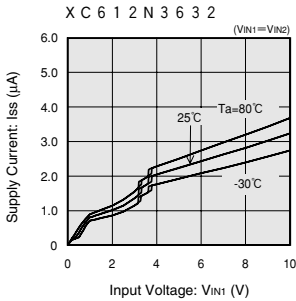


Circuit 4.



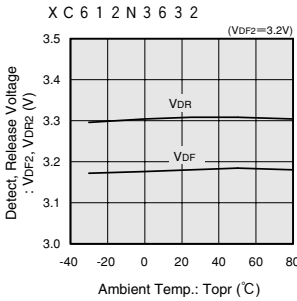
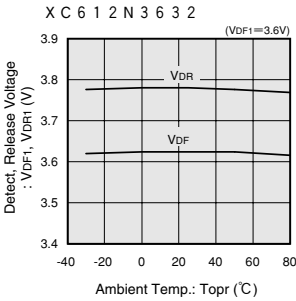
**Typical Performance Characteristics**

(1) SUPPLY CURRENT vs. INPUT VOLTAGE



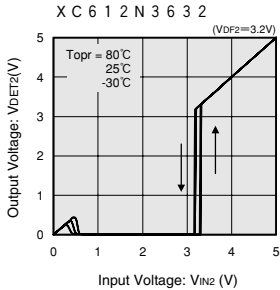
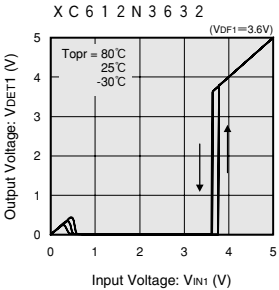
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(2) DETECT & RELEASE VOLTAGE vs. AMBIENT TEMPERATURE



Note : Unless otherwise stated, pull up resistance = 100kΩ with N-ch open drain output types.

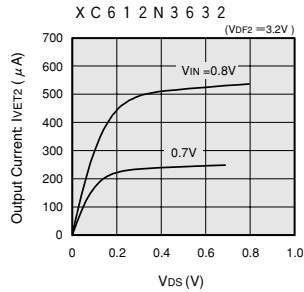
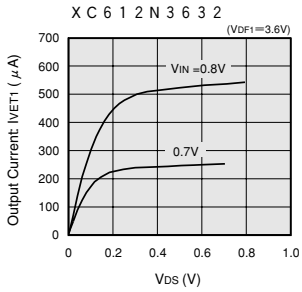
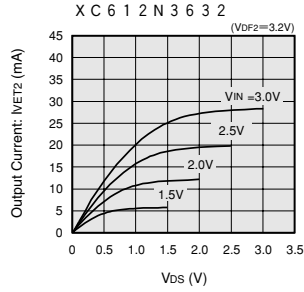
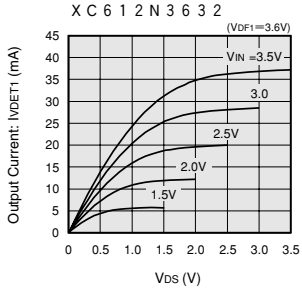
(3) OUTPUT VOLTAGE vs. INPUT VOLTAGE



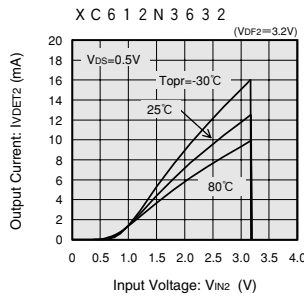
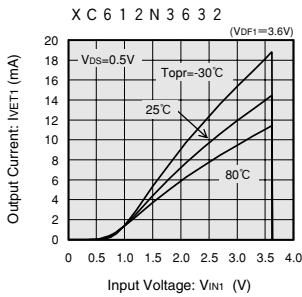
# XC612 Series

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(4) N-CH DRIVER OUTPUT CURRENT vs.  $V_{ds}$

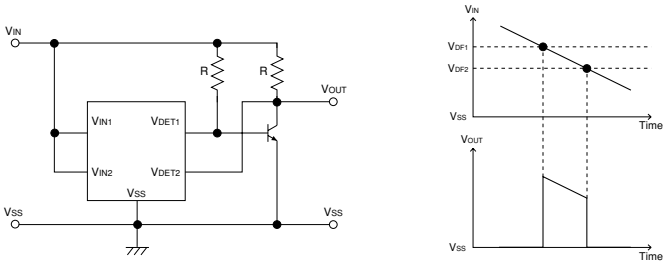


(5) N-CH DRIVER OUTPUT CURRENT vs. INPUT VOLTAGE



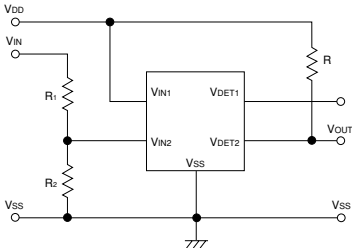
**Typical Application Circuits**

●Window comparator circuit (Example covers N-channel open drain product's circuits.)



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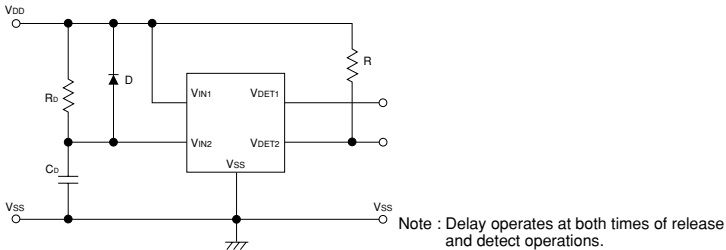
●Detect voltages above respective established voltages circuit (Example covers N-channel open drain product's circuits.)



Notes on resistors R1 and R2's (1), (2) functions :  
 Detect voltage =  $\{ (R1 + R2) + R2 \} \times V_{DF2}$  (1)  
 N.B.  $V_{DF2}$  = detect voltage VD2  
 Please set-up so that  
 Hysteresis ( $V_{HYS2}$ ) =  $\{ (R1 + R2) \div \}$   $\times V_{HYS2}$  (2)

Note : Please ensure that input voltage 2 ( $V_{IN2}$ ) is less than  $V_{IN1} + 0.3V$

●Voltage detect circuit with delay built-in (Example covers N-channel open drain product's circuits.)



Note : Delay operates at both times of release and detect operations.