National Semiconductor

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LMC272
CMOS Dual Low Cost Rail to Rail Output Operational Amplifier

General Description

The LMC272 is a CMOS dual operational amplifier with rail-to-rail output swing and an input common voltage range that extends below the negative supply. Other performance characteristics include low voltage operation, low bias current, excellent channel-to-channel isolation, good bandwidth performance and a competitive price.

These devices are available in MSOP package which is about half the size of a SO-8 device. This enables the designer to fit the device in extremely small applications.

The LMC272C is a direct replacement for TLC272C with performance which meets or exceeds the TLC272C's guaranteed limits in the commercial temperature range when operating from a supply of 2.7V to 15V (see Electrical Characteristics table for details).

These features make this cost effective device ideal for new designs as well as for upgrading existing designs. Applications include hand-held analytic instruments, transducer amplifiers, sample and hold circuits, etc.

Features

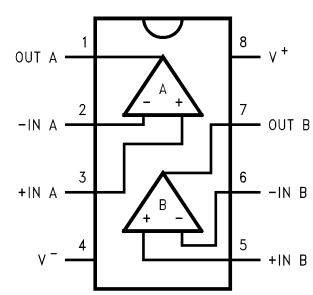
(Typical unless otherwise noted) V_S = 5V, T_A = 25˚C

- Output Swing to within 60 mV of supply rail (10 kΩ load)
- High voltage gain: 90 dB
- Unity gain-bandwidth: 2.0 MHz
- Wide supply voltage: 2.7V to 15V
- Characterized for: 2.7V, 5V, 10V
- Low supply current: 0.975 mA/amplifier
- Input voltage range: −0.3V to 4.2V

Applications

- Portable instruments
- Upgrade for TLC272C and TS272C
- Photodetector preamplifiers
- D/A converters
- Filters

Connection Diagram



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Top View

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied as
8-pin Molded DIP	LMC272CN	N08E	LMC272CN	Rails
8-pin SO-8	LMC272CM	M08A	LMC272CM	Rails
	LMC272CMX	M08A	LMC272CM	2.5k Tape and Reel
MSOP	LMC272CMM	MUA08A	A07	Rails
	LMC272CMMX	MUA08A	A07	3k Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	±Supply Voltages
Voltage at Input/Output Pin	(V^+)+0.3V, (V^-)−0.3V
Supply Voltage ($V^+ - V^-$):	16V
Current at Input Pin (Note 10)	±5 mA
Current at Output Pin (Note 3) (Note 7)	±30 mA
Lead Temperature (soldering, 10 sec.)	260˚C
Storage Temp. Range	−65˚C to +150˚C
Junction Temperature (Note 4)	150˚C

Operating Ratings (Note 1)

Supply Voltage	2.5V ≤ V_S ≤ 15V
Junction Temperature Range	
LMC272C	0˚C ≤ T_J ≤ +70˚C
Thermal Resistance (θ_{JA})	
N Package, 8-pin Molded DIP	115˚ C/W
M Package, 8-pin Surface Mount	177˚ C/W
MSOP Package	235˚ C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$, R_L to ground, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_O = 1.4V, R_S = 50, V_{CM} = 0V, R_L = 10k	1.40	7 **9**	mV max
TCV_{OS}	Temp. Coefficient of Input Offset Voltage	T_A = 0˚C to 70˚C	**3.9**		µV/˚C
I_B	Input Bias Current		1	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
CMRR	Common Mode Rejection Ratio	V_{CM} = −0.2V to 1.2V	77	65 **60**	dB min
PSRR	Power Supply Rejection Ratio	V+ = 2.7V to 5V, V_O = 1.4V	75	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	1.7	1.5 **1.2**	V min
			−0.3	−0.2 **−0.2**	V max
A_V	Large Signal Voltage Gain	V_O = 0.25V to 2.45V, R_L = 10k	88		dB
V_O	Output Swing	R_L = 10 kΩ, V_{ID} = 100 mV (Note 11)	2.64	2.55	V min
		V_{ID} = −100 mV (Note 11)	0	20 **25**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Note 11)	3.7		mA
		Sinking, V_{ID} = −100 mV (Note 11)	2.5		mA
I_S	Total Supply Current		1.60	2.5 **3.0**	mA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$, R_L to ground and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
SR	Slew Rate (Note 8)	$A_V = +1$, $R_L = 10\ k\Omega$, VI = 1 V_{PP}, $C_L = 20\ pF$ (Note 12)	1.7		V/µs
GBW	Unity Gain Frequency	VI = 10 mV_{PP}, $C_L = 20\ pF$ (Note 12)	1.9		MHz
ϕ_m	Phase Margin	VI = 10 mV_{PP}, $C_L = 20\ pF$ (Note 12)	39		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz, $R_S = 20\Omega$	27		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0015		$\frac{pA}{\sqrt{Hz}}$
f_{max}	Full Power Bandwidth	$V_S = 10V$, $C_L = 20\ pF$, $R_L = 20\ k\Omega$	120		kHz
	Amp-to-Amp Isolation	(Note 9)	150		dB
THD	Total Harmonic Distortion	$A_V = +1$, $V_{IN} = 0.7V_{PP}$ f = 1 kHz	0.035		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, R_L to ground and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_O = 1.4V, R_S = 50, R_L = 10k, V_{CM} = 0V	1.75	7 **9**	mV max
TCV_{OS}	Temp. Coefficient of Input Offset Voltage	T_A = 0˚C to 70˚C	**3.3**		µV/˚C
I_B	Input Bias Current		1	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
CMRR	Common Mode Rejection Ratio	V_{CM} = −0.2V to 3.5V	77	65 **60**	dB min
PSRR	Power Supply Rejection Ratio	V+ = 5V to 10V, V_O = 1.4V	88	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	4.2	4 **3.5**	V min
			−0.3	−0.2 **−0.2**	V max
A_V	Large Signal Voltage Gain	V_O = 0.25V to 2V, R_L = 10k	90	80 **72**	dB min
V_O	Output Swing	R_L = 10 kΩ, V_{ID} = 100 mV (Note 11)	4.94	4.85 **4.75**	V min
		V_{ID} = −100 mV (Note 11)	0	20 **25**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Note 11)	16		mA
		Sinking, V_{ID} = −100 mV (Note 11)	16		mA
I_S			1.95	3.2 **3.6**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, R_L to ground and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
SR	Slew Rate (Note 8)	A_V = +1, R_L = 10 kΩ, VI = 1 V_{PP}, C_L = 20 pF (Note 12)	2.5		V/µs
		A_V = +1, R_L = 10 kΩ, VI = 2.5 V_{PP}, C_L = 20 pF (Note 12)	2.5		
GBW	Unity Gain Frequency	VI = 10 mV, C_L = 20 pF (Note 12)	2.0		MHz
ϕ_m	Phase Margin	VI = 10 mV, C_L = 20 pF (Note 12)	43		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz, R_S = 20Ω	25		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0015		$\frac{pA}{\sqrt{Hz}}$
f_{max}	Full Power Bandwidth	V_S = 10V, C_L = 20 pF, R_L = 20 kΩ	120		kHz
	Amp-to-Amp Isolation	(Note 9)	150		dB
THD	Total Harmonic Distortion	A_V = +1, V_{IN} = 2.5 V_{PP} f = 1 kHz	0.015		%

10V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = V^+/2, R_L to ground and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_O = 1.4V, R_S = 50, R_L = 10k, V_{CM} = 0V	2.1	7 **9**	mV max
TCV_{OS}	Temp. Coefficient of Input Offset Voltage	T_A = 0˚C to 70˚C	**3.6**		µV/˚C
I_B	Input Bias Current		1	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
CMRR	Common Mode Rejection Ratio	V_{CM} = −0.2V to 8.5V	77	65 **60**	dB min
PSRR	Power Supply Rejection Ratio	V+ = 5V to 10V, V_O = 1.4V	88	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	9.2	9 **8.5**	V min
			−0.3	−0.2 **−0.2**	V max
A_V	Large Signal Voltage Gain	V_O = 1V to 6V, R_L = 10k	95	85 **78**	dB min
V_O	Output Swing	R_L = 10 kΩ, V_{ID} = 100 mV (Note 11)	9.93	9.85 **9.75**	V min
		V_{ID} = −100 mV (Note 11)	33	45 **50**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Note 11)	55		mA
		Sinking, V_{ID} = −100 mV (Note 11)	25		mA
I_S	Total Supply Current		2.25	3.6 **4.0**	mA max

10V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = $V^+/2$, R_L to ground and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC272C Limit (Note 6)	Units
SR	Slew Rate (Note 8)	A_V = +1, R_L = 10 kΩ, VI = 1 V_{PP}, C_L = 20 pF (Note 12)	2.65		V/µs
		A_V = +1, R_L = 10 kΩ, VI = 5.5 V_{PP}, C_L = 20 pF (Note 12)	2.65		
GBW	Unity Gain Frequency	VI = 10 mV, C_L = 20 pF (Note 12)	2.1		MHz
ϕ_m	Phase Margin	VI = 10 mV, C_L = 20 pF (Note 12)	44		Deg
e_n	Input-Referred Voltage Noise	f = 1 kHz, R_S = 20Ω	25		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0015		$\frac{pA}{\sqrt{Hz}}$
f_{max}	Full Power Bandwidth	C_L = 20 pF, R_L = 20 kΩ	120		kHz
	Amp-to-Amp Isolation	(Note 9)	150		dB
THD	Total Harmonic Distortion	A_V = +1, V_{IN} = 5 V_{PP} f = 1 kHz	0.005		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Do not short circuit output to V+, when V+ is greater than 13V or reliability will be adversely affected.

Note 8: Slew rate is the slower of the rising and falling slew rates.

Note 9: Input referred, V+ = 10V and R_L = 100 kΩ connected to 5V. Each amp excited in turn with 1 kHz to produce about 10 V_{PP} output.

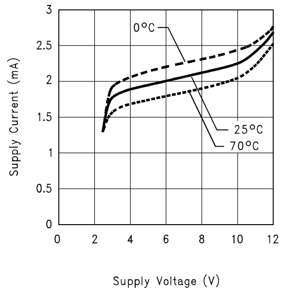
Note 10: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 11: V_{ID} is the differential voltage on the non-inverting input with respect to the inverting input.

Note 12: V_I is the input voltage.

Typical Performance Characteristics (V_S = +5V, single supply, T_A = 25˚C, and R_L to ground unless otherwise specified)

Supply Current vs Supply Voltage



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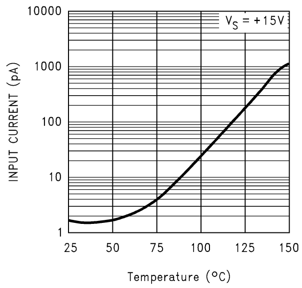
Input Current vs Temperature



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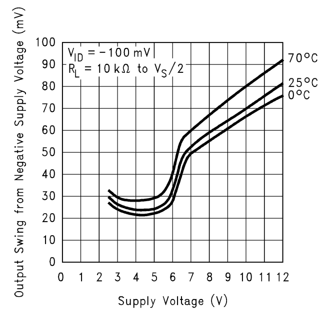
Negative Output Voltage Swing vs Supply Voltage



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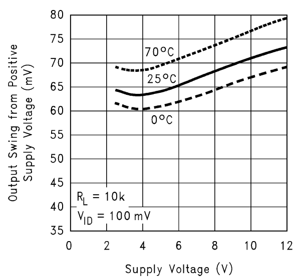
Positive Output Voltage Swing vs Supply Voltage



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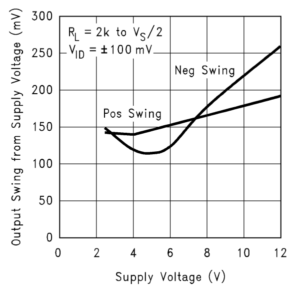
Output Voltage Swing vs Supply Voltage



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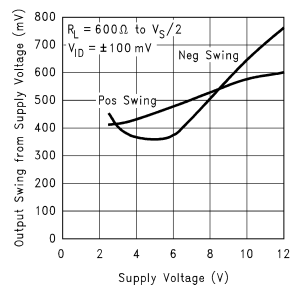
Output Voltage Swing vs Supply Voltage



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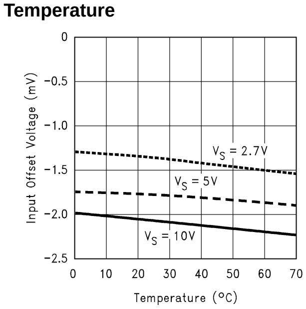
Input Offset Voltage vs Temperature



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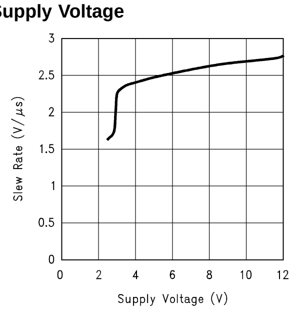
Slew Rate vs Supply Voltage



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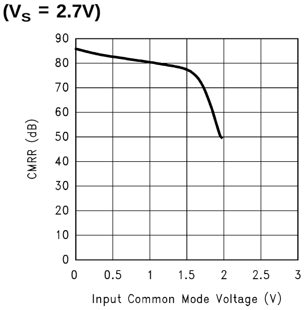
CMRR vs Input Common Mode Voltage (V_S = 2.7V)



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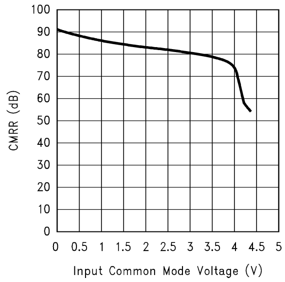
Typical Performance Characteristics (V_S = +5V, single supply, T_A = 25˚C, and R_L to ground unless otherwise specified) (Continued)

CMRR vs Input Common Mode Voltage (V_S = 5V)



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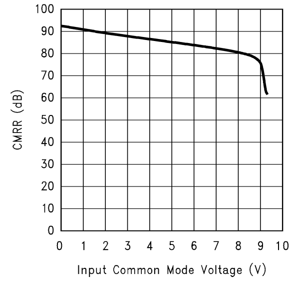
CMRR vs Input Common Mode Voltage (V_S = 10V)



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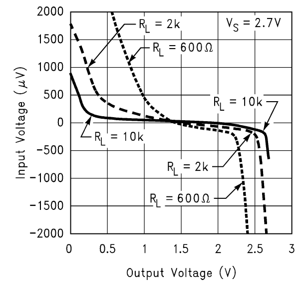
Input Voltage vs Output Voltage



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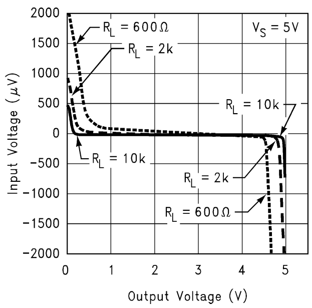
Input Voltage vs Output Voltage



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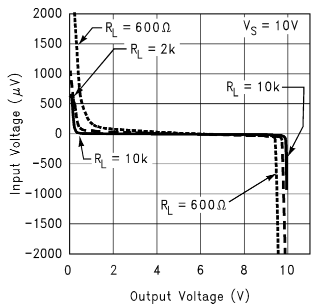
Input Voltage vs Output Voltage



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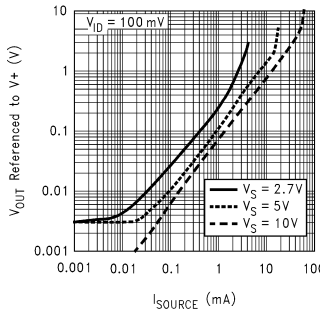
Sourcing Current vs Output Voltage



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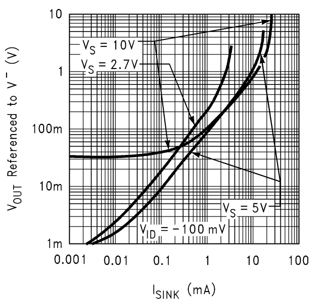
Sinking Current vs Output Voltage



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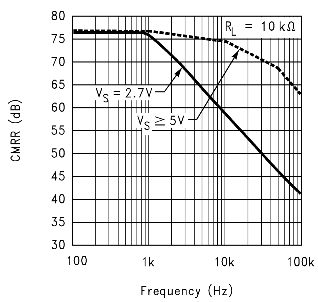
CMRR vs Frequency



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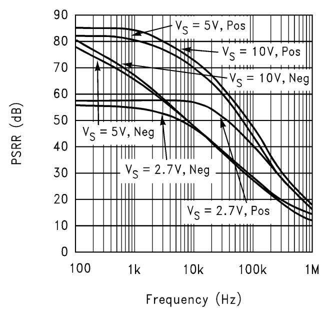
PSRR vs Frequency



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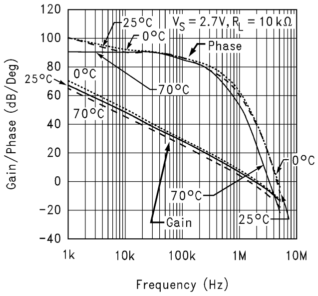
Typical Performance Characteristics (V_S = +5V, single supply, T_A = 25˚C, and R_L to ground unless otherwise specified) (Continued)

Gain/Phase Response vs Temperature



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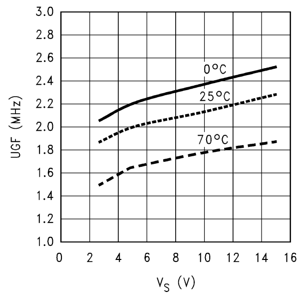
Unity Gain Frequency vs Temperature



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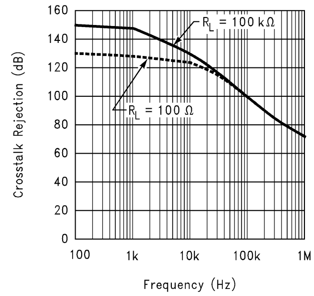
Crosstalk Rejection vs Frequency



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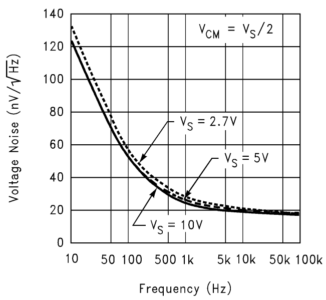
Input Voltage Noise vs Frequency



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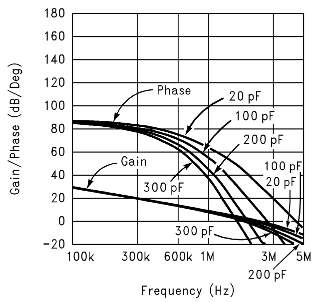
Gain/Phase vs Capacitive Load



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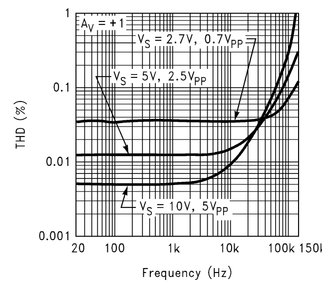
THD vs Frequency



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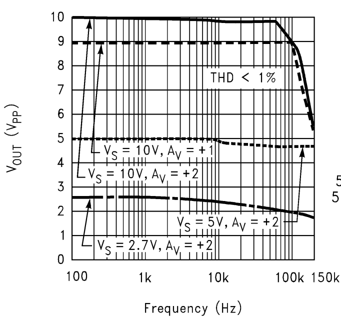
Output Swing vs Frequency



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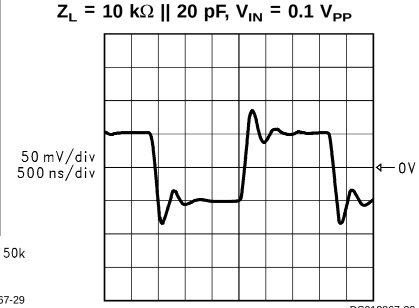
Small Signal Step Response
V_S = ±1.35V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 0.1 V_{PP}



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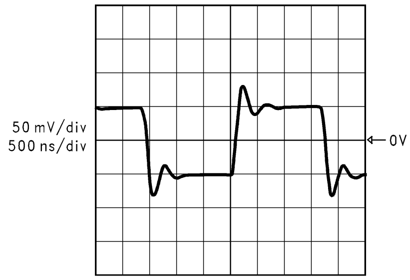
Typical Performance Characteristics (V_S = +5V, single supply, T_A = 25˚C, and R_L to ground unless otherwise specified) (Continued)

Small Signal Step Response
V_S = ±2.5V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 0.1 V_{PP}



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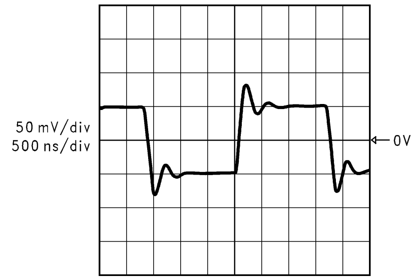
Small Signal Step Response
V_S = ±5V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 0.1 V_{PP}



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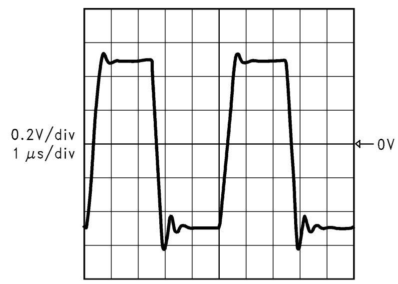
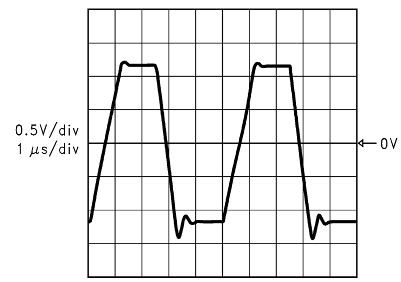
Large Signal Step Response
V_S = ±1.35V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 1 V_{PP}



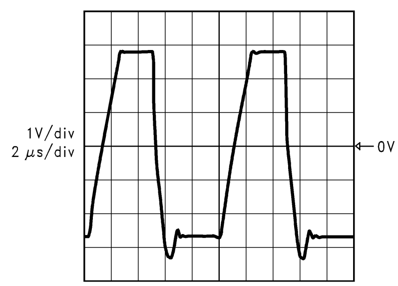
DS012867-33

Large Signal Step Response
V_S = ±2.5V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 2.4 V_{PP}



DS012867-34

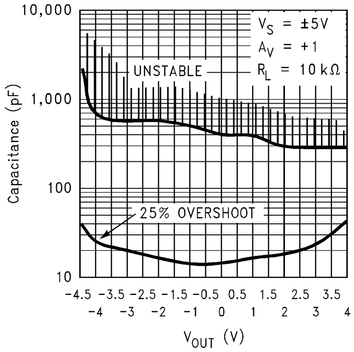
Large Signal Step Response
V_S = ±5V, A_V = +1,
Z_L = 10 kΩ || 20 pF, V_{IN} = 5.5 V_{PP}



DS012867-35

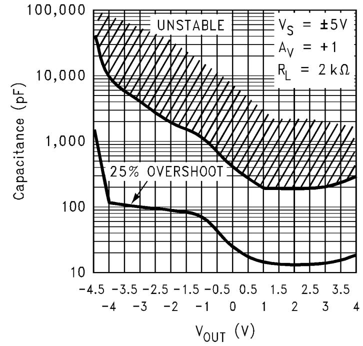
Typical Performance Characteristics (V_S = +5V, single supply, T_A = 25˚C, and R_L to ground unless otherwise specified) (Continued)

Stability vs Capacitive Load



DS012867-36

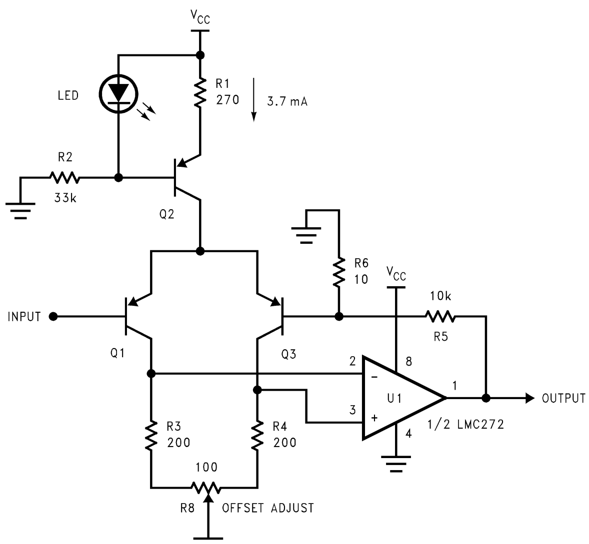
Stability vs Capacitive Load



DS012867-37

Application Information

Low Noise Single Supply Preamp



DS012867-2

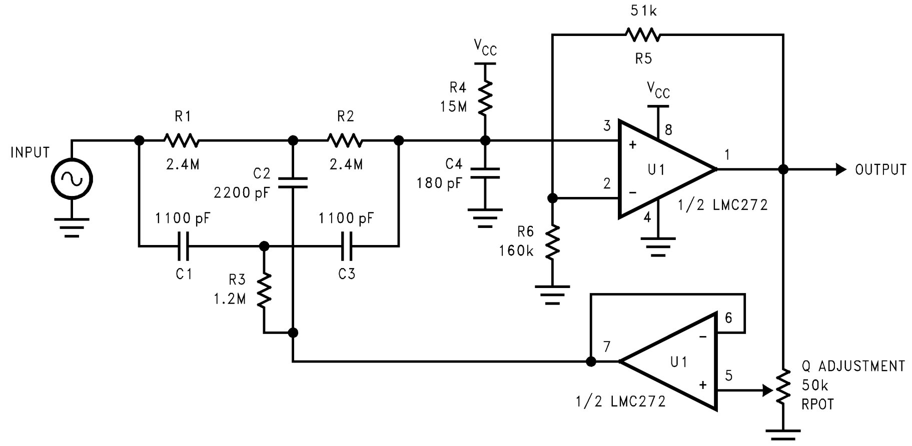
It is generally difficult to find already existing solutions in the market which are single supply and low noise. The circuit above is a low noise single supply preamp using the LMC272. It utilizes the feature of input common mode voltage range to ground to achieve zero-volt-in zero-volt-out performance and uses the RR output swing to achieve maximum dynamic range. By introducing a differential pair operating at high bias current as the front end, the equivalent input noise voltage, e_n, is reduced. The gain is 1 + R5/R6 which is a 1000 in this case. There is an inherent trade off between noise voltage and power consumption, input bias current, and input noise current. Input equivalent noise current is inconsequential if the source impedance is small. R1 can be adjusted to vary bias current. To avoid saturation, R3 and R4 should be set such that Q1 and Q3 collector voltages do not exceed 0.5V. *Table 1* shows typical noise data for two different R1 settings:

Application Information (Continued)

TABLE 1. Equivalent Input Noise Voltage, e_n, for Two Different Values of R1

Ω	mA	nV/√Hz		
R1	**I_C(Q1, 3)**	**e_n (100 Hz)**	**e_n (1 kHz)**	**e_n (10 kHz)**
270	1.85	3.2	2.0	1.7
1000	0.50	5.3	2.4	1.9

Single Supply Twin-T Notch Filter with "Q" Adjustment



DS012867-3

Here is another application for the LMC272. This is a single supply notch filter set for 60 Hz using the component values shown, but the frequency can be changed using the equations below. The main feature of this circuit is its ability to adjust the filter selectivity (Q) using RPOT. You can trade off notch depth for Q. *Table 2* shows data for two different settings. The LMC272 lends itself nicely to general purpose applications like this because it is very well behaved and easy to use. This filter can operate from 2.7V to 15V supplies. Component value matching is important to achieve good results. Here R4 is used to set the input to within the common mode range of the device to allow maximum swing on the non-inverting input (pin 3). Since R1, R2, and R4 form a voltage divider at low frequencies, C4 is added to introduce a high frequency attenuation in conjunction with C1, and C3. R5 and R6 were picked to set the pass band gain to 0 dB.

$R = R1 = R2 = 2R3$

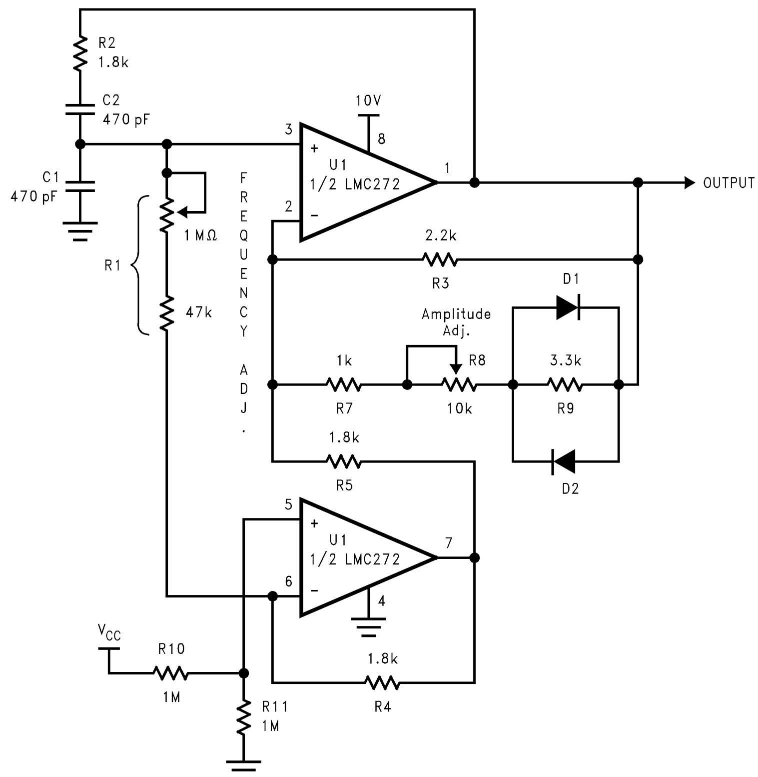
$C = C1 = C3 = C2/2$

$$f(notch) = \frac{1}{2\pi RC};\ C4 = \frac{R \bullet C}{R4},\ Q = \frac{f(notch)}{BW}$$

TABLE 2. Filter Selectivity (Q) vs Notch Depth

	(dB)
Q	**Notch Depth**
0.3	40
6	17

Single Supply Wein_Bridge Oscillator with Amplitude and Frequency Adjustment

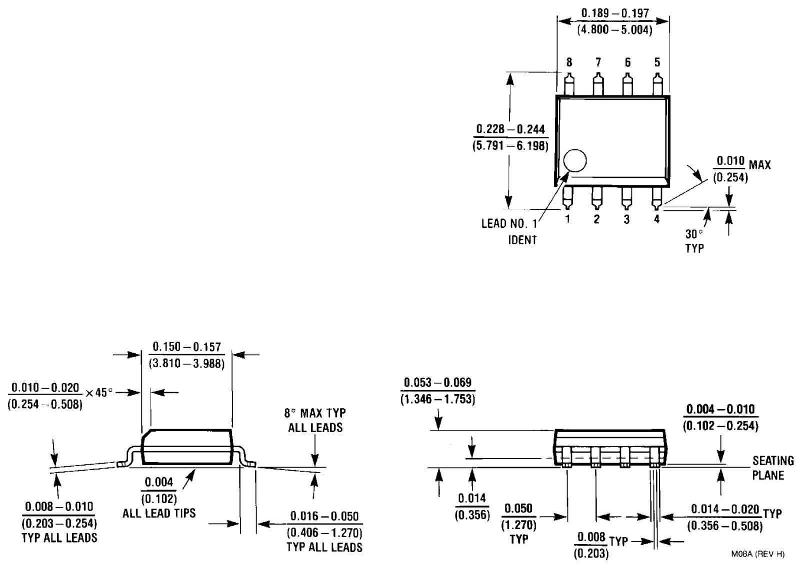


$$f_{OSC} \cong \frac{1}{2\pi\sqrt{C1\ C2\ R1\ R2}}$$

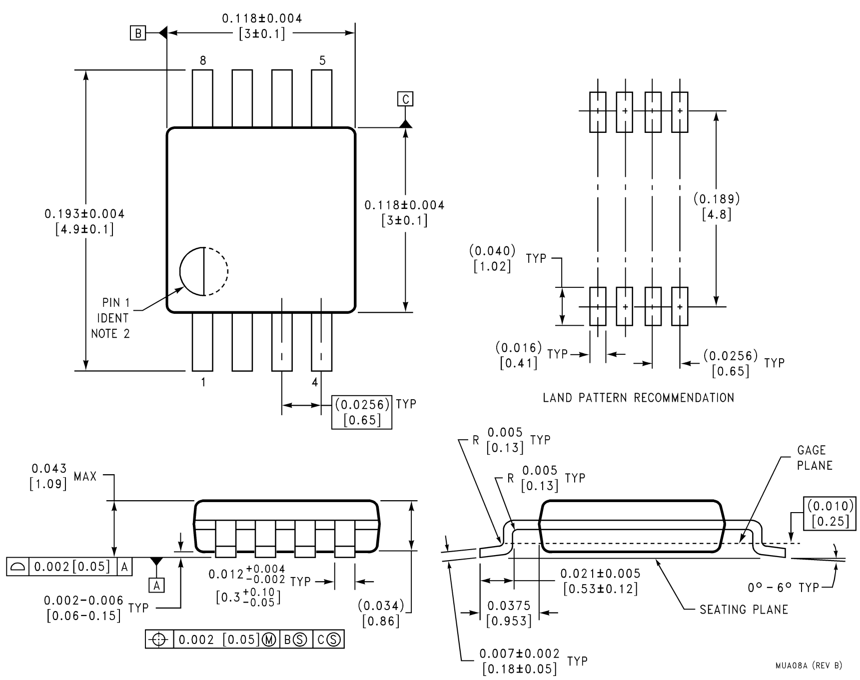
f(range) = 6.4 kHz to 30 kHz

Amplitude Adjustment (range) = 2.8 V_{PP} to 8.6 V_{PP}

Physical Dimensions inches (millimeters) unless otherwise noted

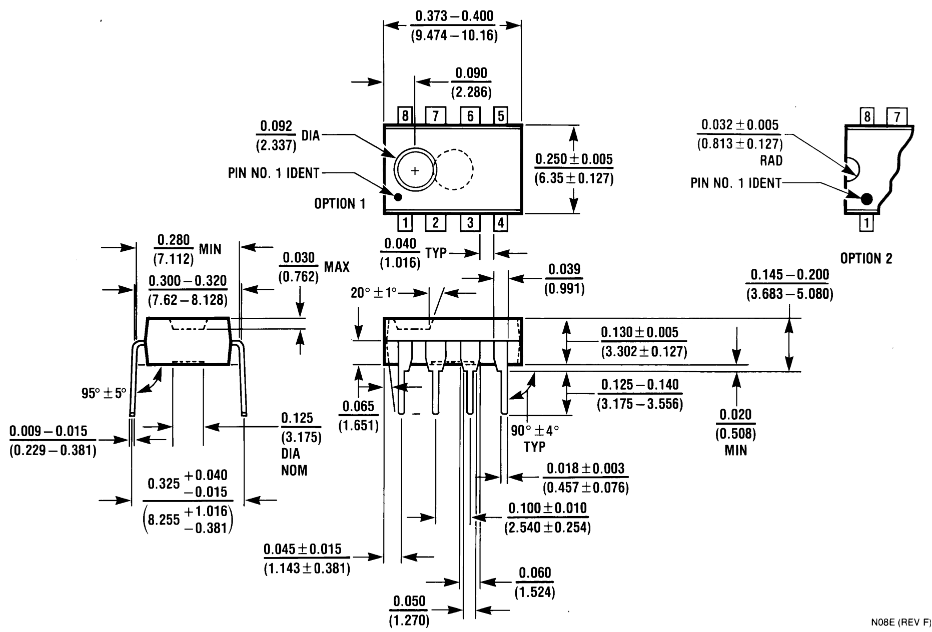


8-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
Order Number LMC272CM or LMC272CMX
NS Package Number M08A



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LMC272CMM or LMC272CMMX
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number LMC272CN
NS Package Number N08E

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