National Semiconductor

PRELIMINARY
November 1995

LMC2626
CMOS LDOR/Buffer Chip for Row Inversion Flat Panel Display Systems

General Description

The LMC2626 integrated circuit is specifically developed for a row inversion TFT FPD system architecture. It is designed only to be used in conjunction with National's LM2625 switching regulator chip.

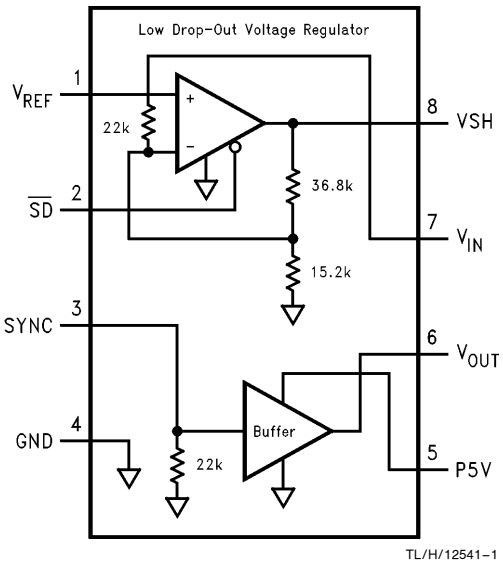
Built on National's advanced CMOS CS80 process, this chip generates a high-power, precision square-wave from a digital sync signal. The chip also contains thermal shutdown circuitry, system shutdown circuitry, and a low drop-out voltage regulator to generate a 4.2 volt supply from an externally applied reference voltage of 1.227V.

Features

- Used in conjunction with LM2625 chip
- High output current buffer
- Low buffer on resistance
- System shutdown control
- LDO voltage regulator
- LDOR dropout 0.3V maximum at 150 mA
- Thermal shutdown/short circuit protection
- External reference required for LDOR
- V_{REF} pin converts to a digital pin to shutdown LM2625

Connection Diagram

8-Pin SO



TL/H/12541–1

Top View

Pin Description

Pin #	Pin Name	Description
1	V_{REF}	1.218V to 1.242V Ext. Reference from LM2625 (see Note 8)
2	$\overline{SD}$	System Shutdown input pin for LMC2626 and LMC2625
3	SYNC	Digital input square wave from FPD controller
4	GND	Ground
5	P5V	Precision Regulated +5V Supply
6	V_{OUT}	Power Buffer Output
7	V_{IN}	FPD System Supply (+4.5V to +5.5V)
8	V_{SH}	Low Drop-Out Voltage Regulator Output

Ordering Information

Package	Temperature Range −40°C to +85°C	NSC Drawing	Transport Media
8-Pin SO	LMC2626IM	M08A	Rail Tape and Reel

RRD-B30M26/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

ESD Tolerance 2 kV HBM, 200V MM (Note 4)

Sync Input Voltage	P5V
Supply Voltage (V_{IN}, P5V)	6.3V
Continuous Total Power Dissipation (Note 1)	
Lead Temperature (less than 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Operating Ratings (Note 1)

V_{IN} Supply Voltage	$4.5V \le V_{IN} \le 5.5V$
P5V Supply Voltage (Note 5)	$4.8V \le P5V \le 5.2V$
Junction Temperature Range	−25°C to +125°C
Ambient Temperature Range	−40°C to +85°C

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $-20°C \le T_A \le +85°C$, P5V = 5V and $4.5V \le V_{IN} \le 5.5V$, V_{REF} = 1.227V SYNC(OPEN), $\overline{SD}$(OPEN) < P5V = V_{IN} = 5V

VSH LDO Voltage Regulator (Notes 7, 10, 11)

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
$V_{O(VREF)}$	V_{REF} Voltage Level in Shutdown	$\overline{SD}$ = 0V I_{VREF} = −1 mA V_{IN} = 5V	4.00	4.76		V
I_{VREF}	DC Current from V_{REF} Pin		−40.0	−13.3	−5	μA
V_{SH}	Output Voltage on V_{SH} Pin (see Note 2)	$4.5V \le V_{IN} \le 5.5V$ 20 mA ≤ IL ≤ 150 mA $1.218 \le V_{REF} \le 1.242$	4.10	4.20	4.30	V
ΔV_{SH}	Variation of V_{SH} over Temperature	$4.5V \le V_{IN} \le 5.5V$ 20 mA ≤ IL ≤ 150 mA		4	126	mV
V_{DO}	LDOR Voltage Dropout (V_{IN}−V_{SH})	IL = 150 mA		0.17	0.30	V
$I_{S(VIN)}$	V_{IN} Supply Current		230	394	500	μA
	Load Regulation of LDO Voltage Regulation	$4.5V \le V_{IN} \le 5.5V$ 20 mA ≤ IL ≤ 150 mA		0.002	0.015	%/mA
	Line Regulation of LDOR	$4.5V \le V_{IN} \le 5.5V$ 20 mA ≤ IL ≤ 150 mA		0.24	0.95	%/V
T_{SD}	Thermal Shutdown Threshold	(see Note 8)		160		°C
I_{OUT}	Output Load Current	(see Note 2)			300	mA

Shutdown Control (Note 8)

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
$I_{IL(\overline{SD})}$	Low Level Input Current for $\overline{SD}$ Pin	V_{IN} = 5V $\overline{SD}$ = 0V	−300	−217	−150	μA
$I_{IH(\overline{SD})}$	High Level Input Current for $\overline{SD}$ Pin	$\overline{SD}$ = 5V		310	1000	nA
$I_{S(\overline{SD})}$	V_{IN} Supply Current in Shutdown Mode		180	285	400	μA
$C_{in(SYNC)}$	Input Capacitance at SYNC Pin (Note 6)	SYNC = 5V T_A = 27°C		20		pF

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $-20°C \le T_A \le +85°C$, P5V = 5V and $4.5V \le V_{IN} \le 5.5V$, V_{REF} = 1.227V SYNC(OPEN), $\overline{SD}$(OPEN) < P5V = V_{IN} = 5V (Continued)

Buffer

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
V_{OUT}	Peak to Peak Output Voltage Swing or V_{OUT}	SYNC = $5V_{pp}$ (no load)	4.997	4.999		V
V_{OL}	Low Level Output Voltage	SYNC = 0V (No Load)		0.2	2	mV
V_{OH}	High Level Output Voltage	SYNC = 5V (No Load)		4.999		V
Δ_{VOUT}	Variation of V_{OUT} Over Temperature		0.2	1	3	mV
V_{IH} SYNC, $\overline{SD}$	High Level Input Voltage		3.5	5		V
V_{IL} SYNC, $\overline{SD}$	Low Level Input Voltage			0	1.5	V
$I_{IL(SYNC)}$	Low Level Input Current for SYNC	SYNC = 0V	5.0	42	1000	nA
$I_{IH(SYNC)}$	High Level Input Current for SYNC	SYNC = $5V_{DC}$	170	215	275	μA
$I_{OUT-AVE}$	V_{OUT} Maximum Average Load Current from (see Note 2)	SYNC = $5V_{PP}$			100	mA
R_{ON} N-Channel	On Resistance	IL = 150 mA T_A = 27°C		0.9	1.5	Ω
R_{ON} P-Channel	On Resistance	IL = 150 mA T_A = 27°C		0.7	1.2	Ω
R_{ON} Matching	On Resistance	IL = 150 mA T_A = 27°C		0.18	0.6	Ω
I_s	Supply Current from P5V	No SYNC	200	355	950	μA

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = 27°C$, $V_{IN} = = P5V = 5V$. Other conditions are shown in the test circuit. Conditions that deviate from those shown in the test circuit are listed in the conditions column.

Symbol	Parameter	Conditions	Min	Typ (Note 9)	Max	Units
$t_{s(OUT)}$	Settling Time for V_{OUT}	To 98% p-p V_{OUT}, $V_{IN} = 5V$ (see Note 3)			5.0	μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The typical junction-ambient thermal resistance of the molded plastic SO(M) package is 155°C/W. Therefore the maximum current for the buffer and voltage regulator are limited to the maximum total power dissipation that the package can allow in order to keep the die comfortably below the maximum operating junction temperature of 125°C.

Note 3: The settling time of the Power Buffer is mostly dependent upon the TFT effective series RC load. The measurement of the settling time is taken for the application when driving an all black display. The number in the datasheet reflects a series RC load ($R = 6.8\Omega$ and $C = 0.22\ \mu F$).

Note 4: Human Body Model 100 pF and 1.5 kΩ. Machine Model 0Ω.

Note 5: The precision of the P5V supply determines the output voltage swing precision of the buffer for very small loads. The operating range of P5V in this datasheet assumes a $\pm 4\%$ error in V_{OUT} p-p such that the total error of the signal at the output of the buffer never exceeds $\pm 5\%$.

Note 6: This capacitance is dominated by the ESD protection zeners connected to the SYNC pin.

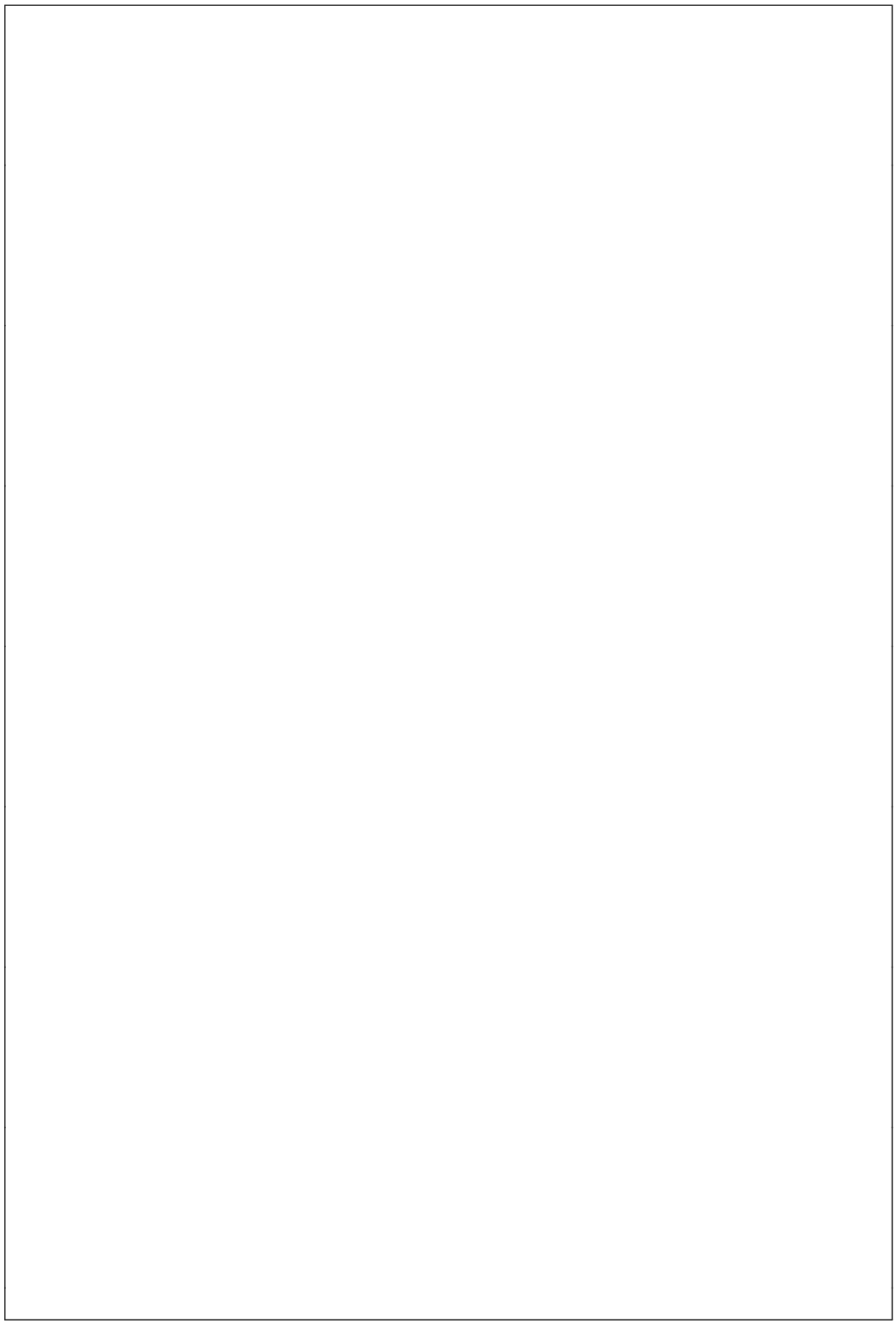
Note 7: It is important to understand that the load current of the low drop-out voltage regulator must not drop below 2 mA. Otherwise, the internal error amplifier will not have sufficient drive capability to the large series pass transistor. If load requirements from the FPD system is less than 2 mA, an external pre-load resistor must be connected from V_{SH} to ground in order to satisfy the previously mentioned load requirements.

Note 8: The thermal shutdown mode of the voltage regulator and the system shutdown mode are identical. When either of the two functions are enabled, two results occur. The pass transistor of the voltage regulator is shut off and The V_{REF} pin of the LMC2626 is pulled up to the V_{IN} supply to shutdown the LM2625 switching regulator.

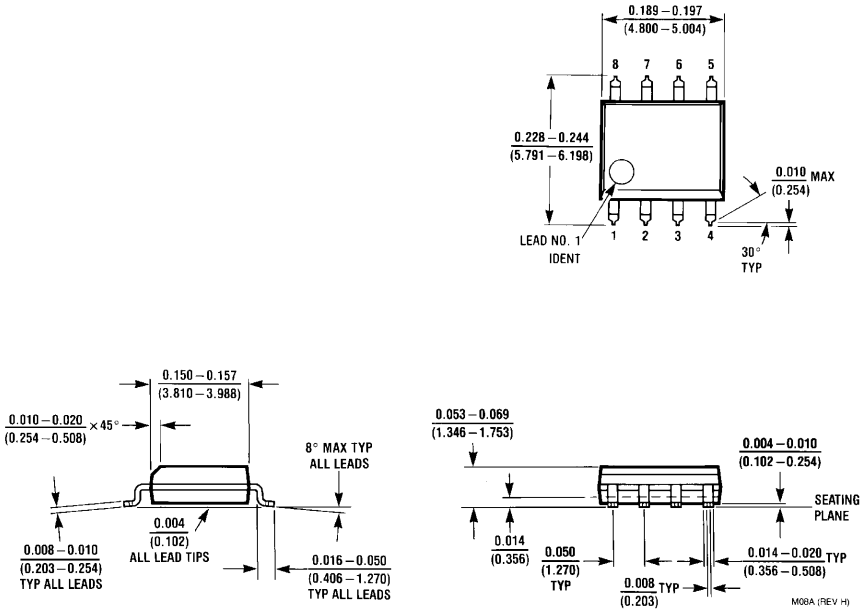
Note 9: Typical values represent the most likely parametric norm.

Note 10: The typical closed loop voltage gain of the low drop-out voltage regulator is 3.44(10.7 dB).

Note 11: The minimum load current of the voltage regulator is a specific parameter used to guarantee that the regulated output voltage of the LDO regulator stays within the limits specified in the datasheet for $1.216V < V_{REF} < 1.242V$. For applications requiring minimum load current less than 20 mA, regulated output voltage limits of the voltage regulator and V_{REF} voltage range must be carefully determined by characterizing the change in regulated output voltage at the minimum load current needed.



Physical Dimensions inches (millimeters)



8-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
Order Number LMC2626IM
NS Package M08A

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