



# Instrumentation Operational Amplifier

## OP-05

### FEATURES

- Low Noise .....  $0.6\mu V_{p-p}$  Max, 0.1 to 10Hz
- Low Drift vs. Temperature .....  $0.5\mu V/^{\circ}C$  Max
- Low Drift vs. Time .....  $0.2\mu V/\text{Month}$  Typ
- Low Bias Current ..... 2.0nA Max
- High CMRR ..... 114dB Min
- High PSRR ..... 100dB Min
- High Gain ..... 300,000 Min
- High  $R_{IN}$  Differential .....  $30M\Omega$  Min
- High  $R_{IN}$  CM .....  $200G\Omega$  Typ
- Internally Compensated ..... Stable to 500pF Load
- Fits 725, 108A and 741 Sockets
- 125°C Temperature Tested Dice
- Available in Die Form

### GENERAL DESCRIPTION

The OP-05 series of monolithic instrumentation operational amplifiers combine excellent performance in low-signal-level applications with the simplicity of use of a fully-protected, internally-compensated op amp. The OP-05 has low input offset voltage and bias current combined with very high levels of gain, input impedance, CMRR, and PSRR.

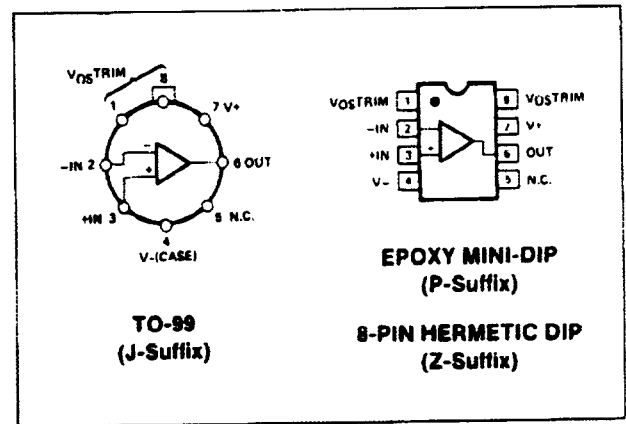
The OP-05 is a direct replacement in 725, 108A, and unnullled 741 sockets allowing instant system performance improvement without redesign. The OP-05 is an excellent choice for a wide variety of applications including strain gauge and thermocouple bridges, high-gain active filters, buffers, integrators, and sample-and-hold amplifiers. For dual-matched versions, refer to the OP-207 and OP-10 data sheets.

### ORDERING INFORMATION †

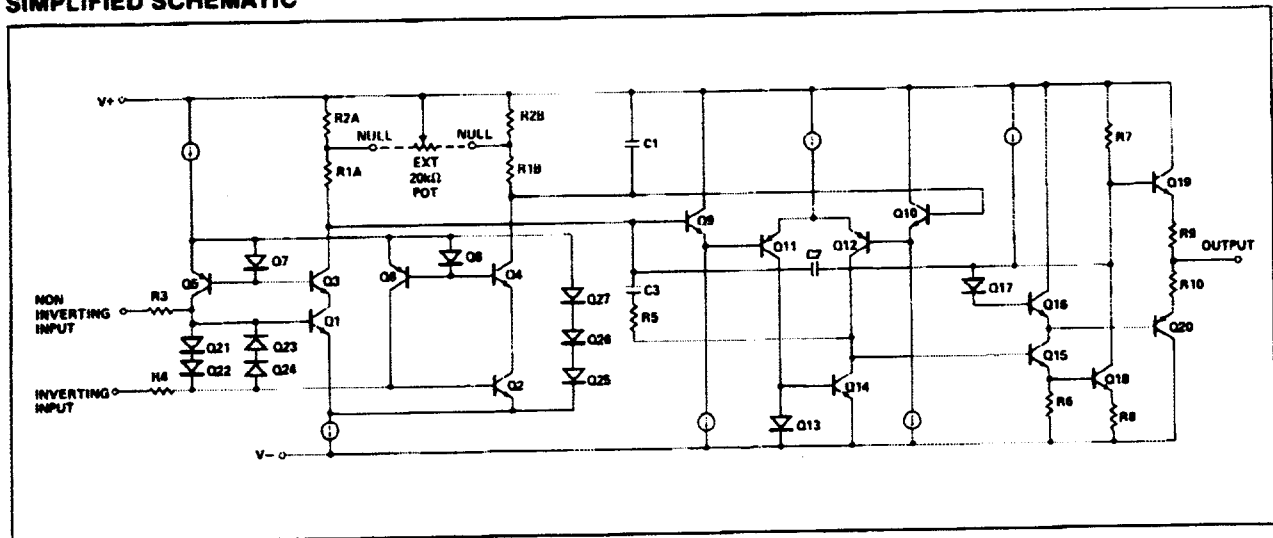
$T_A = 25^{\circ}C$ $V_{OS}$ MAX (mV)	PACKAGE			OPERATING TEMPERATURE RANGE
	TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	
0.15	OP05AJ*	OP05AZ*	-	MIL
0.5	OP05J*	-	-	MIL
0.5	OP05EJ	OP05EZ	OP05EP	COM
1.3	OP05CJ	OP05CZ	OP05CP	COM

- \* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
- † Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC



# OP-05

## ABSOLUTE MAXIMUM RATINGS (Note 3)

Supply Voltage .....	±22V
Differential Input Voltage .....	±30V
Input Voltage (Note 1) .....	±22V
Output Short-Circuit Duration .....	Indefinite
Storage Temperature Range	
J and Z Packages .....	-65°C to +150°C
P Package .....	-65°C to +125°C
Operating Temperature Range	
OP-05A, OP-05 .....	-55°C to +125°C
OP-05E, OP-05C .....	0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) .....	300°C
Junction Temperature .....	-65°C to +150°C

PACKAGE TYPE	$\theta_{JA}$ (NOTE 2)	$\theta_{JC}$	UNITS
TO-99 (J)	150	18	°C/W
8-Pin Hermetic DIP (Z)	148	18	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W

**NOTES:**

1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2.  $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDIP, P-DIP, and LCC packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SO and PLCC packages.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		-	0.07	0.15	-	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Note 1)	-	0.2	1.0	-	0.2	1.0	$\mu V/Mo$
Input Offset Current	$I_{OS}$		-	0.7	2.0	-	1.0	2.8	nA
Input Bias Current	$I_B$		-	±0.7	±2.0	-	±1.0	±3.0	nA
Input Noise Voltage (Note 2)	$e_{n-p-p}$	0.1Hz to 10Hz	-	0.35	0.6	-	0.35	0.6	$\mu V_{p-p}$
Input Noise Voltage Density (Note 2)	$e_n$	$f_O = 10\text{Hz}$	-	10.3	18.0	-	10.3	18.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	-	10.0	13.0	-	10.0	13.0	
		$f_O = 1000\text{Hz}$	-	9.6	11.0	-	9.6	11.0	
Input Noise Current (Note 2)	$i_{n-p-p}$	0.1Hz to 10Hz	-	14	30	-	14	30	$\text{pA}_{p-p}$
Input Noise Current Density (Note 2)	$i_n$	$f_O = 10\text{Hz}$	-	0.32	0.80	-	0.32	0.80	$\text{pA}/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	-	0.14	0.23	-	0.14	0.23	
		$f_O = 1000\text{Hz}$	-	0.12	0.17	-	0.12	0.17	
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	30	80	-	20	80	-	M $\Omega$
Input Resistance — Common-Mode	$R_{INCM}$		-	200	-	-	200	-	G $\Omega$
Input Voltage Range	IVR		±13.5	±14.0	-	±13.5	±14.0	-	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	114	126	-	114	126	-	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	-	4	10	-	4	10	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	300	500	-	200	500	-	V/mV
		$R_L \geq 500\Omega$ , $V_O = \pm 0.5V$	150	500	-	150	500	-	
		$V_S = \pm 3V$ (Note 3)							
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	±12.5	±13.0	-	±12.5	±13.0	-	V
		$R_L \geq 2k\Omega$	±12.0	±12.8	-	±12.0	±12.8	-	
		$R_L \geq 1k\Omega$	±10.5	±12.0	-	±10.5	±12.0	-	
Slew Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	-	0.1	0.3	-	V/ $\mu s$
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	-	0.4	0.6	-	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0$ , $I_O = 0$	-	60	-	-	60	-	$\Omega$
Power Consumption	$P_d$	No load	-	90	120	-	90	120	mW
		$V_S = \pm 3V$ , No load	-	4	6	-	4	6	
Offset Adjustment Range		$R_p = 20k\Omega$	-	4	-	-	4	-	mV

**NOTES:**

1. Long-term input offset voltage stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically 2.5 $\mu V$ . Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.10	0.24	—	0.3	0.7	mV
Average Input Offset Voltage Drift Without External Trim	$TCV_{OS}$	(Note 2)	—	0.3	0.9	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$	$R_p = 20k\Omega$ (Note 3)	—	0.2	0.5	—	0.3	1.0	
Input Offset Current	$I_{OS}$		—	1.0	4.0	—	1.8	5.6	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	5	25	—	8	50	$\mu A/^\circ C$
Input Bias Current	$I_B$		—	$\pm 1$	$\pm 4$	—	$\pm 2$	$\pm 6$	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	8	25	—	13	50	$\mu A/^\circ C$
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	110	123	—	110	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	200	400	—	150	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.6$	—	$\pm 12.0$	$\pm 12.6$	—	V

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.2	0.5	—	0.3	1.3	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.3	1.5	—	0.4	2.0	$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	$I_B$		—	$\pm 1.2$	$\pm 4.0$	—	$\pm 1.8$	$\pm 7.0$	nA
Input Noise Voltage (Note 2)	$e_{np-p}$	0.1Hz to 10Hz	—	0.35	0.8	—	0.38	0.65	$\mu V_{p-p}$
Input Noise Voltage Density (Note 2)	$e_n$	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current (Note 2)	$i_{np-p}$	0.1Hz to 10Hz	—	14	30	—	15	35	$\mu A_{p-p}$
		$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.15	0.27	
Input Noise Current Density (Note 2)	$i_n$	$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	$\mu A/\sqrt{\text{Hz}}$
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	15	50	—	8	33	—	M $\Omega$
Input Resistance — Common-Mode	$R_{INCM}$		—	160	—	—	120	—	G $\Omega$
Input Voltage Range	IVR		$\pm 13.5$	$\pm 14.0$	—	$\pm 13.0$	$\pm 14.0$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	110	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	7	32	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	200	500	—	180	400	—	V/mV
		$R_L \geq 500\Omega$ , $V_O = \pm 0.5V$	150	500	—	100	400	—	
		$V_S = \pm 3V$ (Note 3)							
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.0$	$\pm 13.0$	—	V
		$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	$\pm 11.5$	$\pm 12.8$	—	
		$R_L \geq 1k\Omega$	$\pm 10.5$	$\pm 12.0$	—	—	$\pm 12.0$	—	
Slew Rate (Note 2)	SR	$R_L \geq 2k\Omega$	0.1	0.3	—	0.1	0.3	—	V/ $\mu s$
Closed-Loop Bandwidth (Note 2)	BW	$A_{VCL} = +1.0$	0.4	0.6	—	0.4	0.6	—	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0$ , $I_O = 0$	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_D$	No load	—	90	120	—	95	150	mW
		$V_S = \pm 3V$ , No load	—	4	6	—	4	8	
Offset Adjustment Range		$R_p = 20k\Omega$	—	4	—	—	4	—	mV

NOTE: See notes on previous page.

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**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$ , unless otherwise noted.

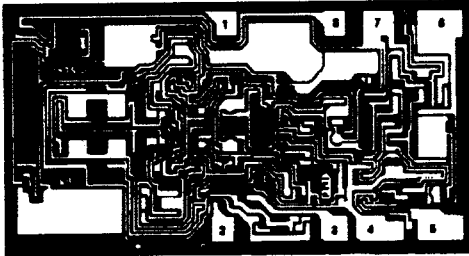
PARAMETER	SYMBOL	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage									
Drift Without External Trim	$TCV_{OS}$	(Note 2)	—	0.7	2.0	—	1.3	4.5	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$	$R_P = 20k\Omega$ (Note 3)	—	0.2	0.6	—	0.4	1.5	
Input Offset Current	$I_{OS}$		—	1.4	5.3	—	2.0	6.0	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	8	35	—	12	50	$\mu A/^\circ C$
Input Bias Current	$I_B$		—	$\pm 1.5$	$\pm 5.5$	—	$\pm 2.2$	$\pm 9.0$	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	13	35	—	18	50	$\mu A/^\circ C$
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.0V$	107	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	180	450	—	100	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.6$	—	$\pm 11.0$	$\pm 12.6$	—	V

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$ . Refer to typical performance curve.
2. Sample tested.
3. Guaranteed by design.

OP-05

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



- 1. BALANCE
- 2. INVERTING INPUT
- 3. NONINVERTING INPUT
- 4. V-
- 5. NO CONNECTION
- 6. OUTPUT
- 7. V+
- 8. BALANCE

DIE SIZE 0.101 × 0.052 inch, 5300 sq. mils  
(2.57 × 1.32 mm, 3.34 sq. mm)

WAFER TEST LIMITS at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  for OP-05N, OP-05G and OP-05GR devices;  $T_A = 125^\circ C$  for OP-05NT and OP-05GT devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT LIMIT	OP-05N LIMIT	OP-05GT LIMIT	OP-05G LIMIT	OP-05GR LIMIT	UNITS
Input Offset Voltage	$V_{OS}$		0.25	0.15	0.7	0.5	1.3	mV MAX
Input Offset Current	$I_{OS}$		4.0	2.0	5.7	3.8	6.0	nA MAX
Input Bias Current	$I_B$		$\pm 4$	$\pm 2$	$\pm 6$	$\pm 4$	$\pm 7$	nA MAX
Input Resistance Differential Mode	$R_{IN}$	(Note 2)	—	20	—	15	8	M $\Omega$ MIN
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	$\pm 13.0$	$\pm 13.5$	$\pm 13.0$	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$ at $+25^\circ C$ $V_{CM} = \pm 13.0$ at $+125^\circ C$	110	114	110	110	100	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	20	10	20	20	30	$\mu V/V$ MAX
Output Voltage Swing	$V_O$	$R_L = 10k\Omega$	—	$\pm 12.5$	—	$\pm 12.5$	$\pm 12.0$	V MIN
		$R_L = 2k\Omega$	$\pm 12.0$	$\pm 12.0$	$\pm 12.0$	$\pm 12.0$	$\pm 11.5$	
		$R_L = 1k\Omega$	—	$\pm 10.5$	—	$\pm 10.5$	—	
Large-Signal Voltage Gain	$A_{VO}$	$R_L = 2k\Omega$ $V_O = \pm 10V$	200	200	150	200	120	V/mV MIN
Differential Input Voltage			$\pm 30$	$\pm 30$	$\pm 30$	$\pm 30$	$\pm 30$	V MAX
Power Consumption	$P_d$	$V_{OUT} = 0V$	—	120	—	120	150	mW MAX

NOTES:

- 1. For  $25^\circ C$  characteristics of NT & GT devices see N & G characteristics respectively.
- 2. Guaranteed by design.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

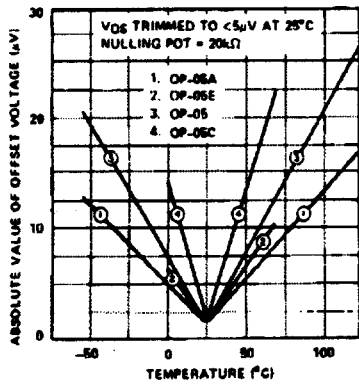
TYPICAL ELECTRICAL CHARACTERISTICS at  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-05NT TYPICAL	OP-05N TYPICAL	OP-05GT TYPICAL	OP-05G TYPICAL	OP-05GR TYPICAL	UNITS
Average Input Offset Voltage Drift	$TCV_{OS}$	$R_S \leq 50\Omega$	0.3	0.3	0.7	0.7	1.2	$\mu V/^\circ C$
Nullified Input Offset Voltage Drift	$TCV_{OSn}$	$R_S \leq 50\Omega$ , $R_p = 20k\Omega$	0.2	0.2	0.3	0.3	0.4	$\mu V/^\circ C$
Average Input Offset Current Drift	$TCI_{OS}$		5	5	8	8	12	$\mu A/^\circ C$
Slew Rate	SR	$R_L \geq 2k\Omega$	0.3	0.3	0.3	0.3	0.3	V/ $\mu s$
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	0.6	0.6	0.6	0.6	0.6	MHz

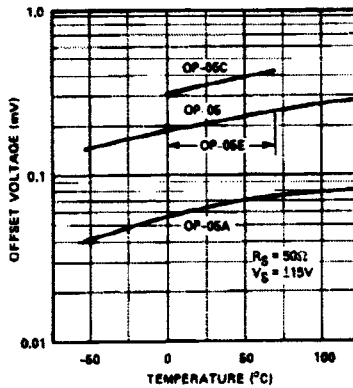
# OP-05

## TYPICAL PERFORMANCE CHARACTERISTICS

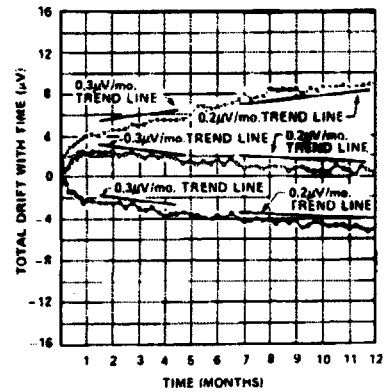
**TRIMMED OFFSET VOLTAGE vs TEMPERATURE**



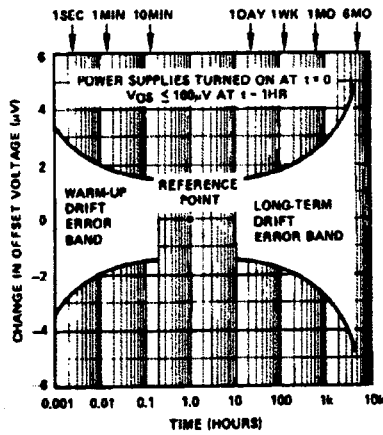
**UNTRIMMED OFFSET VOLTAGE vs TEMPERATURE**



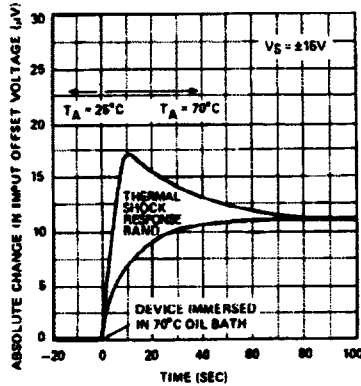
**TYPICAL OFFSET VOLTAGE STABILITY vs TIME**



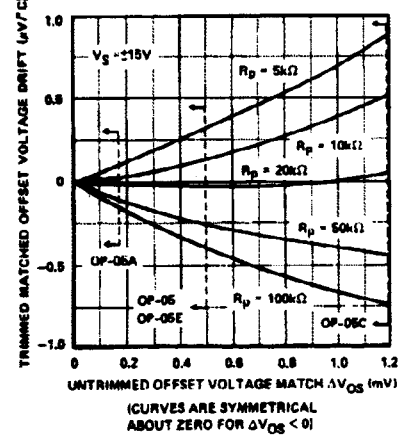
**OFFSET VOLTAGE DRIFT WITH TIME**



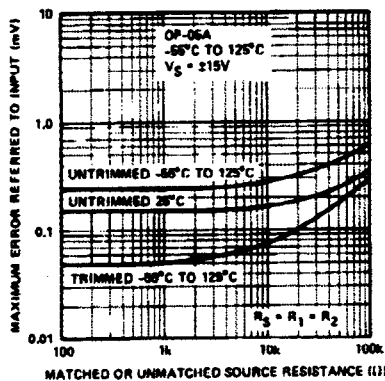
**OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK**



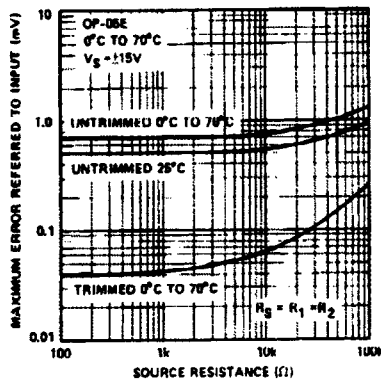
**TRIMMED OFFSET VOLTAGE DRIFT**



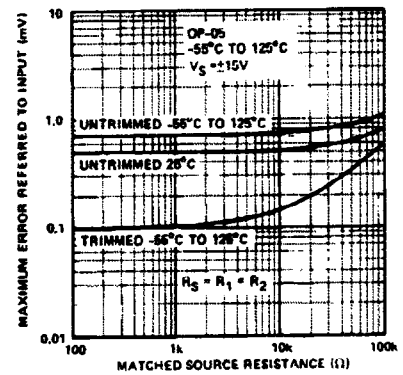
**MAXIMUM ERROR vs SOURCE RESISTANCE**



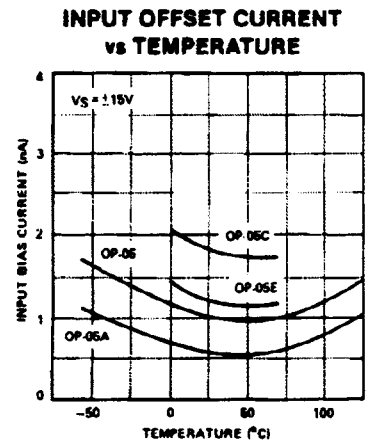
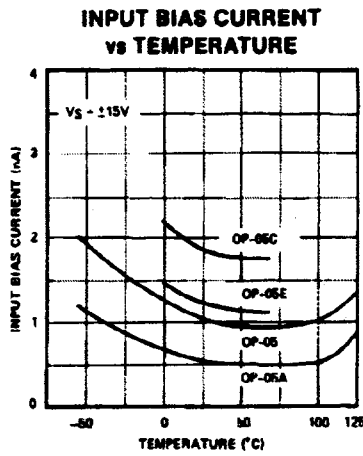
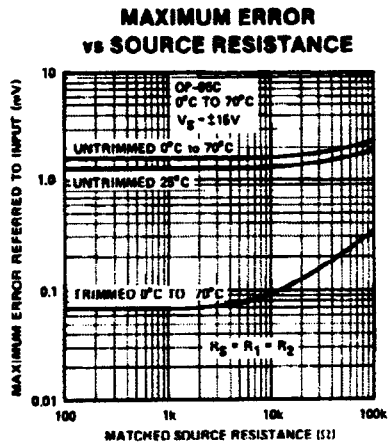
**MAXIMUM ERROR vs SOURCE RESISTANCE**



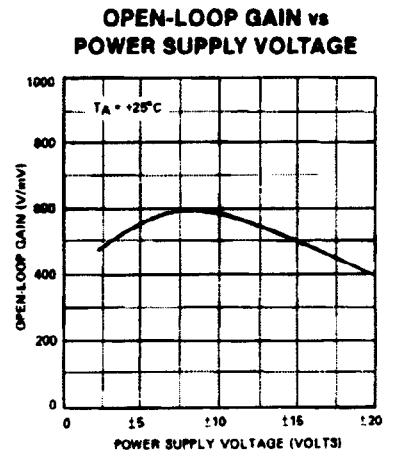
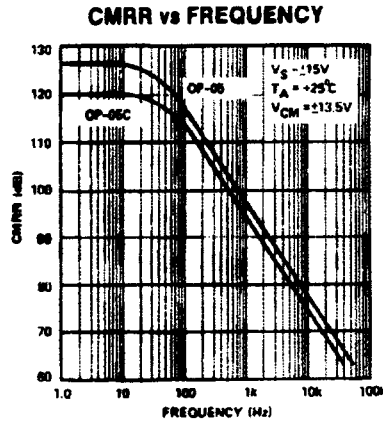
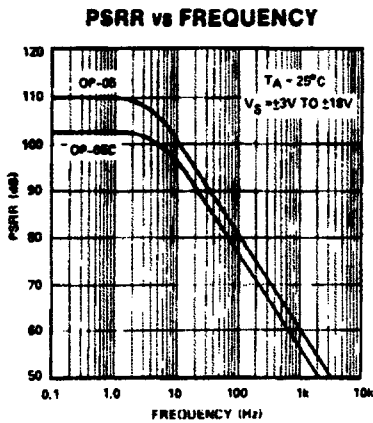
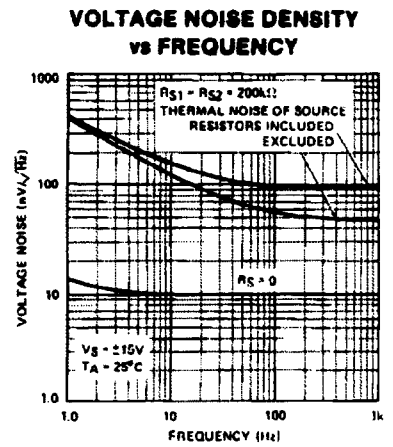
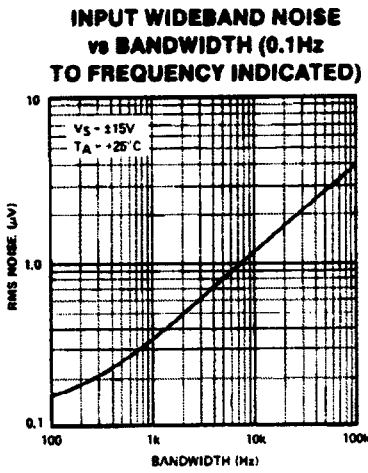
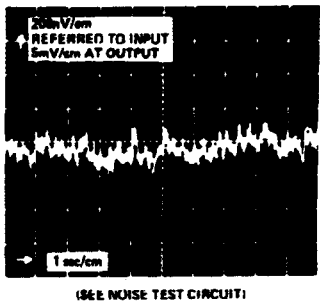
**MAXIMUM ERROR vs SOURCE RESISTANCE**



TYPICAL PERFORMANCE CHARACTERISTICS

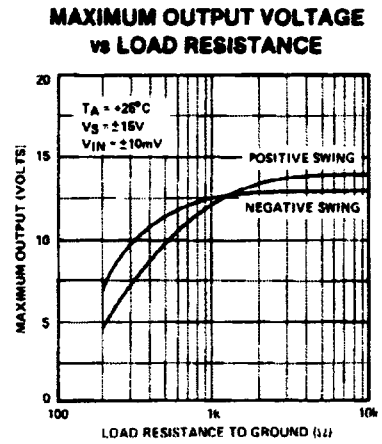
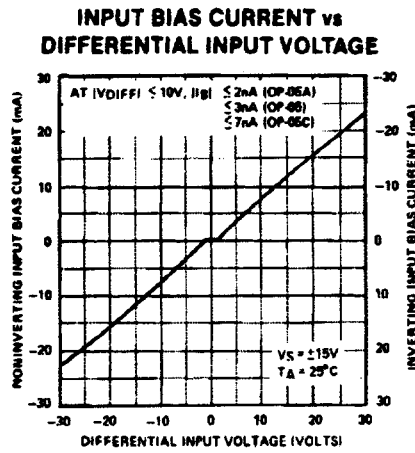
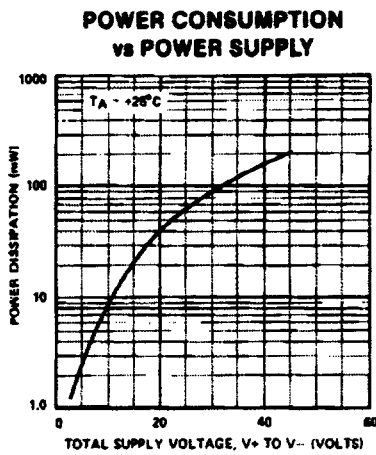
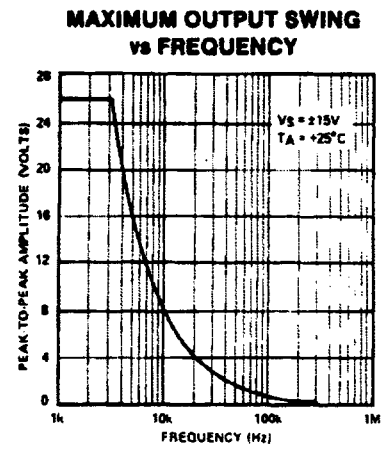
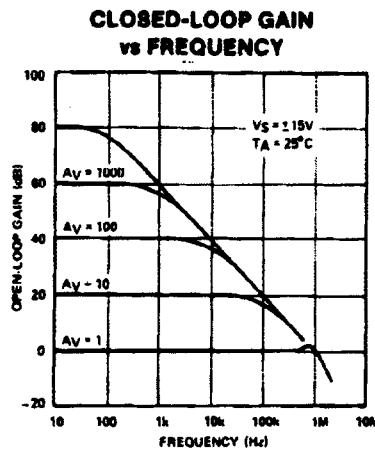
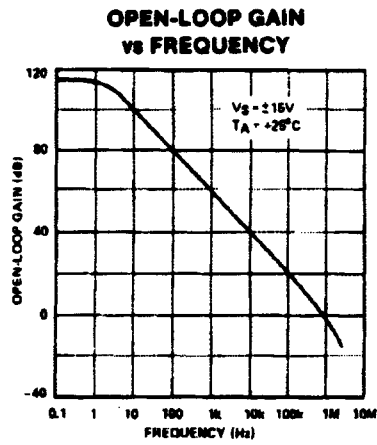


OP-05 LOW FREQUENCY NOISE

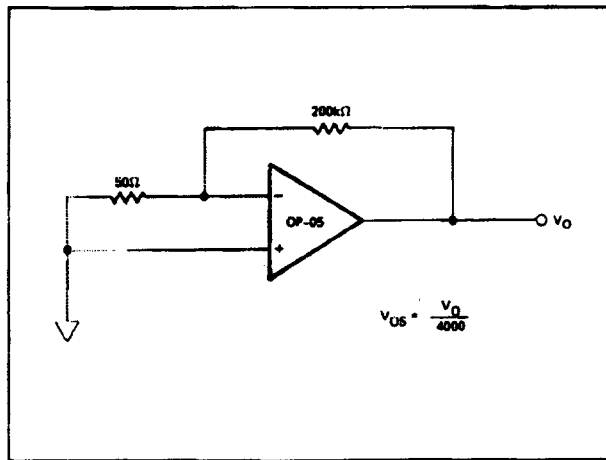


# OP-05

## TYPICAL PERFORMANCE CHARACTERISTICS



### TYPICAL OFFSET VOLTAGE TEST CIRCUIT



### TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT\*

