FEATURES

- **Low Offset Voltage ..... 150μV Max**
- **Low Offset Voltage Drift ..... 2.5μV/°C Max**
- **Five Times PM108A Output Current ..... 5mA Min**
- **Low Offset Current ..... 200pA Max**
- **Low Bias Current ..... 2nA Max**
- **Low Power Consumption ..... 18mW Max @ ±15V**
- **High Common-Mode Input Range ..... ±13.5V Min**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**
- **125° C Temperature-Tested Dice**
- **Available in Die Form**

ORDERING INFORMATION †

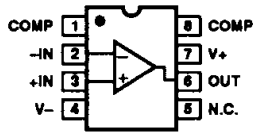
T_A = 25°C V_{OS} MAX (mV)	PACKAGE CERDIP 8-PIN	PACKAGE PLASTIC 8-PIN	OPERATING TEMPERATURE RANGE
0.15	OP08AZ	–	MIL
0.15	–	OP08EP	COM
1.0	OP08GZ	–	COM

† Burn-in is available on commercial and industrial temperature range parts in CerDIP and plastic DIP packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The PMI OP-08 is an improved version of the popular LM108A low-power op amp. Excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip-zener-zap trimming. The OP-08 has a three-times lower offset voltage and a two-times lower offset voltage drift. Worst-case input offset voltage over −55° C to +125° C for the OP-08 is only 350μV. In addition, the OP-08 has five times the output current capability of the 108A. For an op amp with identical specifications plus internal frequency compensation, see the OP-12 data sheet.

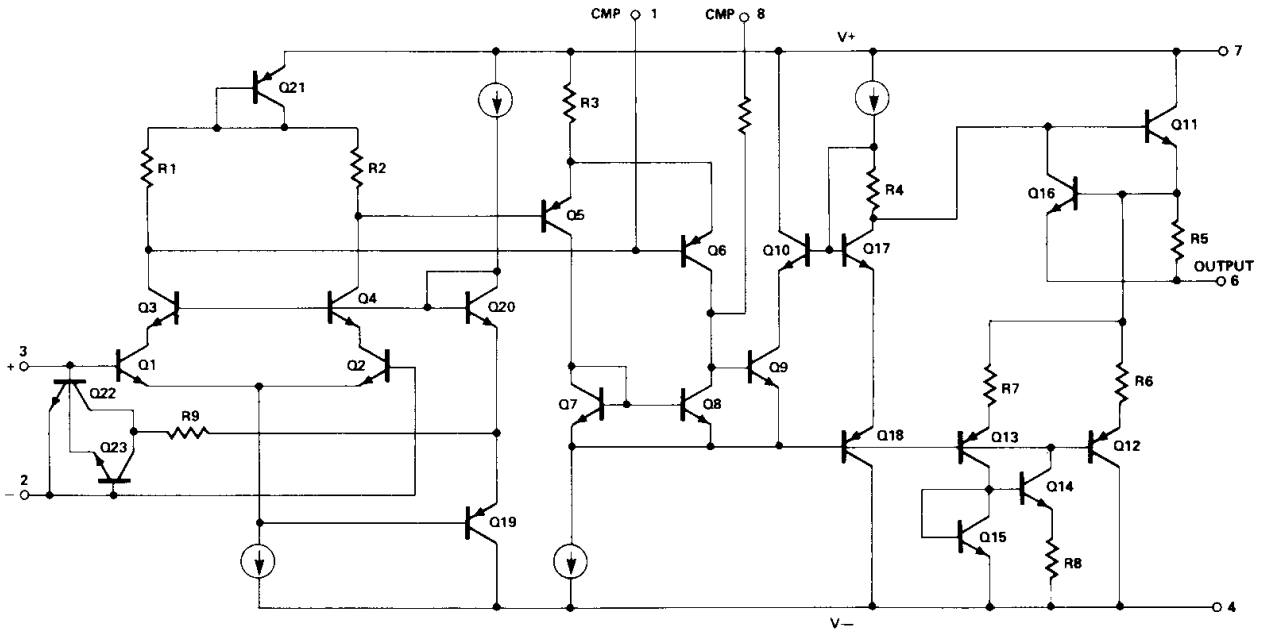
PIN CONNECTIONS



EPOXY MINI-DIP (P-Suffix)

8-PIN HERMETIC DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
- OP-08A, OP-08E (All DICE Except GR) ..... ±20V
- OP-08G (GR DICE Only) ..... ±18V

Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range
- OP-08A ..... −55°C to +125°C
- OP-08E, OP-08G ..... 0°C to +70°C

Storage Temperature Range (Z) ..... −65°C to +150°C
Storage Temperature Range (P) ..... −65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 3)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	162	26	°C/W
8-Pin Plastic DIP (P)	110	50	°C/W

NOTES:
1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs without some limiting resistance.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_S = ±20V for A and E Grades, V_S = ±15V for G Grade, unless otherwise noted.

Compensation capacitor = 30pF.

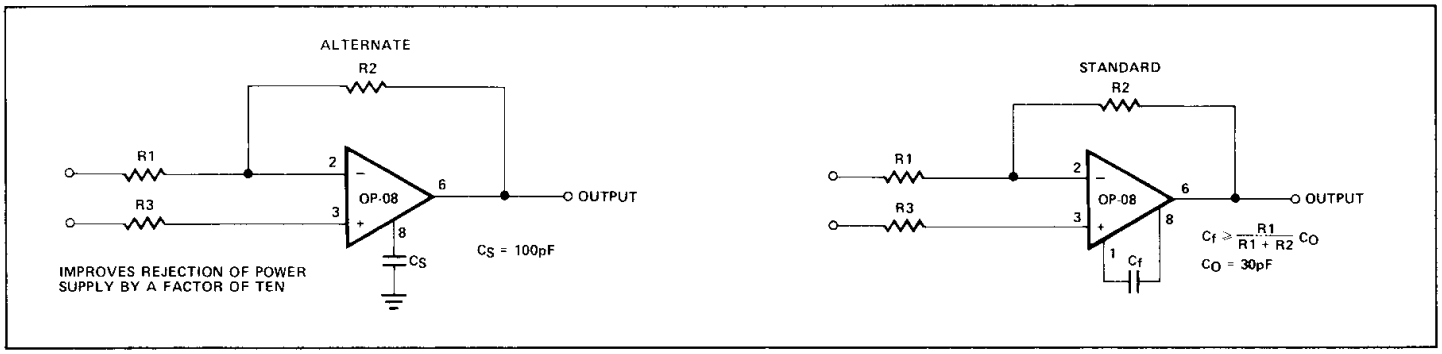
			OP-08A/E			OP-08G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.80	2.0	—	1.0	5.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	— — —	22 21 20	— — —	— — —	22 21 20	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	f_O = 10Hz f_O = 100Hz f_O = 1000Hz	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	$pA/\sqrt{Hz}$
Input Resistance — Differential Mode	R_{IN}	(Note 1)	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	V_S = ±15V	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13.5V	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	—	1	7	—	2	63	μV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 10kΩ, V_O = ±10V R_L ≥ 2kΩ, V_O = ±10V, V_S = ±15V	80 50	300 150	— —	40 —	250 100	— —	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ, V_S = ±15V R_L ≥ 2kΩ, V_S = ±15V	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	V
Slew Rate	SR	R_L ≥ 2kΩ	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	A_{VCL} = +1	—	0.8	—	—	0.8	—	MHz
Open-Loop Output Resistance	R_O	V_O = 0, I_O = 0	—	200	—	—	200	—	Ω
Power Consumption	P_d	V_S = ±15V V_S = ±5V	— —	9 3	18 6	— —	12 4	24 8	mW

NOTE:
1. Guaranteed by input bias current.

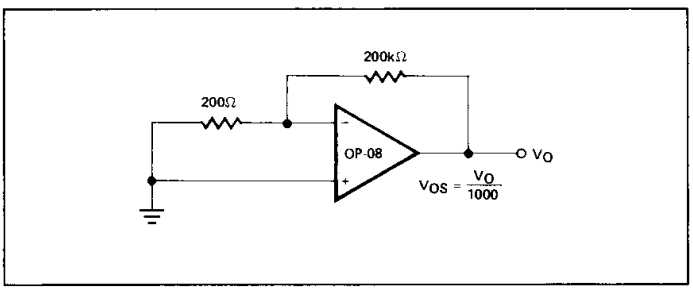
ELECTRICAL CHARACTERISTICS V_S = ±20V for A Grade, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08A MIN	OP-08A TYP	OP-08A MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.12	0.35	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	µV/°C
Input Offset Current	I_{OS}		–	0.12	0.40	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	pA/°C
Input Bias Current	I_B		–	1.2	3.0	nA
Input Voltage Range	IVR	V_S = ±15V	±13.5	±14.0	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13.5	100	110	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5V to ±15V	–	4	10	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 5k\Omega$, V_O = ±10V, V_S = ±15V	40	120	–	V/mV
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, V_S = ±15V $R_L \geq 5k\Omega$, V_S = ±15V	±13 ±10	±14 ±12	– –	V
Power Consumption	P_d	V_S = ±15V	–	9	18	mW

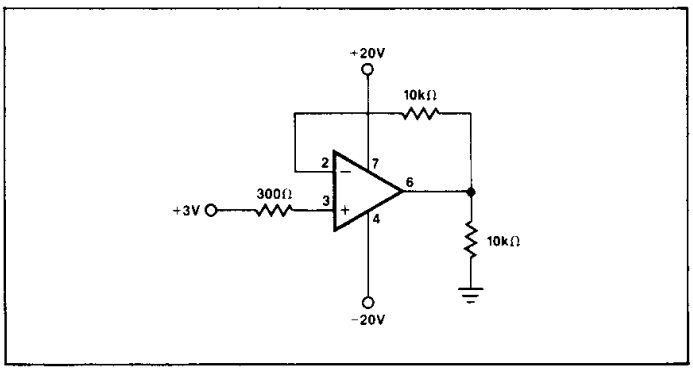
COMPENSATION CIRCUITS



OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT

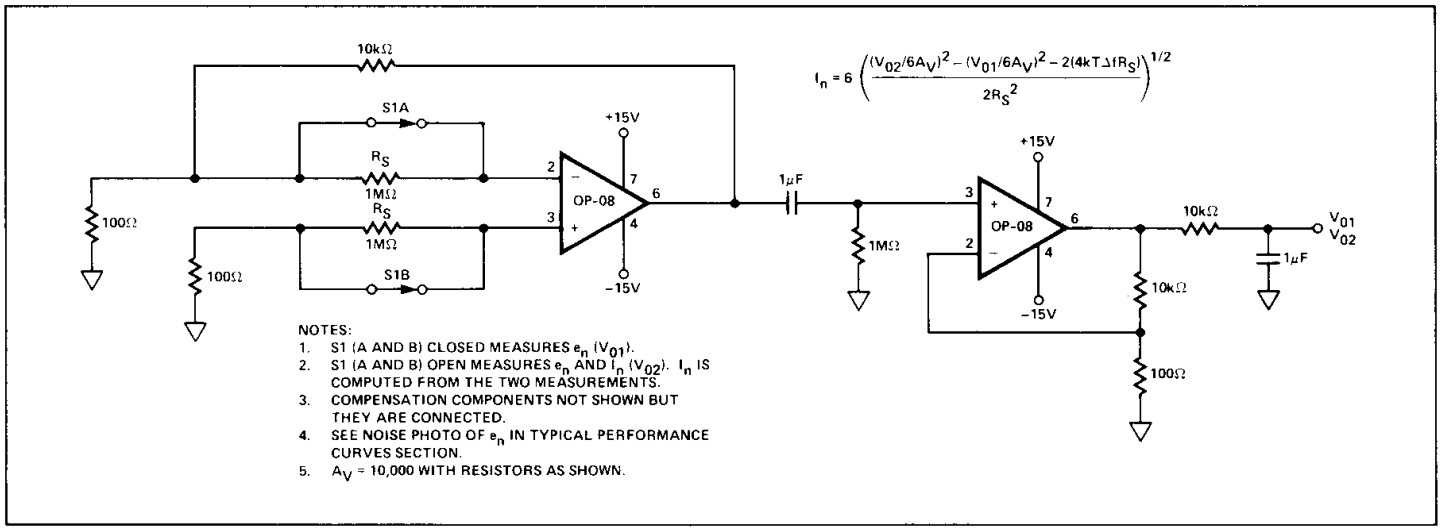


ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ for G Grade and $V_S = \pm 20V$ for E Grade, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

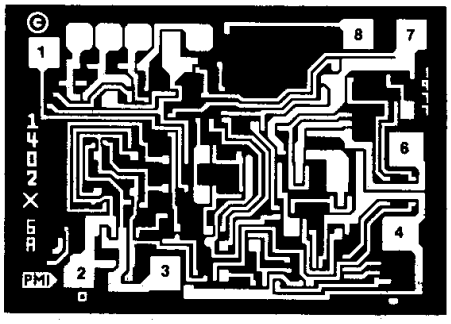
			OP-08E			OP-08G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	—	0.50	2.5	—	1.5	10	µV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.12	6.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 1)	—	0.50	2.5	—	2.0	50	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.4	6.5	nA
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±14.0	—	±13.5	±14.0	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13.5V$	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	2	10	—	3	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	25	100	—	—	80	—	V/mV
		$R_L \geq 10k\Omega$, $V_O = \pm 10V$, $V_S = \pm 15V$	60	200	—	25	150	—	
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$	±13	±14	—	±13	±14	—	V
		$R_L \geq 2k\Omega$, $V_S = \pm 15V$	±10	±12	—	±10	±12	—	
Power Consumption	P_d	$V_S = \pm 15V$	—	9	18	—	15	24	mW

NOTE:
1. Sample tested.

LOW-FREQUENCY NOISE TEST CIRCUIT (0.1 to 10Hz)



DICE CHARACTERISTICS (125° C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.043 inch, 2537 sq. mils
(1.50 × 1.09 mm, 1.64 sq. mm)

1. COMPENSATION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V−
6. OUTPUT
7. V+
8. COMPENSATION

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 20V$ and $T_A = 25°C$ for OP-08N and OP-08G devices; $V_S = \pm 20V$ and $T_A = 125°C$ for OP-08NT and OP-08GT devices; $V_S = \pm 15V$ and $T_A = 25°C$ for OP-08GR devices, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT LIMIT	OP-08N LIMIT	OP-08GT LIMIT	OP-08G LIMIT	OP-08GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1.0	mV MAX
Input Offset Current	I_{OS}		0.4	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		3	2	4	2	5	nA MAX
Input Voltage Range	IVR	$V_S = \pm 15V$	±13.5	±13.5	±13.5	±13.5	±13.5	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$ $V_S = \pm 15V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	μV/V MAX
Output Voltage Swing	V_O	$V_S = \pm 15V$ $R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 5k\Omega$	±13 — ±10	±13 ±10 —	±13 — ±10	±13 ±10 —	±13 ±10 —	V MIN
Large-Signal Voltage Gain $V_O = \pm 10V$	A_{VO}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$ $R_L \geq 5k\Omega$, $V_S = \pm 15V$	— — 40	80 50 —	— — 40	80 50 —	40 — —	V/mV MIN
Input Resistance	R_{IN}	Note 2	—	25	—	25	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$, $V_S = \pm 15V$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:
1. For 25° C characteristics of NT & GT devices, see N & G characteristics, respectively.
2. Guaranteed by input bias current.

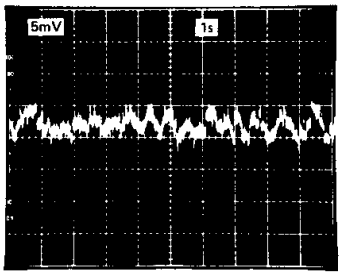
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-08NT TYPICAL	OP-08N TYPICAL	OP-08GT TYPICAL	OP-08G TYPICAL	OP-08GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	μV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	0.5	0.5	1.0	pA/°C

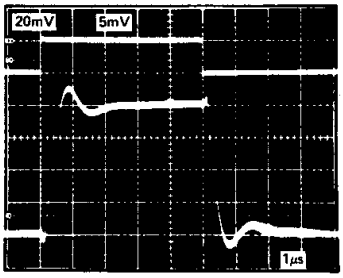
TYPICAL PERFORMANCE CHARACTERISTICS

LOW FREQUENCY NOISE

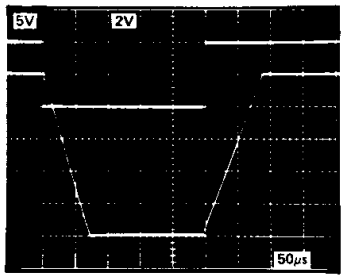


R_S = 0, BW = 0.1Hz TO 10Hz
5mV/DIV AT READOUT
0.5μV/DIV REFERRED TO INPUT

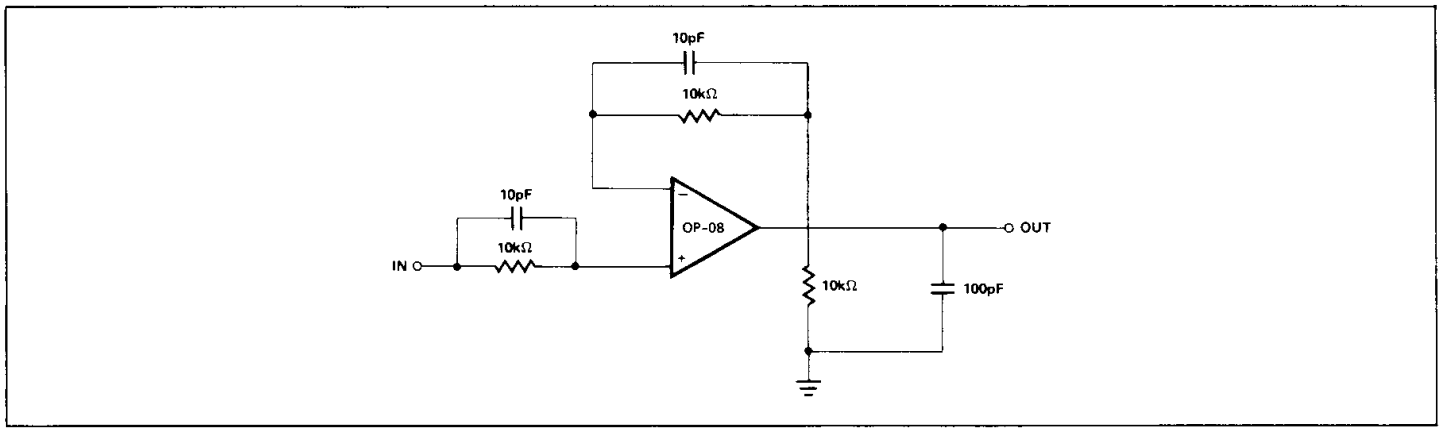
SMALL-SIGNAL TRANSIENT RESPONSE



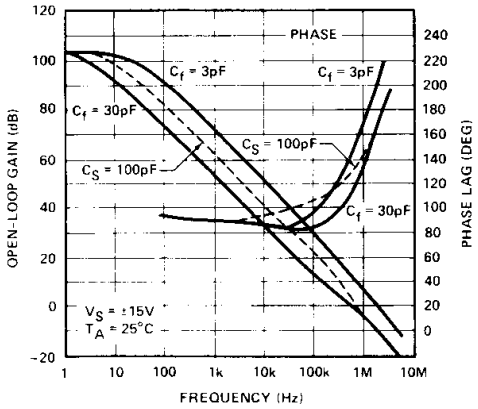
LARGE-SIGNAL TRANSIENT RESPONSE



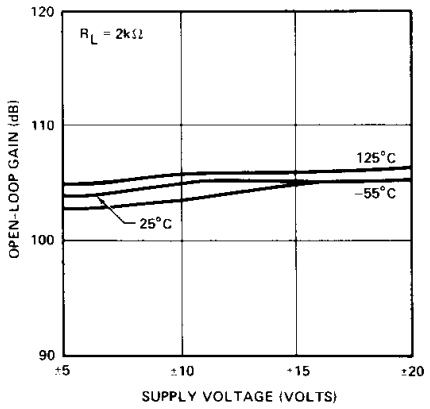
TRANSIENT RESPONSE TEST CIRCUIT



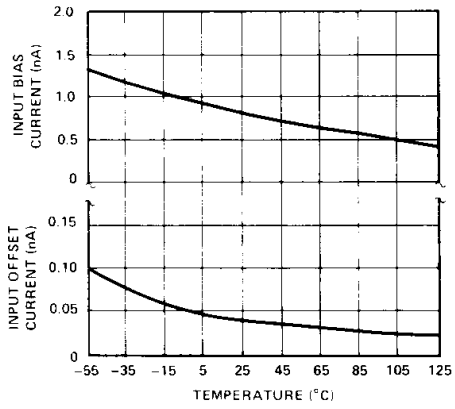
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



OPEN-LOOP GAIN vs SUPPLY VOLTAGE

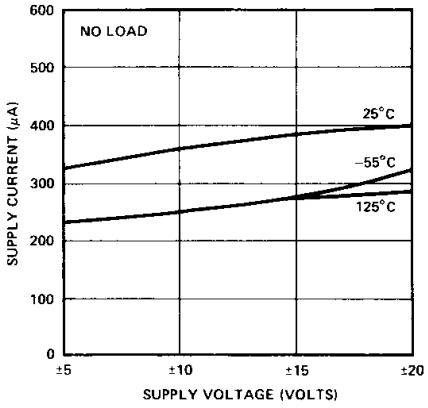


INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE

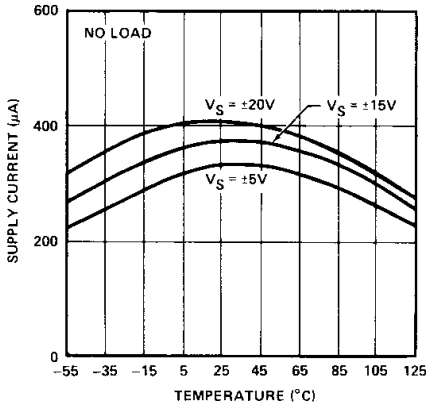


TYPICAL PERFORMANCE CHARACTERISTICS

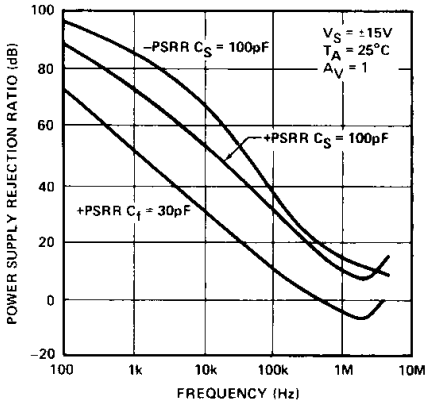
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION RATIO (PSRR) vs FREQUENCY



APPLICATIONS INFORMATION

The OP-08 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakage currents can produce significant errors, especially at high board temperatures. Careful attention to board layout and cleaning procedure is needed to take full advantage of the OP-08 performance. Board leakage is minimized by encircling the input pins with a guard ring maintained at the same potential as the inputs. This guard ring should be driven by a low impedance source, such as an amplifier's output or ground.

TYPICAL APPLICATION

BILATERAL CURRENT SOURCE