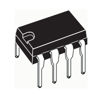
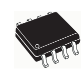
TS912

Rail-to-Rail CMOS Dual Operational Amplifier

- Rail-to-rail input and output voltage ranges
- Single (or dual) supply operation from 2.7V to 16V
- Extremely low input bias current: 1pA typ.
- Low input offset voltage: 2mV max.
- Specified for 600Ω and 100Ω loads
- Low supply current: 200µA/ampli (V_{CC} = 3V)
- Latch-up immunity
- ESD tolerance: 3kV
- Spice macromodel included in this specification

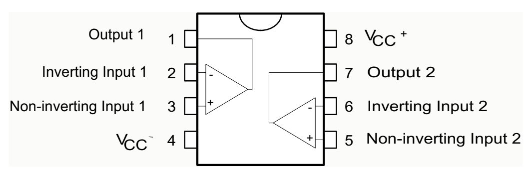


N
DIP-8
(Plastic Package)



D
SO-8
(Plastic Micropackage)

Pin connections (top view)



Description

The TS912 is a rail-to-rail CMOS dual operational amplifier designed to operate with a single or dual supply voltage.

The input voltage range V_{icm} includes the two supply rails V_{CC}^+ and V_{CC}^-.

The output reaches:

- V_{CC}^- +30mV, V_{CC}^+ -40mV, with R_L = 10kΩ
- V_{CC}^- +300mV, V_{CC}^+ -400mV, with R_L = 600Ω

This product offers a broad supply voltage operating range from 2.7V to 16V and a supply current of only 200µA/amp (V_{CC} = 3V).

Source and sink output current capability is typically 40mA (at V_{CC} = 3V), fixed by an internal limitation circuit.

1 Order Codes

Part Number	Temperature Range	Package	Packing	Marking
TS912IN	-40, +125°C	DIP8	Tube	TS912IN
TS912ID/IDT		SO-8	Tube or Tape & Reel	912I
TS912AIN		DIP8	Tube	TS912AIN
TS912AID/AIDT		SO-8	Tube or Tape & Reel	912AI
TS912BID/BIDT		SO-8		912BI
TS912IYD/IYDT		SO-8 (automotive grade level)		912IY
TS912AIYD/AIYDT				912AIY

2 Absolute Maximum Ratings and Operating Conditions

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	18	V_{CC}
Vid	Differential Input Voltage (2)	±18	Vid
V_i	Input Voltage (3)	-0.3 to 18	V_i
I_{in}	Current on Inputs	±50	I_{in}
I_o	Current on Outputs	±130	I_o
T_{oper}	Operating Free Air Temperature Range TS912I/AI/BI	-40 to + 125	T_{oper}
T_{stg}	Storage Temperature	-65 to +150	T_{stg}
T_j	Maximum Junction Temperature	150	T_j
R_{thja}	Thermal Resistance Junction to Ambient (4) DIP8 SO-8	 85 125	°C/W
R_{thjc}	Thermal Resistance Junction to Case DIP8 SO-8	 41 40	°C/W
ESD	HBM: Human Body Model(5)	3	kV
	MM: Machine Model(6)	200	V
	CDM: Charged Device Model	1500	kV

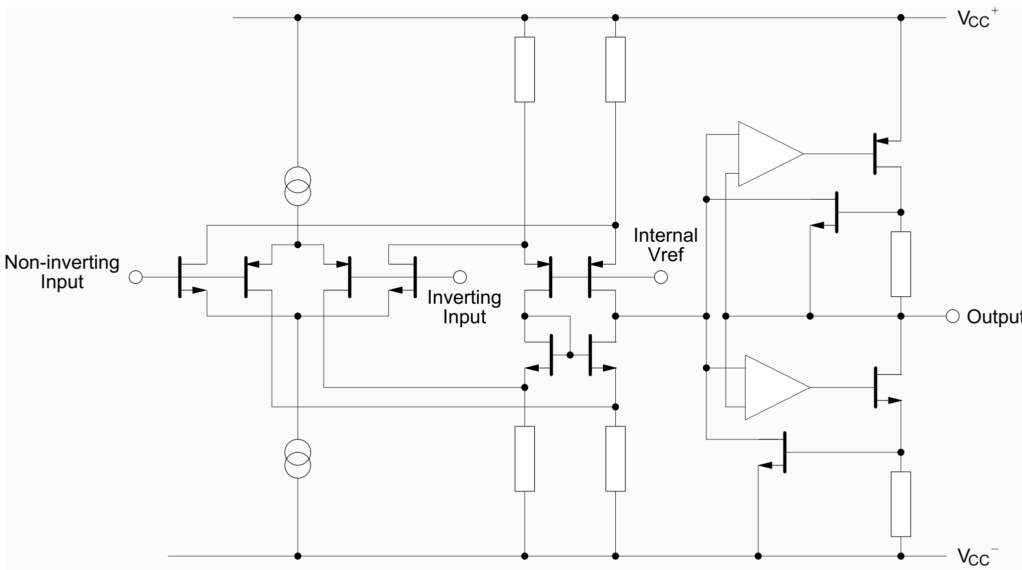
1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuit on all amplifiers. These values are typical.
5. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
6. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 16	V
V_{icm}	Common Mode Input Voltage Range	V_{CC}^- -0.2 to V_{CC}^+ +0.2	V

3 Typical Application Information

Figure 1. Schematic diagram (1/2 TS912)



4 Electrical Characteristics

Table 3. $V_{CC}^+ = 3V$, $V_{cc}^- = 0V$, R_L, C_L connected to $V_{CC/2}$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($V_{ic} = V_o = V_{CC/2}$)TS912 TS912A TS912B $T_{min.} \leq T_{amb} \leq T_{max.}$TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input Offset Voltage Drift		5		µV/°C
I_{io}	Input Offset Current (1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	100 200	pA
I_{ib}	Input Bias Current 1) $T_{min.} \leq T_{amb} \leq T_{max.}$		1	150 300	pA
I_{CC}	Supply Current (per amplifier, $A_{VCL} = 1$, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		200	300 400	µA
CMR	Common Mode Rejection Ratio $V_{ic} = 0$ to 3V, $V_o = 1.5V$		70		dB
SVR	Supply Voltage Rejection Ratio ($V_{CC}^+ = 2.7$ to 3.3V, $V_o = V_{CC/2}$)	50	80		dB
A_{vd}	Large Signal Voltage Gain ($R_L = 10k\Omega$, $V_o = 1.2V$ to 1.8V) $T_{min.} \leq T_{amb} \leq T_{max.}$	3 2	10		V/mV
V_{OH}	High Level Output Voltage ($V_{id} = 1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 10k\Omega$ $R_L = 600\Omega$	 2.95 2.9 2.3 2.8 2.1	 2.96 2.6 2		V
V_{OL}	Low Level Output Voltage ($V_{id} = -1V$) $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 600\Omega$ $R_L = 100\Omega$ $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 10k\Omega$ $R_L = 600\Omega$		 30 300 900	50 70 400 100 600	mV
I_o	Output Short Circuit Current ($V_{id} = \pm1V$) Source ($V_o = V_{CC}^-$) Sink ($V_o = V_{CC}^+$)	 20 20	 40 40		mA
GBP	Gain Bandwidth Product ($A_{VCL} = 100$, $R_L = 10k\Omega$, $C_L = 100pF$, f = 100kHz)		0.8		MHz
SR^+	Slew Rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to 1.7V)		0.4		V/µs
SR^-	Slew Rate ($A_{VCL} = 1$, $R_L = 10k\Omega$, $C_L = 100pF$, $V_i = 1.3V$ to 1.7V)		0.3		V/µs

Table 3. V_{CC}^{+} = 3V, V_{cc}^{-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ϕm	Phase Margin		30		Degrees
en	Equivalent Input Noise Voltage (R_s = 100Ω, f = 1kHz)		30		nV/√Hz

1. Maximum values including unavoidable inaccuracies of the industrial test

Table 4. V_{CC}^{+} = 5V, V_{cc}^{-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (V_{ic} = V_o = $V_{CC/2}$)TS912 TS912A TS912B $T_{min.} \le T_{amb} \le T_{max.}$TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input Offset Voltage Drift		5		µV/°C
I_{io}	Input Offset Current (1) $T_{min.} \le T_{amb} \le T_{max.}$		1	100 200	pA
I_{ib}	Input Bias Current 1) $T_{min.} \le T_{amb} \le T_{max.}$		1	150 300	pA
I_{CC}	Supply Current (per amplifier, A_{VCL} = 1, no load) $T_{min.} \le T_{amb} \le T_{max.}$		230	350 450	µA
CMR	Common Mode Rejection Ratio V_{ic} = 1.5 to 3.5V, V_o = 2.5V	60	85		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^{+} = 3 to 5V, V_o = $V_{CC/2}$)	55	80		dB
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_o = 1.5V to 3.5V) $T_{min.} \le T_{amb} \le T_{max.}$	10 7	40		V/mV
V_{OH}	High Level Output Voltage (V_{id} = 1V) R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 10kΩ R_L = 600Ω	 4.95 4.9 4.25 4.8 4.1	 4.95 4.55 3.7		V
V_{OL}	Low Level Output Voltage (V_{id} = -1V) R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 10kΩ R_L = 600Ω		 40 350 1400	50 100 500 150 750	mV
I_o	Output Short Circuit Current (V_{id} = ±1V) Source (V_o = V_{CC}^{-}) Sink (V_o = V_{CC}^{+})	 45 45	 65 65		mA
GBP	Gain Bandwidth Product (A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz)		1		MHz

Table 4. V_{CC}^{+} = 5V, V_{cc}^{-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
SR^+	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 1V to 4V)		0.8		
SR^-	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 1V to 4V)		0.6		V/µs
en	Equivalent Input Noise Voltage (R_s = 100Ω, f = 1kHz)		30		nV/√Hz
V_{O1}/V_{O2}	Channel Separation (f = 1kHz)		120		dB
φm	Phase Margin		30		Degrees

1. Maximum values including unavoidable inaccuracies of the industrial test

Table 5. V_{CC}^{+} = 10V, V_{cc}^{-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (V_{ic} = V_o = $V_{CC/2}$)TS912 TS912A TS912B $T_{min.} \le T_{amb} \le T_{max.}$TS912 TS912A TS912B			10 5 2 12 7 3	mV
ΔV_{io}	Input Offset Voltage Drift		5		µV/°C
I_{io}	Input Offset Current (1) $T_{min.} \le T_{amb} \le T_{max.}$		1	100 200	pA
I_{ib}	Input Bias Current 1) $T_{min.} \le T_{amb} \le T_{max.}$		1	150 300	pA
I_{CC}	Supply Current (per amplifier, A_{VCL} = 1, no load) $T_{min.} \le T_{amb} \le T_{max.}$		400	600 700	µA
CMR	Common Mode Rejection Ratio V_{ic} = 3 to 7V, V_o = 5V V_{ic} = 0 to 10V, V_o = 5V	 60 50	 90 75		dB
SVR	Supply Voltage Rejection Ratio (V_{CC}^{+} = 5 to 10V, V_o = $V_{CC/2}$)	60	90		dB
A_{vd}	Large Signal Voltage Gain (R_L = 10kΩ, V_o = 2.5V to 7.5V) $T_{min.} \le T_{amb} \le T_{max.}$	15 10	50		V/mV
V_{OH}	High Level Output Voltage (V_{id} = 1V) R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 10kΩ R_L = 600Ω	 9.95 9.85 9 9.8 8.8	 9.95 9.35 7.8		V

Table 5. V_{CC}^{+} = 10V, V_{cc}^{-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage (V_{id} = -1V) R_L = 100kΩ R_L = 10kΩ R_L = 600Ω R_L = 100Ω $T_{min.} \le T_{amb} \le T_{max.}$ R_L = 10kΩ R_L = 600Ω		 50 650 2300	 50 150 800 150 900	mV
I_o	Output Short Circuit Current (V_{id} = ±1V) Source ($V_o = V_{CC}^{-}$) Sink ($V_o = V_{CC}^{+}$)	 45 50	 65 75		mA
GBP	Gain Bandwidth Product (A_{VCL} = 100, R_L = 10kΩ, C_L = 100pF, f = 100kHz)		1.4		MHz
SR^{+}	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 2.5V to 7.5V)		1.3		V/µs
SR^{-}	Slew Rate (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_i = 2.5V to 7.5V)		0.8		
φm	Phase Margin		40		Degrees
en	Equivalent Input Noise Voltage (R_s = 100Ω, f = 1kHz)		30		nV/√Hz
THD	Total Harmonic Distortion (A_{VCL} = 1, R_L = 10kΩ, C_L = 100pF, V_o = 4.75V to 5.25V, f = 1kHz)		0.02		%
C_{in}	Input Capacitance		1.5		pF

1. Maximum values including unavoidable inaccuracies of the industrial test

Figure 2. Supply current (each amplifier) vs. supply voltage

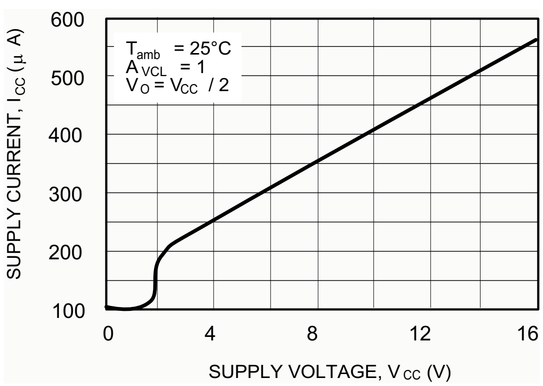


Figure 3. High level output voltage vs. high level output current

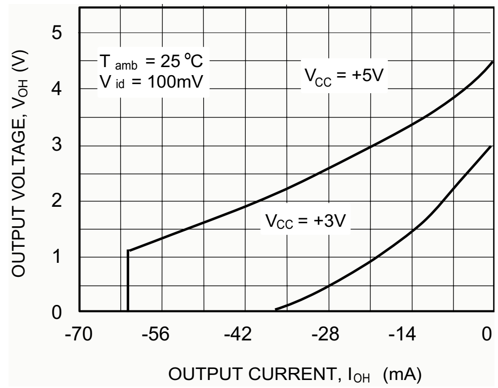


Figure 4. Low level output voltage vs. low level output current

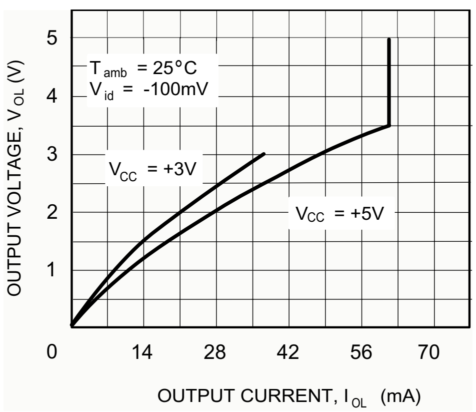


Figure 5. Input bias current vs. temperature

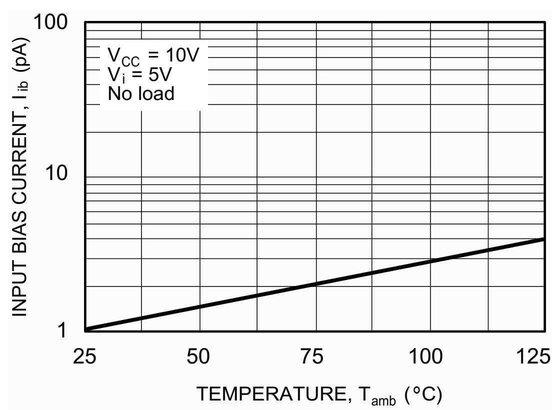


Figure 6. High level output voltage vs. high level output current

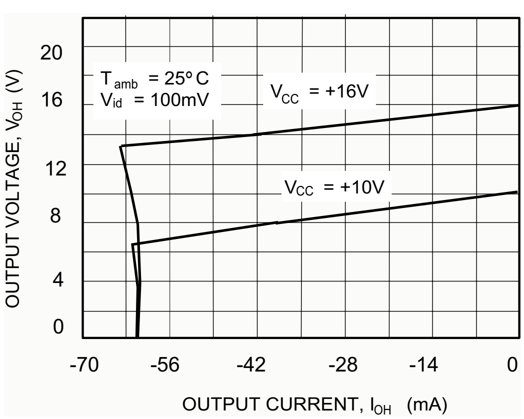


Figure 7. Low level output voltage vs. low level output current

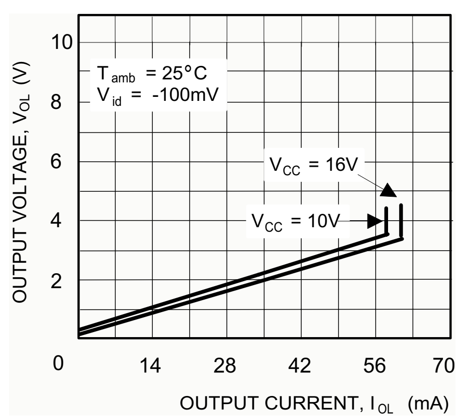


Figure 8. Gain and phase vs. frequency

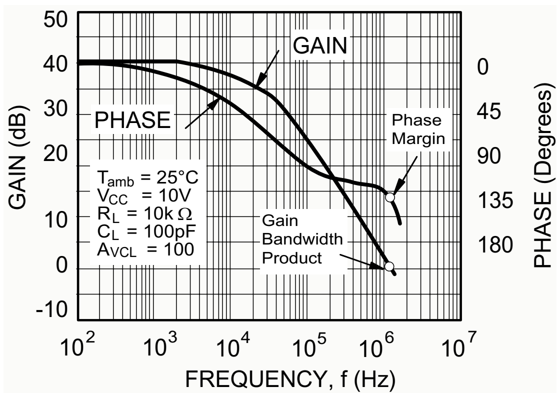


Figure 9. Gain bandwidth product vs. supply voltage

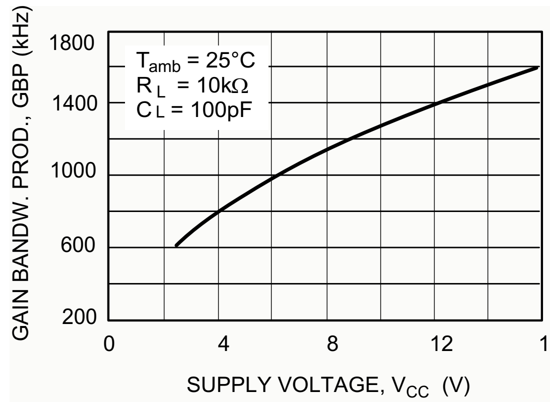


Figure 10. Phase margin vs. supply voltage

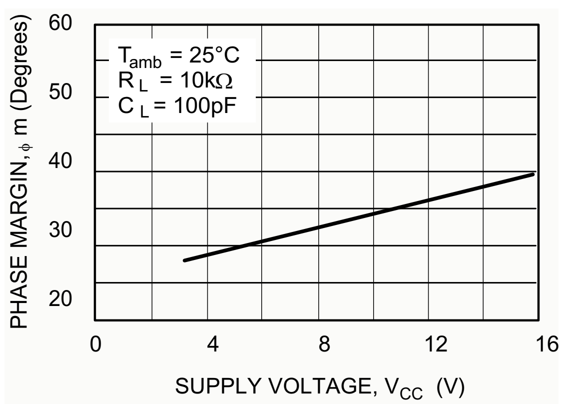


Figure 11. Gain and phase vs. frequency

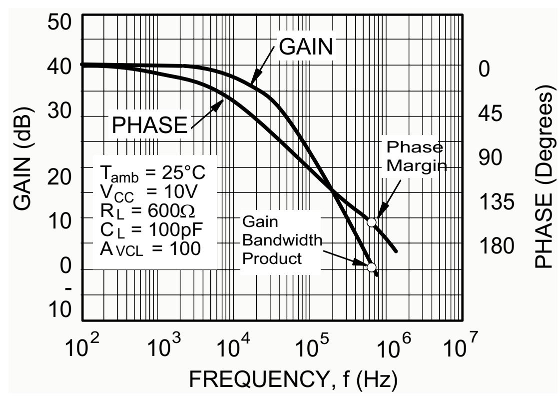


Figure 12. Gain bandwidth product vs. supply voltage

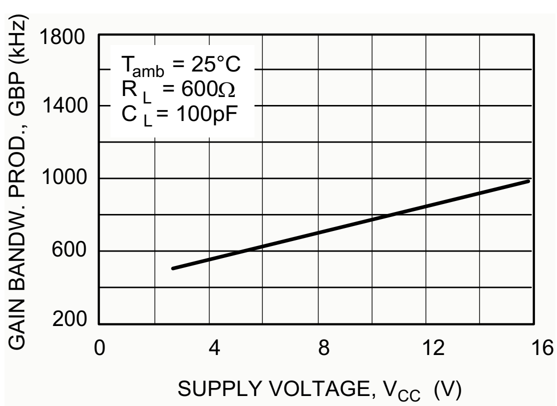


Figure 13. Phase margin vs. supply voltage

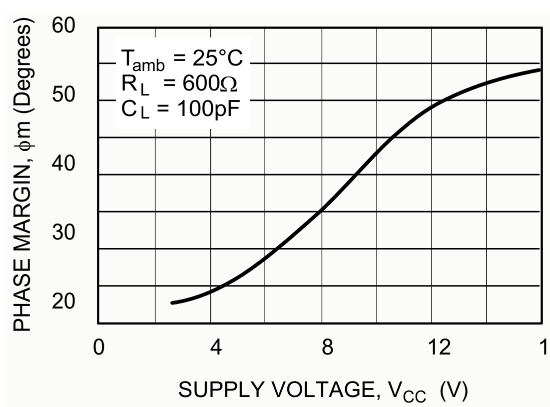
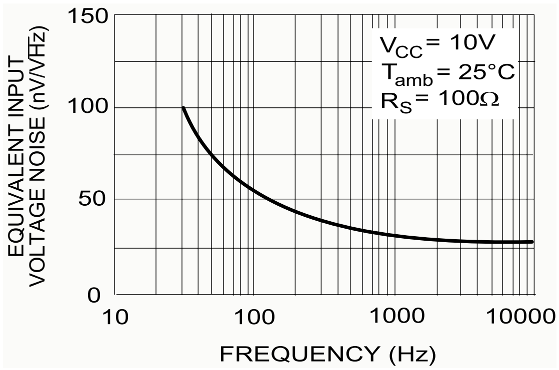


Figure 14. Input voltage noise vs. frequency



5 Macromodels

5.1 Important note concerning this macromodel

Please consider following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.
- Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc.) or even worse: outside of the device operating conditions (Vcc, Vicm, etc.) are not reliable in any way.

In *Section 5.2* and *Section 5.4*, the electrical characteristics resulting from the use of these macromodels are presented.

5.2 Electrical characteristics from macromodelization

Table 6. Electrical characteristics resulting from macromodel simulation at $V_{CC}^+ = 3V$, $V_{CC}^- = 0V$, R_L, C_L connected to $V_{CC/2}$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 10k\Omega$	10	V/mV
I_{CC}	No load, per operator	200	µA
V_{icm}		-0.2 to 3.2	V
V_{OH}	$R_L = 10k\Omega$	2.96	V
V_{OL}	$R_L = 10k\Omega$	30	mV
I_{sink}	$V_O = 3V$	40	mA
I_{source}	$V_O = 0V$	40	mA
GBP	$R_L = 10k\Omega$, $C_L = 100pF$	0.8	MHz
SR	$R_L = 10k\Omega$, $C_L = 100pF$	0.3	V/µs

5.3 Macromodel code

Applies to: TS912 (V_{cc} = 3V)

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
```

```
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT TS912_3 1 3 2 4 5 (analog)
*****************************************************
*****
.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 6.500000E+00
RIN 15 16 6.500000E+00
RIS 11 15 1.271505E+01
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 4.000000E-05
CPS 11 15 2.125860E-08
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.000000E+00
FCP 4 5 VOFP 5.000000E+00
FCN 5 4 VOFN 5.000000E+00
* AMPLIFYING STAGE
FIP 5 19 VOFP 2.750000E+02
FIN 5 19 VOFN 2.750000E+02
RG1 19 5 1.916825E+05
RG2 19 4 1.916825E+05
CC 19 29 2.200000E-08
HZTP 30 29 VOFP 1.3E+03
HZTN  5 30 VOFN 1.3E+03
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 3800
VIPM 28 4 150
HONM 21 27 VOUT 3800
VINM 5 27 150
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 75
COUT 3 5 1.000000E-12
DOP 19 68 MDTH 400E-12
VOP 4 25 1.724
HSCP 68 25 VSCP1 0.8E8
DON 69 19 MDTH 400E-12
VON 24 5 1.7419107
HSCN 24 69 VSCN1 0.8E+08
VSCTHP 60 61 0.0875
** VSCTHP = le seuil au dessus de vio * 500
** c.a.d 275U-000U dus a l'offset
DSCP1 61 63 MDTH 400E-12
VSCP1 63 64 0
ISCP 64 0 1.000000E-8
DSCP2 0 64 MDTH 400E-12
DSCN2 0 74 MDTH 400E-12
ISCN 74 0 1.000000E-8
VSCN1 73 74 0
DSCN1 71 73 MDTH 400E-12
VSCTHN 71 70 -0.55
** VSCTHN = le seuil au dessous de vio * 2000
```

```
** c.a.d -375U-000U dus a l'offset
ESCP 60 0 2 1 500
ESCN 70 0 2 1 -2000
.ENDS
```

5.4 Electrical characteristics from macromodelization

Table 7. Electrical characteristics resulting from macromodel simulation at V_{CC}^+ = 5V, V_{CC^-} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10kΩ	50	V/mV
I_{CC}	No load, per operator	230	µA
V_{icm}		-0.2 to 5.2	V
V_{OH}	R_L = 10kΩ	4.95	V
V_{OL}	R_L = 10kΩ	40	mV
I_{sink}	V_O = 5V	65	mA
I_{source}	V_O = 0V	65	mA
GBP	R_L = 10kΩ, C_L = 100pF	1	MHz
SR	R_L = 10kΩ, C_L = 100pF	0.8	V/µs

5.5 Macromodel code

Applies to: TS912 (V_{cc} = 5V)

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
* 6 STANDBY
.SUBCKT TS912_5 1 3 2 4 5 (analog)
*****************************************************
*****
.MODEL MDTH D IS=1E-8 KF=6.564344E-14 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 6.500000E+00
RIN 15 16 6.500000E+00
RIS 11 15 7.322092E+00
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 4.000000E-05
CPS 11 15 2.498970E-08
DINN 17 13 MDTH 400E-12
```

```
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.000000E+00
FCP 4 5 VOFP 5.750000E+00
FCN 5 4 VOFN 5.750000E+00
ISTB0 5 4 500N
* AMPLIFYING STAGE
FIP 5 19 VOFP 4.400000E+02
FIN 5 19 VOFN 4.400000E+02
RG1 19 5 4.904961E+05
RG2 19 4 4.904961E+05
CC 19 29 2.200000E-08
HZTP 30 29 VOFP 1.8E+03
HZTN  5 30 VOFN 1.8E+03
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 3800
VIPM 28 4 230
HONM 21 27 VOUT 3800
VINM 5 27 230
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 82
COUT 3 5 1.000000E-12
DOP 19 68 MDTH 400E-12
VOP 4 25 1.724
HSCP 68 25 VSCP1 0.8E+08
DON 69 19 MDTH 400E-12
VON 24 5 1.7419107
HSCN 24 69 VSCN1 0.8E+08
VSCTHP 60 61 0.0875
** VSCTHP = le seuil au dessus de vio * 500
** c.a.d 275U-000U dus a l'offset
DSCP1 61 63 MDTH 400E-12
VSCP1 63 64 0
ISCP 64 0 1.000000E-8
DSCP2 0 64 MDTH 400E-12
DSCN2 0 74 MDTH 400E-12
ISCN 74 0 1.000000E-8
VSCN1 73 74 0
DSCN1 71 73 MDTH 400E-12
VSCTHN 71 70 -0.55
** VSCTHN = le seuil au dessous de vio * 2000
** c.a.d -375U-000U dus a l'offset
ESCP 60 0 2 1 500
ESCN 70 0 2 1 -2000
.ENDS
```

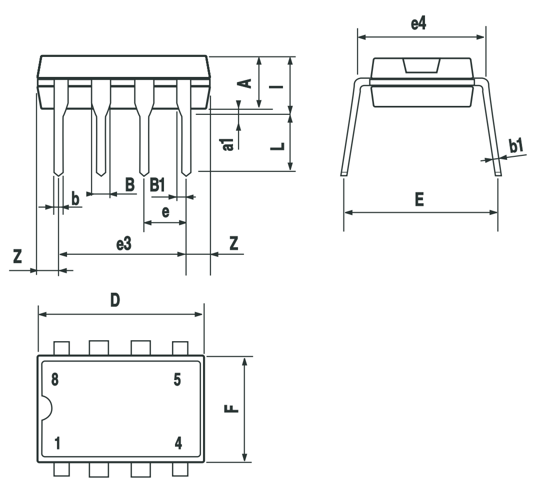
6 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.1 DIP-8 Package

Plastic DIP-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

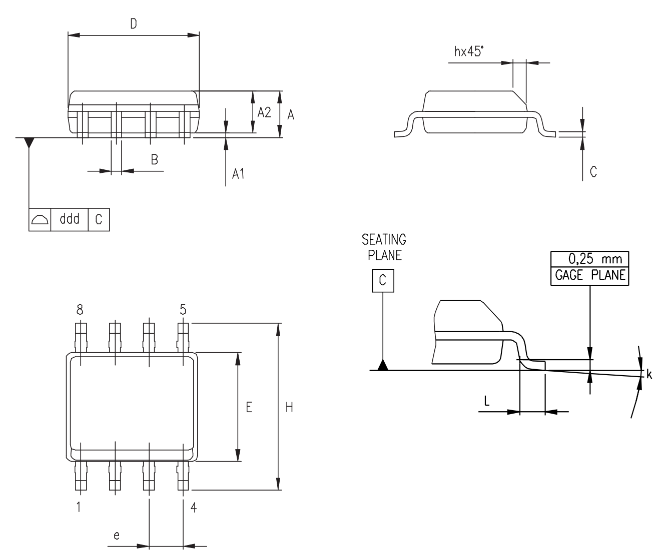


P001F

6.2 SO-8 Package

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



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7 Revision History

Table 8. Document revision history

Date	Revision	Changes
Dec. 2001	1	First Release
July 2005	2	1 - PPAP references inserted in the datasheet see *Table : on page 1* 2 - ESD protection inserted in *Table I: Key parameters and their absolute maximum ratings on page 2*
Oct. 2005	3	The following changes were made in this revision: – Some errors in the Order Codes table was corrected *on page 1*. – Reorganization of *Chapter 5: Macromodels on page 12*.
Feb. 2006	4	– Parameters added in *Table 1. on page 3* (T_j, ESD, R_{thja}, R_{thjc}).