SupIRBuck™

USER GUIDE FOR IR3898 EVALUATION BOARD 1.2Vout

DESCRIPTION

The IR3898 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 4mm X 5 mm Power QFN package.

Key features offered by the IR3898 include internal Digital Soft Start/Soft Stop, precision 0.5Vreference voltage, Power Good, thermal protection, programmable switching frequency, Enable input, input under-voltage lockout for proper start-up, enhanced line/ load regulation with feed forward, external frequency synchronization with smooth clocking, internal LDO and pre-bias start-up.

Output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous Mosfet for optimum cost and performance and the current limit is thermally compensated.

This user guide contains the schematic and bill of materials for the IR3898 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3898 is available in the IR3898 data sheet.

BOARD FEATURES

- V_{in} = +12V (+ 13.2V Max)
- V_{out} = +1.2V @ 0- 6A
- F_s=600kHz
- L= 1.0uH
- C_{in}= 3x10uF (ceramic 1206) + 1X330uF (electrolytic)
- C_{out}=4x22uF (ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +12V input supply should be connected to VIN+ and VIN-. A maximum of 6A load should be connected to VOUT+ and VOUT-. The inputs and output connections of the board are listed in Table I.

IR3898 has only one input supply and internal LDO generates Vcc from Vin. If operation with external Vcc is required, then R15 can be removed and external Vcc can be applied between Vcc+ and Vcc- pins. Vin pin and Vcc/LDO_Out pins should be shorted together for external Vcc operation.

The output can track voltage at the Vp pin. For this purpose, Vref pin is to be connected to ground (use zero ohm resistor for R21). The value of R14 and R28 can be selected to provide the desired tracking ratio between output voltage and the tracking input.

Table I. Connections

Connection	Signal Name
VIN+	Vin (+12V)
VIN-	Ground of Vin
Vout+	Vout(+1.2V)
Vout-	Ground for Vout
Vcc+	Vcc/ LDO_Out Pin
Vcc-	Ground for Vcc input
Enable	Enable
PGood	Power Good Signal
AGnd	Analog ground

LAYOUT

The PCB is a 4-layer board (2.23”x2”) using FR4 material. All layers use 2 Oz. copper. The PCB thickness is 0.062”. The IR3898 and other major power components are mounted on the top side of the board.

Power supply decoupling capacitors, the bootstrap capacitor and feedback components are located close to IR3898. The feedback resistors are connected to the output at the point of regulation and are located close to the SupIRBuck IC. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

Connection Diagram

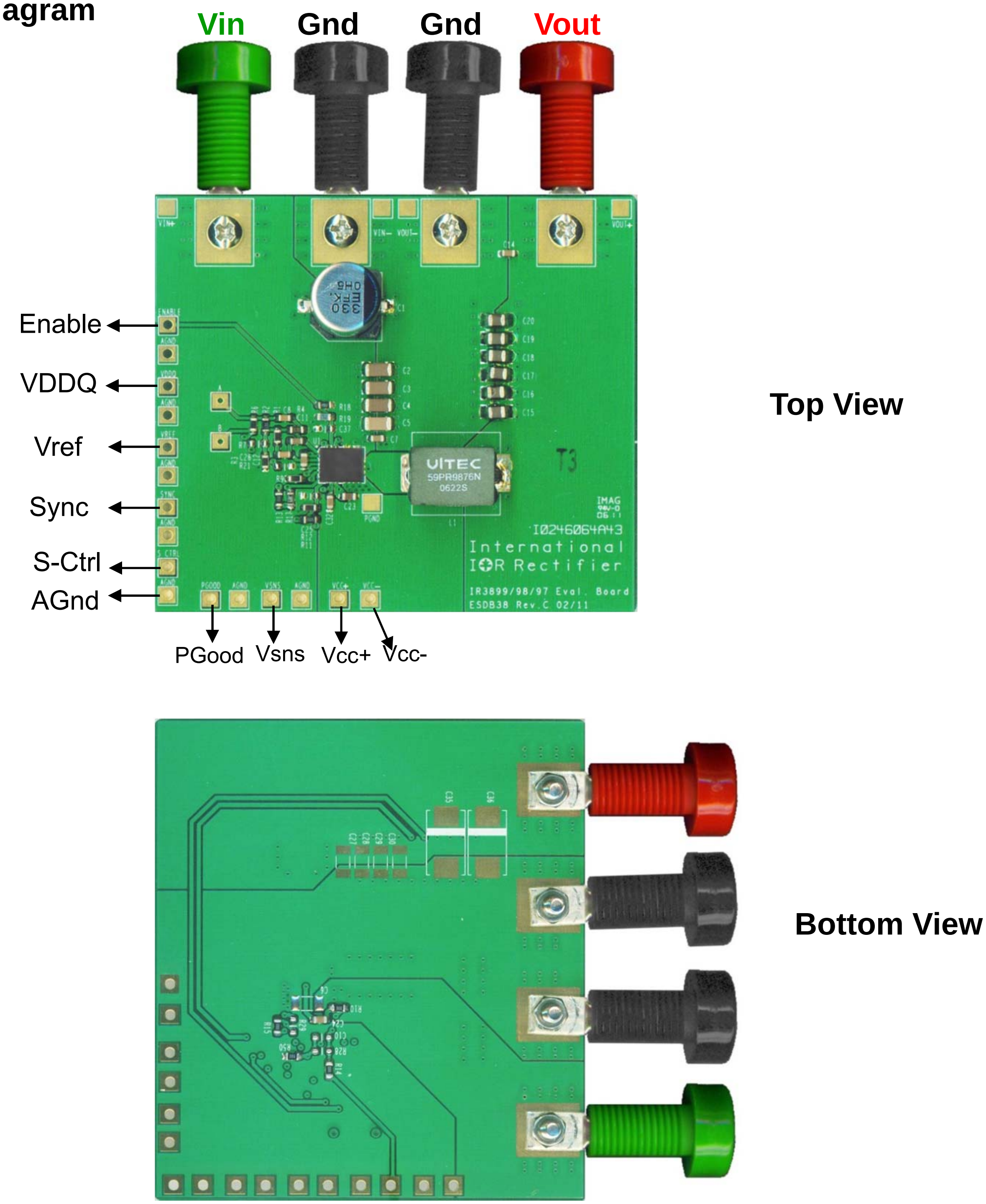


Fig. 1: Connection Diagram of IR3899/98/97 Evaluation Boards

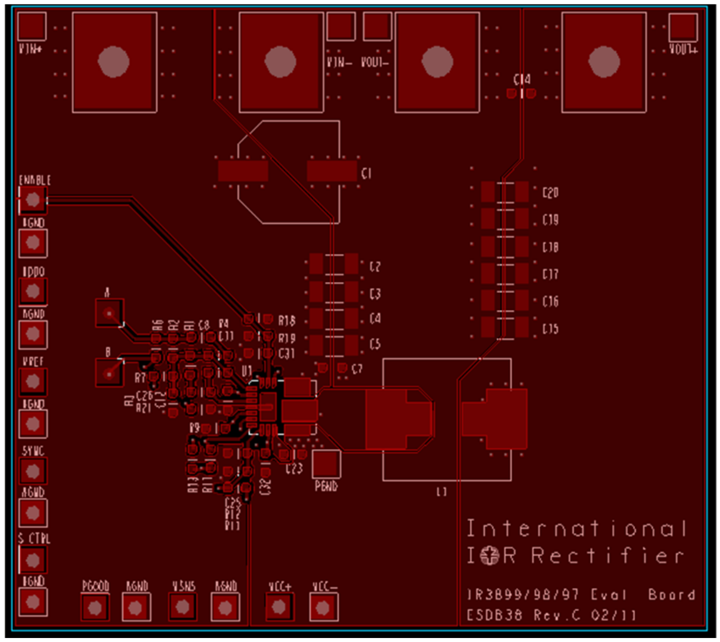


Fig. 2: Board Layout-Top Layer

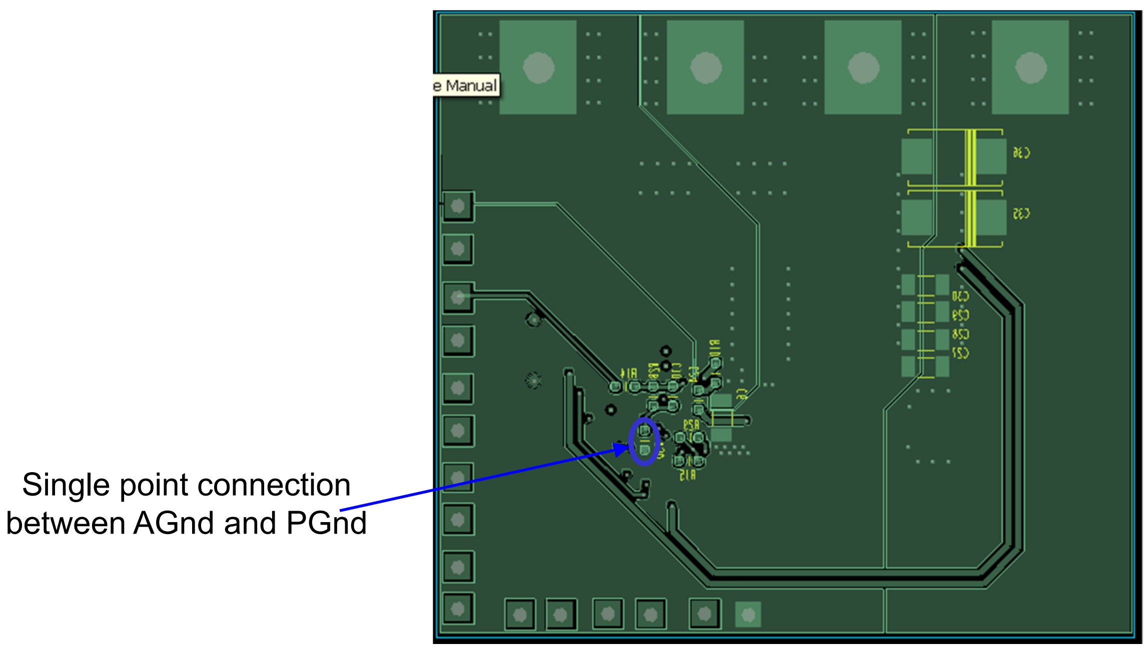


Fig. 3: Board Layout-Bottom Layer

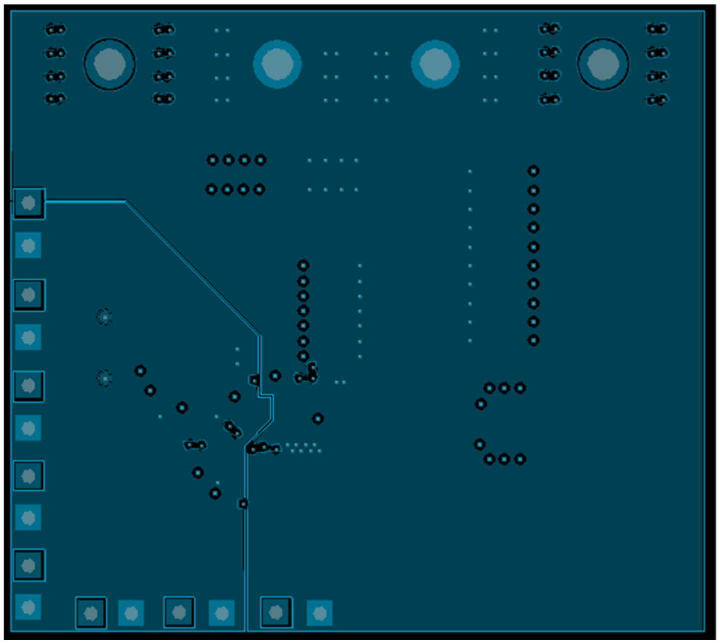


Fig. 4: Board Layout-Mid Layer 1

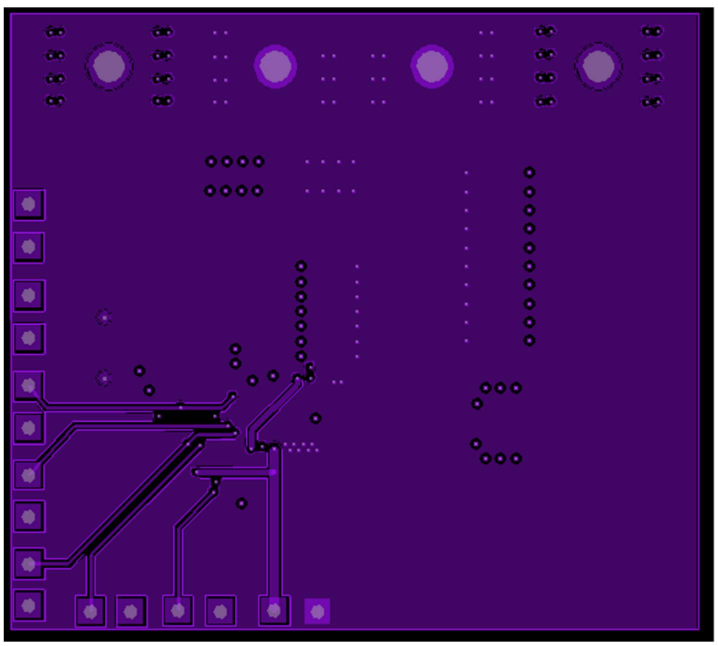


Fig. 5: Board Layout-Mid Layer 2

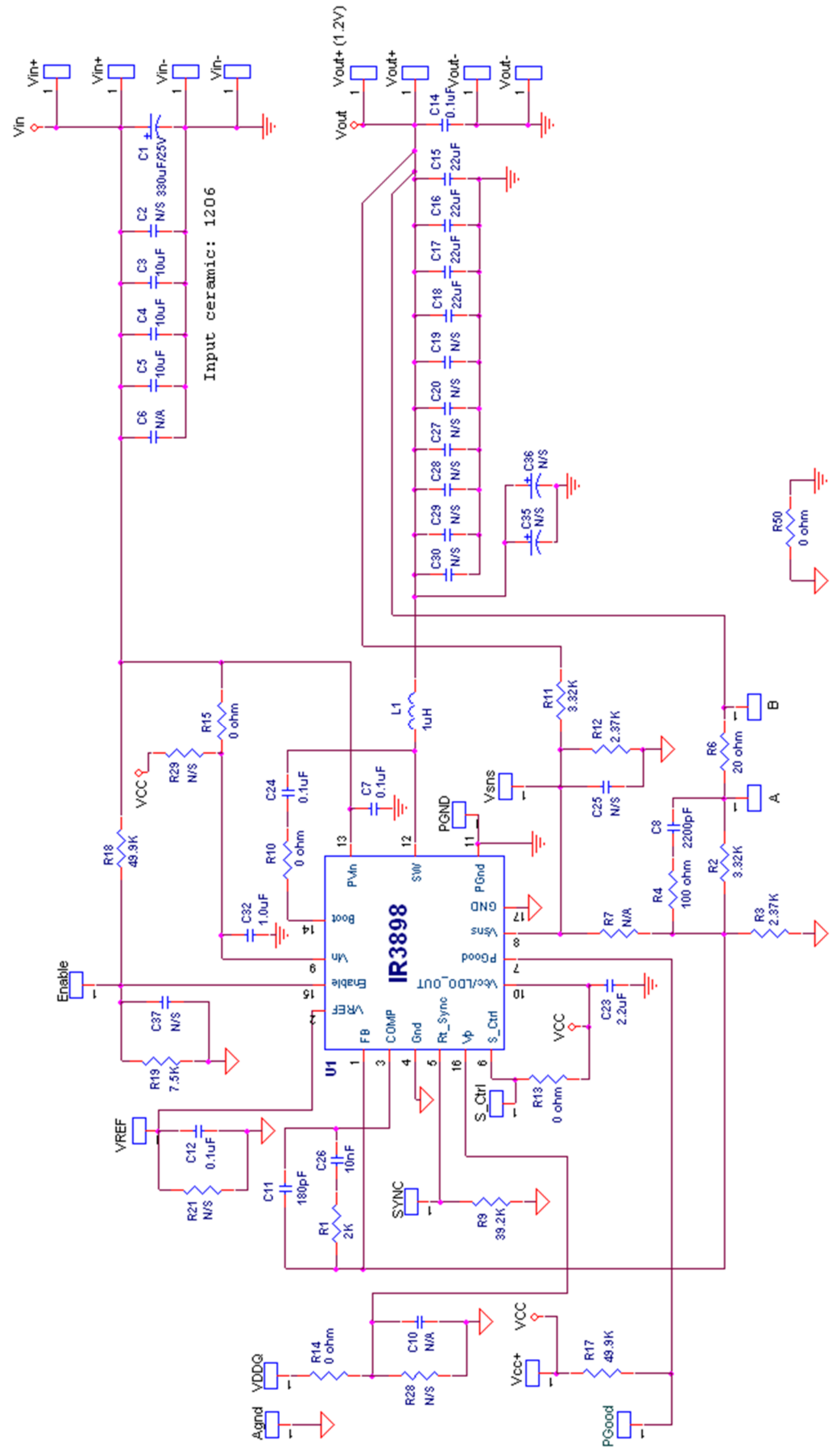


Fig. 6: Schematic of the IR3898 evaluation board

Bill of Materials

Item	Qty	Part Reference	Value	Description	Manufacturer	Part Number
1	1	C1	330uF	SMD Electrolytic F size 25V 20%	Panasonic	EEV-FK1E331P
2	3	C3 C4 C5	10uF	1206, 25V, X5R, 20%	TDK	C3216X5R1E106M
3	4	C7 C12 C14 C24	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
4	1	C8	2200pF	0603,50V,X7R	Murata	GRM188R71H222KA01B
5	1	C11	180pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H181JA01D
6	4	C15 C16 C17 C18	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
7	1	C23	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
8	1	C26	10nF	0603, 25V, X7R, 10%	Murata	GRM188R71E103KA01J
9	1	C32	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
10	1	L1	1.0uH	SMD 7.1x6.5x5mm,4.7mΩ	TDK	SPM6550T-1R0
11	1	R1	2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF2001V
12	2	R2 R11	3.32K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3321V
13	2	R3 R12	2.37K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF2371V
14	1	R4	100	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1000V
15	1	R6	20	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF20R0V
16	1	R9	39.2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3922V
17	5	R10 R13 R14 R15 R50	0	Thick Film, 0603,1/10W	Panasonic	ERJ-3GEY0R00V
18	2	R17 R18	49.9K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
19	1	R19	7.5K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF7501V
20	1	U1	IR3898	PQFN 4x5mm	IR	IR3898MPBF

TYPICAL OPERATING WAVEFORMS

Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, no airflow

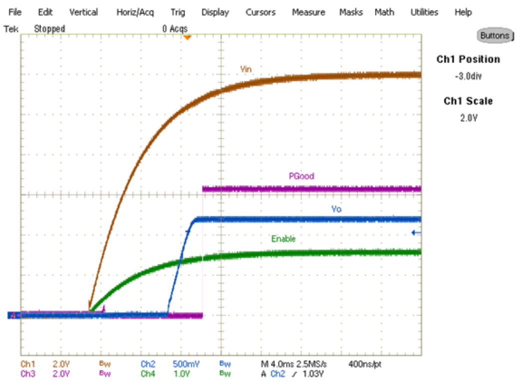


Fig. 7: Start up at 6A Load
Ch_1:V_{in}, Ch_2:V_o, Ch_3:P_{Good} Ch_4:Enable

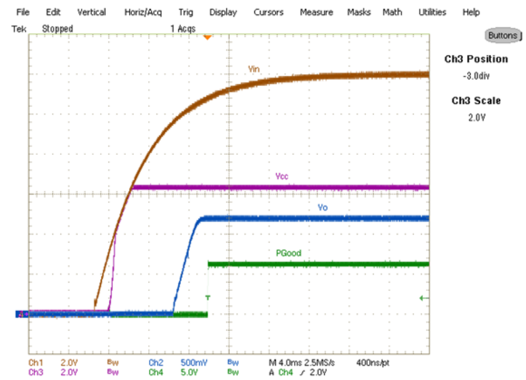


Fig. 8: Start up at 6A Load,
Ch_1:V_{in}, Ch_2:V_o, Ch_3:Vcc, Ch_4:P_{Good}

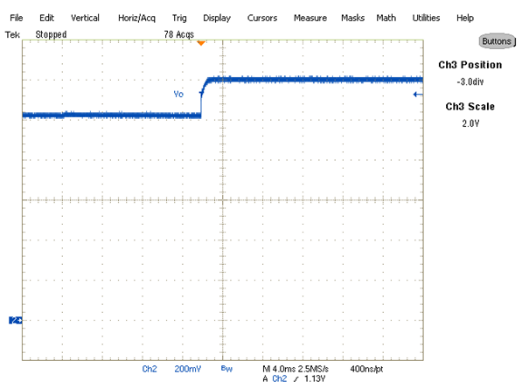


Fig. 9: Start up with 1V Pre Bias , 0A Load,
Ch_2:V_o

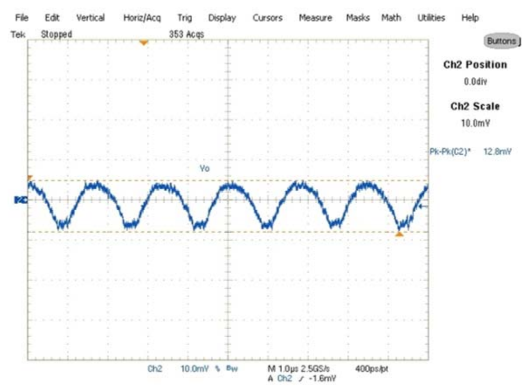


Fig. 10: Output Voltage Ripple, 6A load
Ch_2: V_{out}

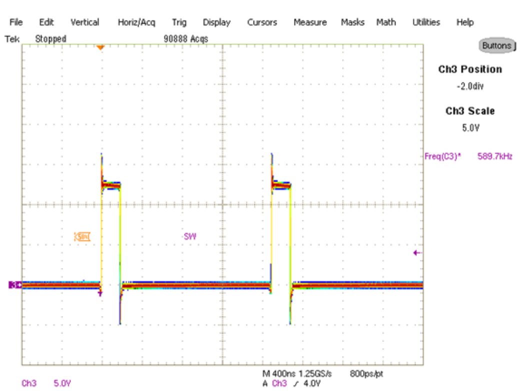


Fig. 11: Inductor node at 6A load
Ch_3:LX

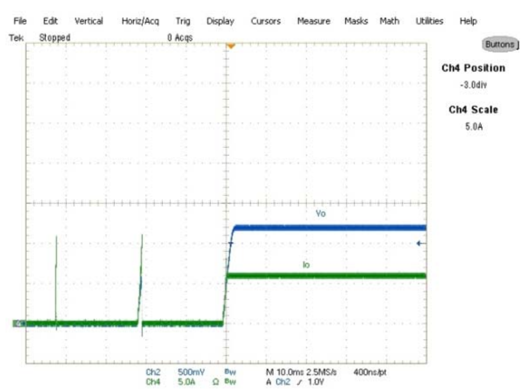


Fig. 12: Short circuit (Hiccup) Recovery
Ch_2:V_{out} , Ch4:Iout

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, no air flow

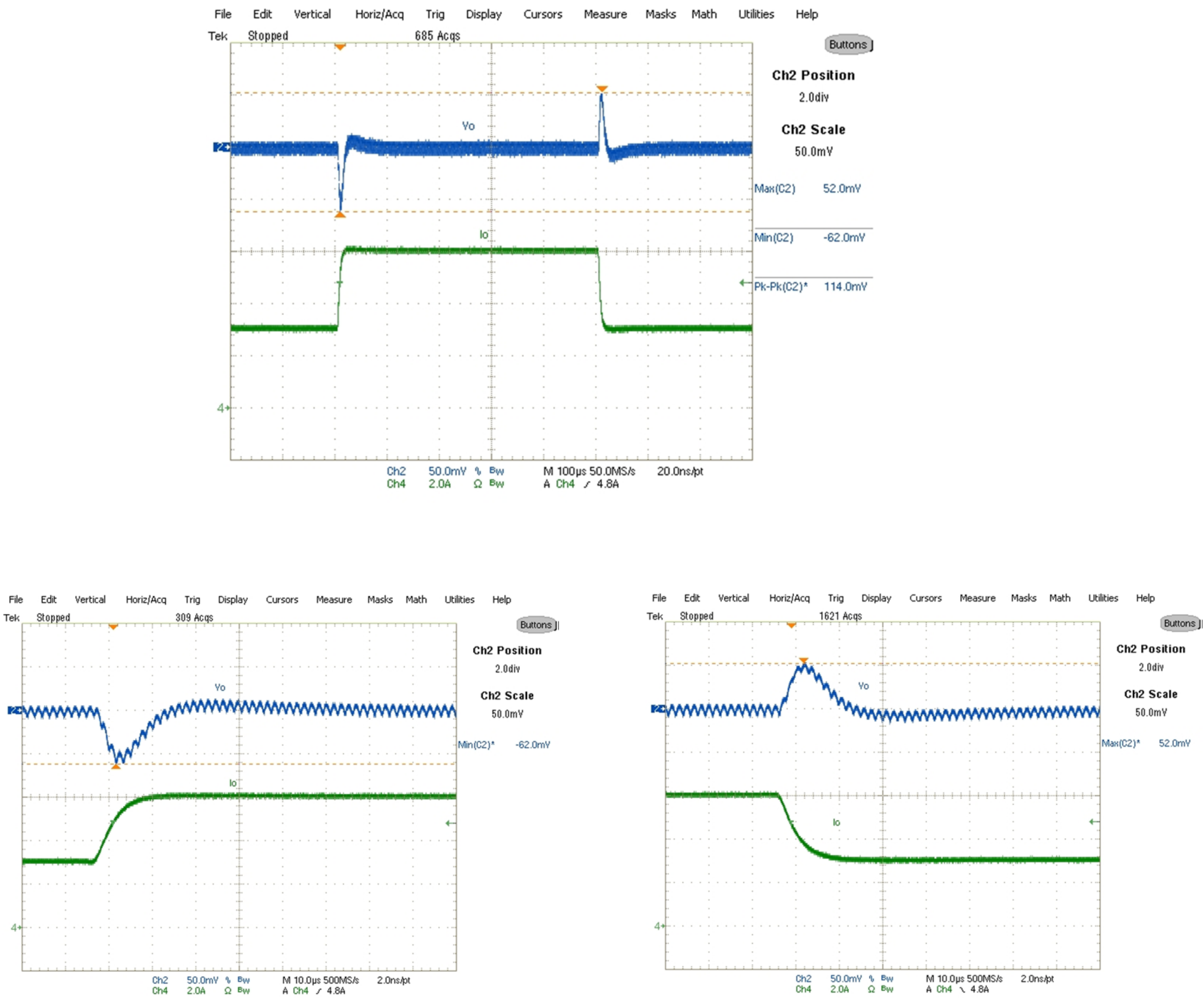


Fig. 13: Transient Response, 3A to 6A step
Ch_2:V_{out} Ch4-Iout

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, no air flow

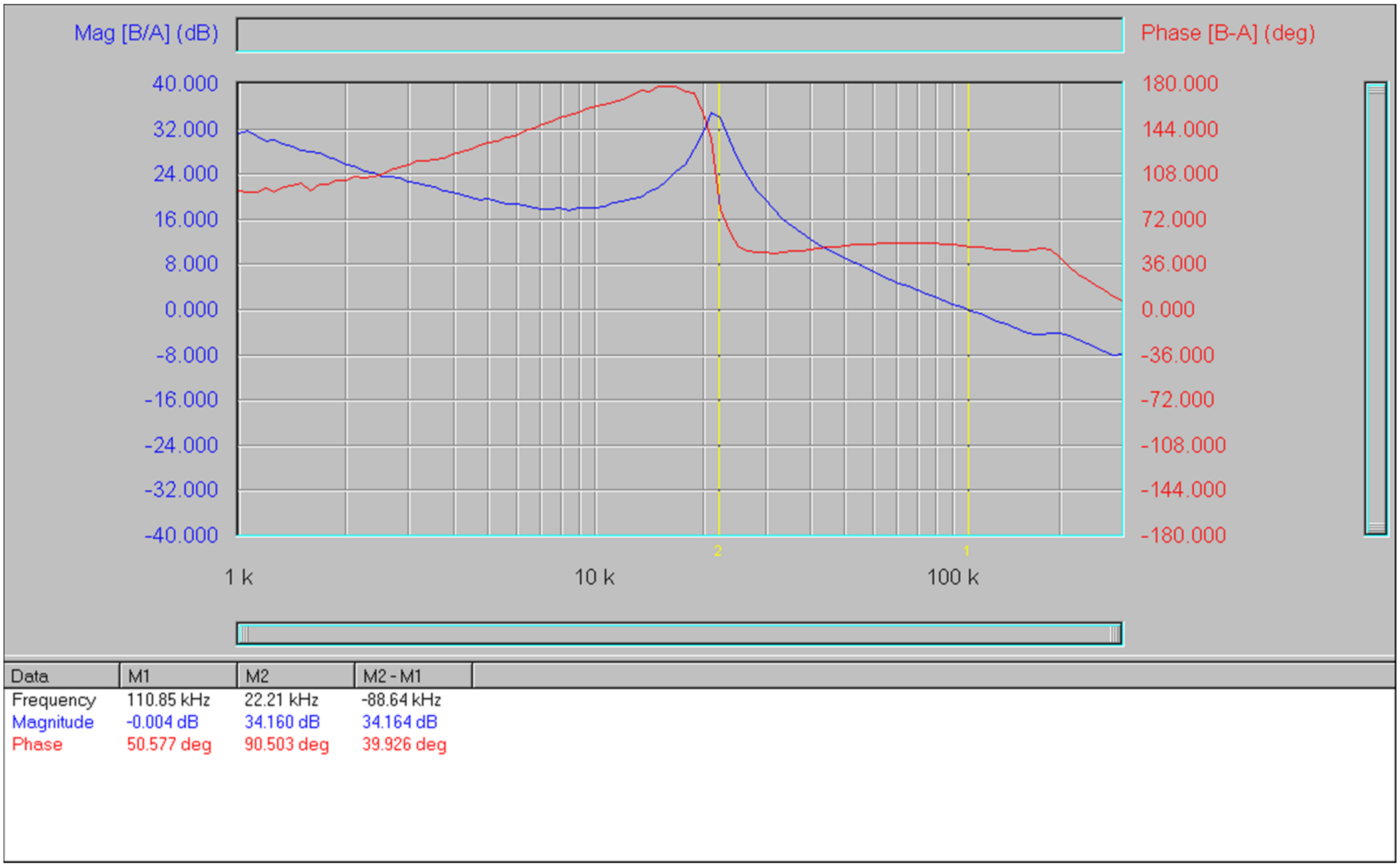


Fig. 14: Bode Plot at 6A load shows a bandwidth of 110.8KHz and phase margin of 50.5 degrees

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, no air flow

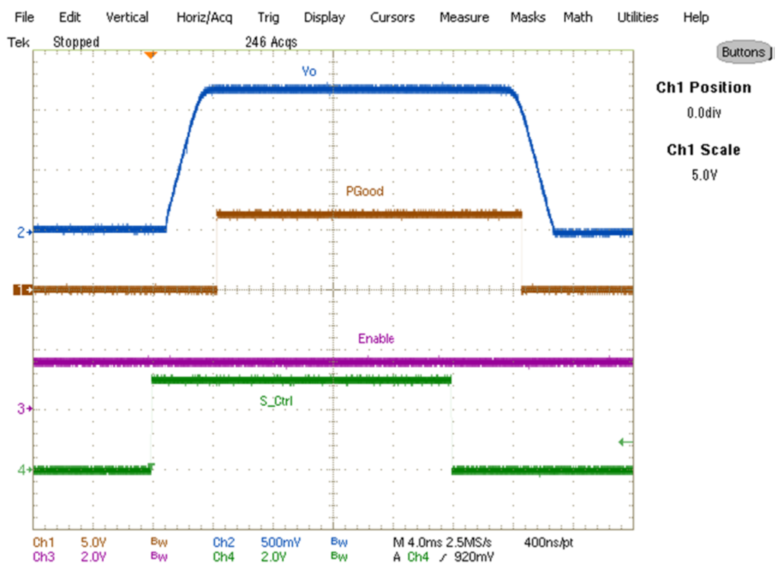


Fig (15) Soft start and soft stop using S_Ctrl pin

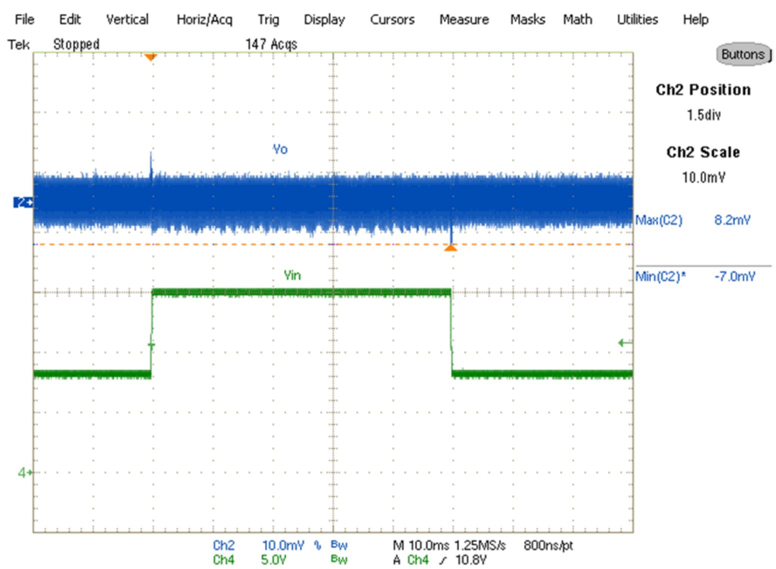


Fig (16) Feed Forward for Vin change from 7 to 16V and back to 7V
Ch_2-Vout Ch_4-Vin

TYPICAL OPERATING WAVEFORMS
Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, no air flow

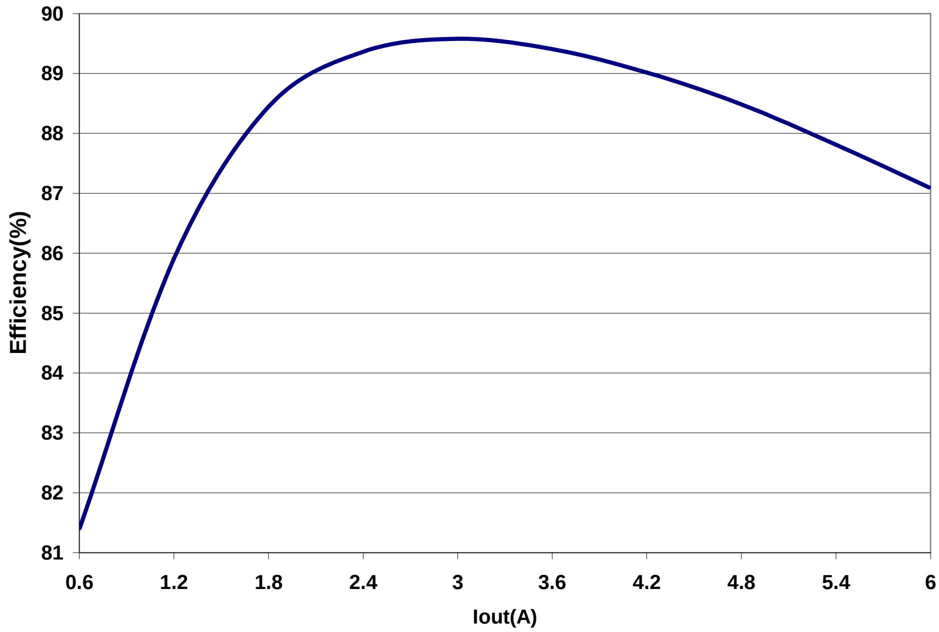


Fig.17: Efficiency versus load current

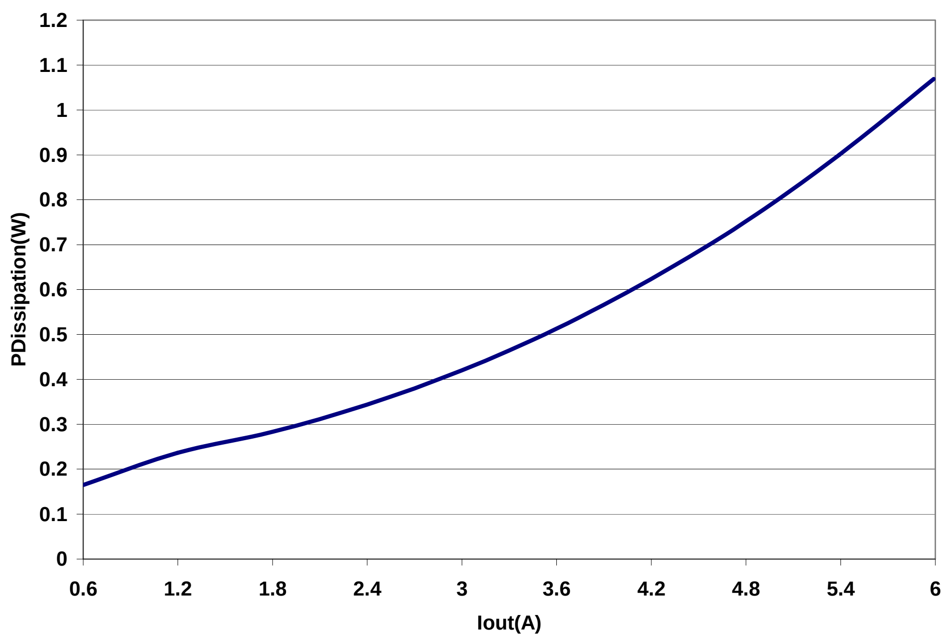


Fig.18: Power loss versus load current

THERMAL IMAGES
Vin=12.0V, Vo=1.2V, Io=0-6A, Room Temperature, No Air flow

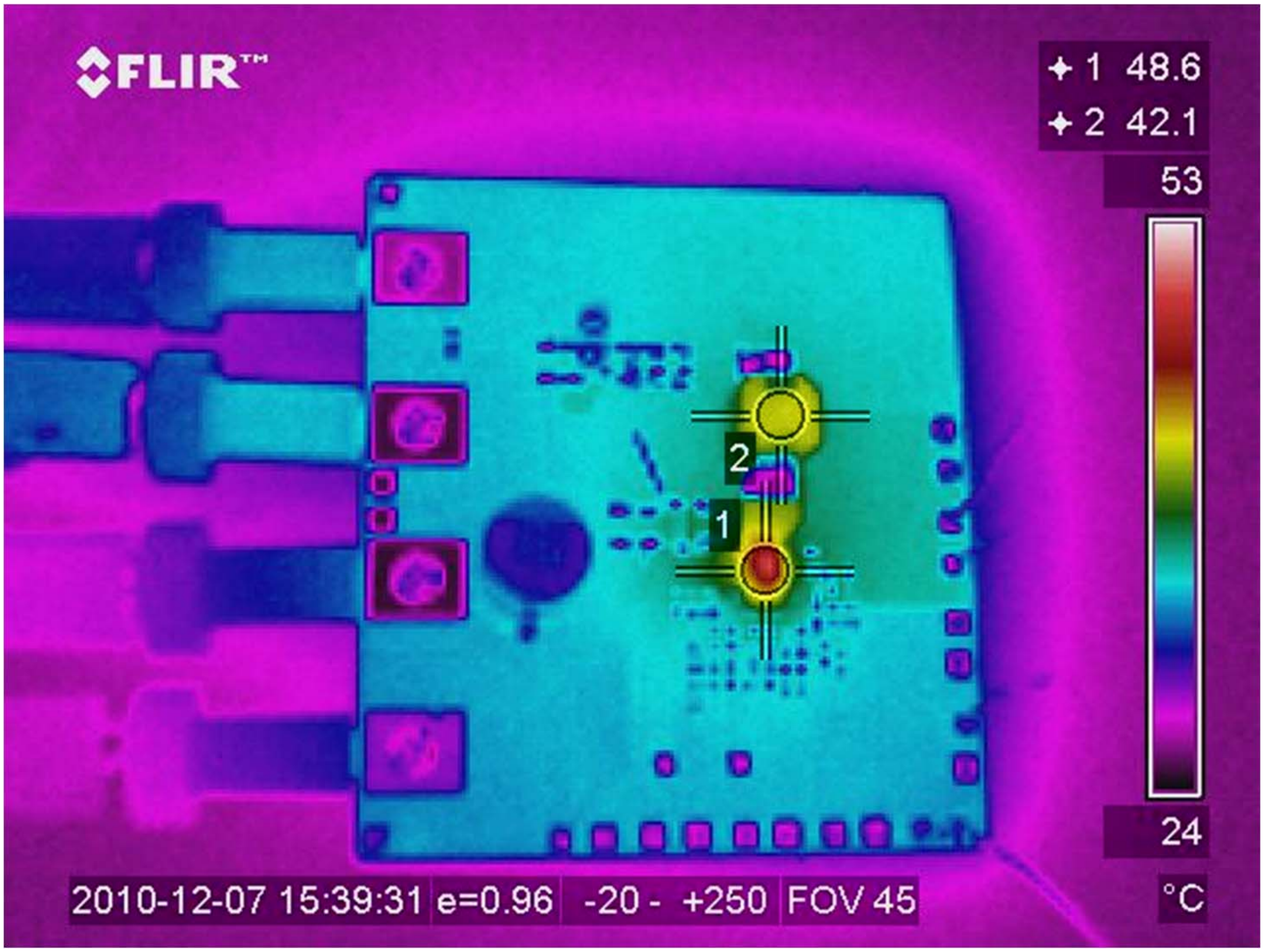


Fig. 19: Thermal Image of the board at 6A load
Test point 1 is IR3898
Test point 2 is inductor

PCB METAL AND COMPONENT PLACEMENT

Evaluations have shown that the best overall performance is achieved using the substrate/PCB layout as shown in following figures. PQFN devices should be placed to an accuracy of 0.050mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes. For further information, please refer to “SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note**.” (AN1132)**

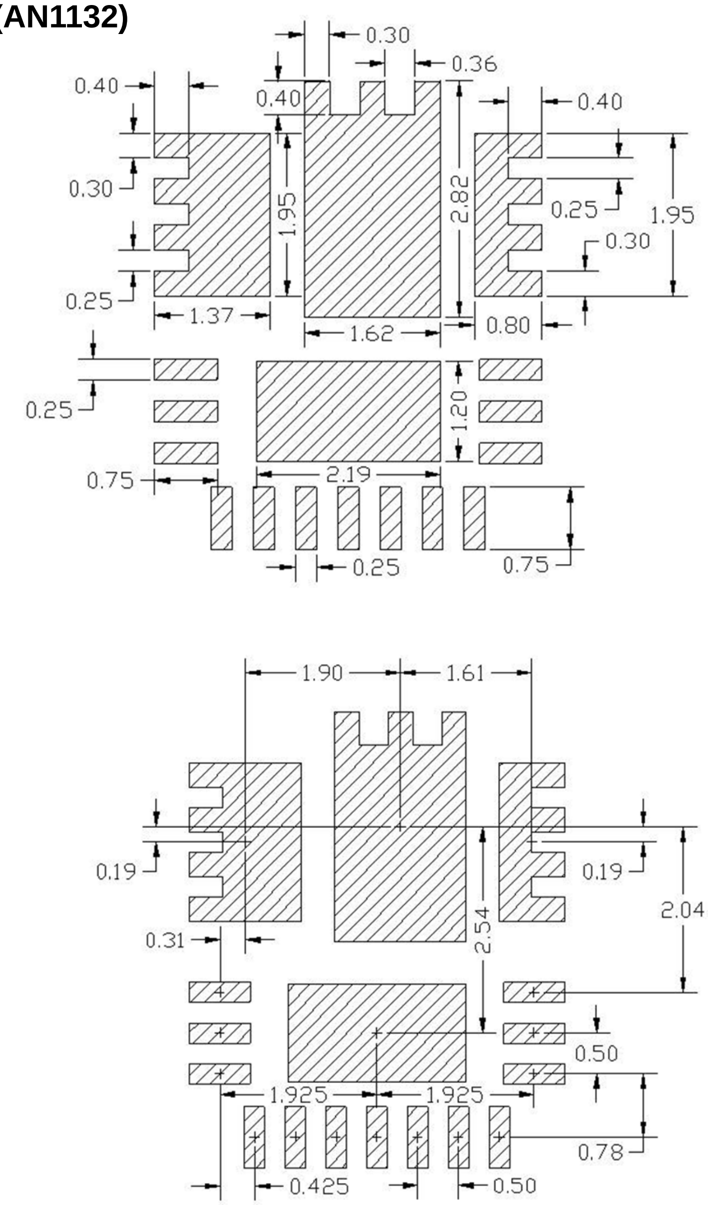


Figure 20: PCB Metal Pad Spacing (all dimensions in mm)

SOLDER RESIST

IR recommends that the larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying Copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1mm in X & Y.)
However, for the smaller Signal type leads around the edge of the device, IR recommends that these are Non Solder Mask Defined or Copper Defined. When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025mm on each edge, (i.e. 0.05mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in-between the smaller signal lead areas are at least 0.15mm wide, due to the high x/y aspect ratio of the solder mask strip.

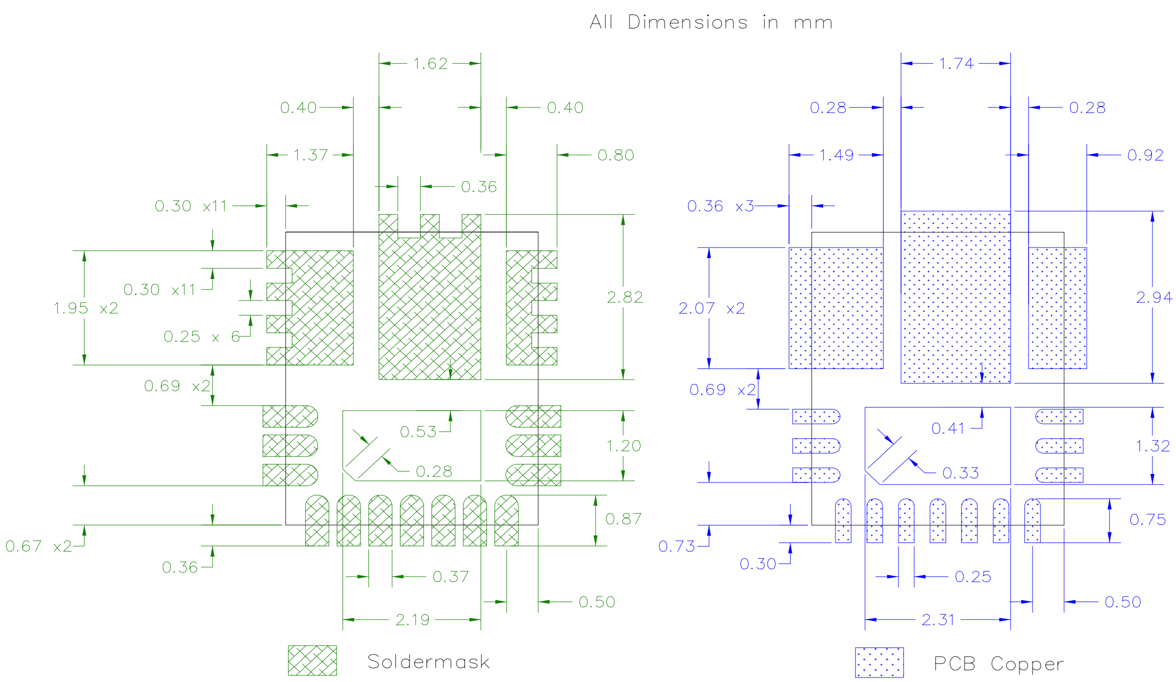


Figure 21: Solder resist

STENCIL DESIGN

Stencils for PQFN can be used with thicknesses of 0.100-0.250mm (0.004-0.010"). Stencils thinner than 0.100mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125mm-0.200mm (0.005-0.008"), with suitable reductions, give the best results. Evaluations have shown that the best overall performance is achieved using the stencil design shown in following figure. This design is for a stencil thickness of 0.127mm (0.005").The reduction should be adjusted for stencils of other thicknesses.

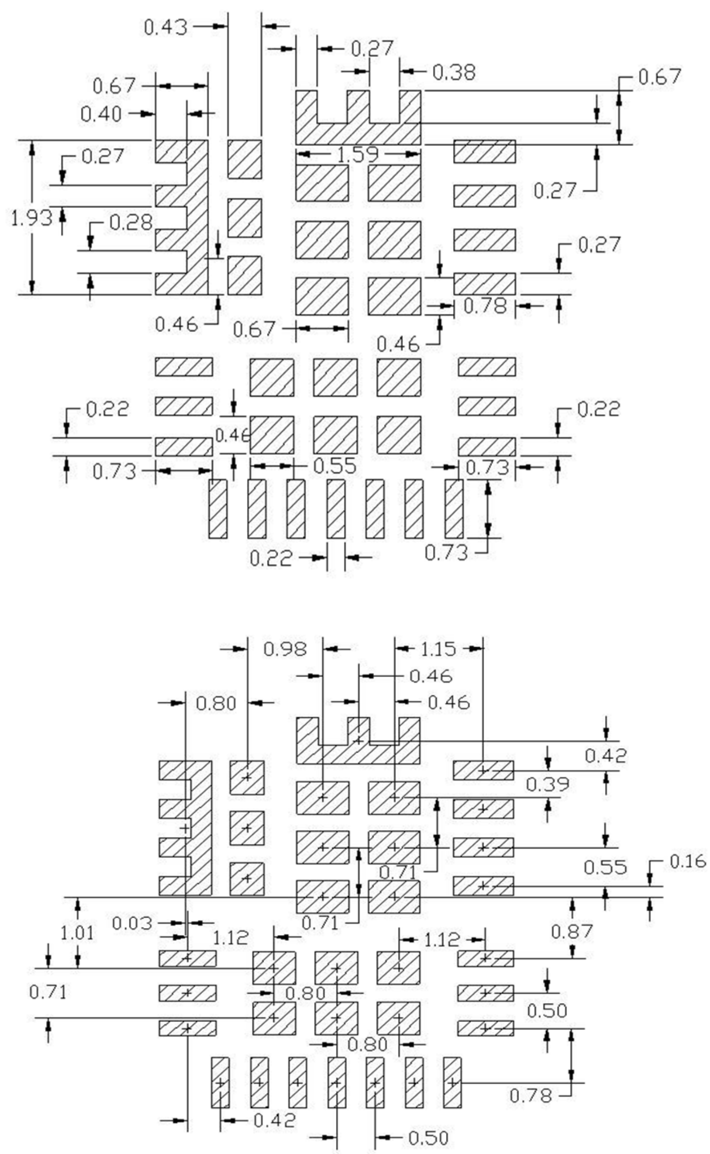
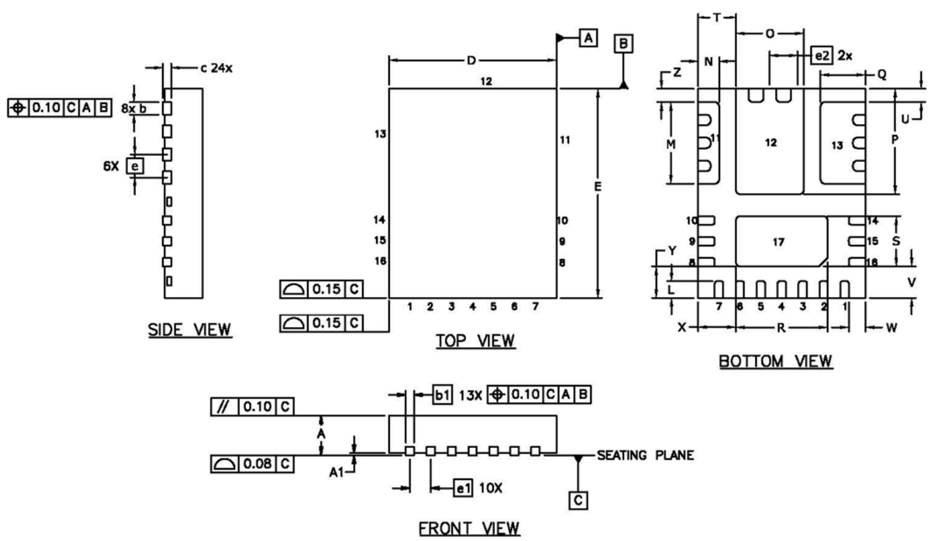


Figure 22: Stencil Pad Spacing (all dimensions in mm)

PACKAGE INFORMATION



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.800	1.000	.0315	.0394
A1	0.000	0.050	.0000	.0020
b	0.250	0.350	.0098	.0138
b1	0.150	0.250	.0059	.0098
c	0.203 REF.		.0080 REF.	
D	4.000 BASIC		.1575 BASIC	
E	5.000 BASIC		.1969 BASIC	
e	0.550 BASIC		.0217 BASIC	
e1	0.500 BASIC		.0197 BASIC	
e2	0.659 BASIC		.0259 BASIC	
L	0.350	0.450	.0138	.0177
M	1.900	2.000	.0748	.0787
N	0.453	0.553	.0178	.0218
O	1.567	1.667	.0617	.0656
P	2.470	2.570	.0972	.1012
Q	1.024	1.124	.0403	.0443
R	2.138	2.238	.0842	.0881
S	1.150	1.250	.0453	.0492
T	0.856	0.956	.0337	.0376
U	0.270	0.370	.0106	.0146
V	0.703	0.803	.0277	.0316
W	0.350	0.450	.0138	.0177
X	0.856	0.956	.0337	.0376
Y	0.703	0.803	.0277	.0316
Z	0.270	0.370	.0106	.0146

Figure 23: Package Dimensions

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