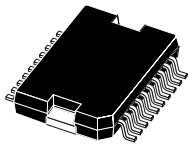
LNBEH21

LNB SUPPLY AND CONTROL IC WITH STEP-UP CONVERTER AND I²C INTERFACE

- COMPLETE INTERFACE BETWEEN LNB AND I²C™ BUS
- BUILT-IN DC/DC CONTROLLER FOR SINGLE 12V SUPPLY OPERATION AND HIGH EFFICIENCY (Typ. 94% @ 750mA)
- TWO SELECTABLE OUTPUT CURRENT LIMIT (450mA / 750mA)
- ACCURATE BUILT-IN 22KHz TONE OSCILLATOR SUITS WIDELY ACCEPTED STANDARDS
- FAST OSCILLATOR START-UP FACILITATES DiSEqC™ ENCODING
- BUILT-IN 22KHz TONE DETECTOR SUPPORTS BI-DIRECTIONAL DiSEqC™ 2.0
- 13/18V CONTROL WORD COMMUNICATION
- SEMI-LOWDROP POST REGULATOR AND HIGH EFFICIENCY STEP-UP PWM FOR LOW POWER LOSS: Typ. 0.56W @ 125mA
- TWO OUTPUT PINS SUITABLE TO BYPASS THE OUTPUT R-L FILTER AND AVOID ANY TONE DISTORSION (R-L FILTER AS PER DiSEqC 2.0 SPECs, SEE APPLICATION CIRCUIT)
- CABLE LENGTH DIGITAL COMPENSATION
- OVERLOAD AND OVER-TEMPERATURE INTERNAL PROTECTIONS I²C WITH DIAGNOSTIC BITs



PowerSO-20

- LNB SHORT CIRCUIT SOA PROTECTION WITH I²C DIAGNOSTIC BIT
- +/- 4KV ESD TOLERANT ON INPUT/ OUTPUT POWER PINS

DESCRIPTION

Intended for analog and digital satellite STB receivers/SatTV, sets/PC cards, the LNBEH21 is a monolithic voltage regulator and interface IC, assembled in POWER SO-20, specifically designed to provide the 13/18V power supply and the 22KHz tone signalling to the LNB downconverter in the antenna or to the multiswitch box. The LNBEH21 supports both methods of communication currently used, 13/18V Control Word Communication Mode and DiSEqC™ communication. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I²C™ standard interfacing.

BLOCK DIAGRAM

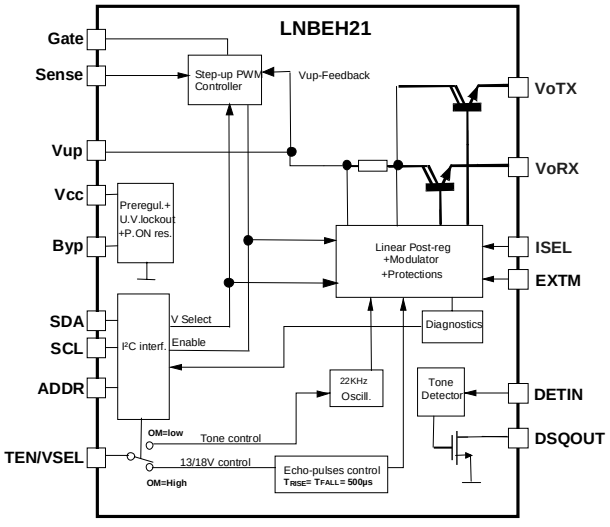


Table 1: Ordering Codes

TYPE	PowerSO-20 (Tube)	PowerSO-20 (Tape & Reel)
LNBEH21	LNBEH21PD	LNBEH21PD-TR

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Input Voltage	-0.3 to 16	V
V_{UP}	DC Input Voltage	-03 to 25	V
I_O	Output Current	Internally Limited	mA
V_OTX/RX	DC Output Pins Voltage	-0.3 to 25	V
V_I	Logic Input Voltage (SDA, SCL, DSQIN, ISEL)	-0.3 to 7	V
V_{DETIN}	Detector Input Signal Amplitude	-0.3 to 2	V_{PP}
V_{OH}	Logic High Output Voltage (DSQOUT)	-0.3 to 7	V
I_{GATE}	Gate Current	± 400	mA
V_{SENSE}	Current Sense Voltage	-0.3 to 1	V
$V_{ADDRESS}$	Address Pin Voltage	-0.3 to 7	V
T_{stg}	Storage Temperature Range	-40 to +150	°C
T_{op}	Operating Junction Temperature Range	-40 to +125	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 3: Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	2	°C/W

Figure 1: Pin Configuration (top view)

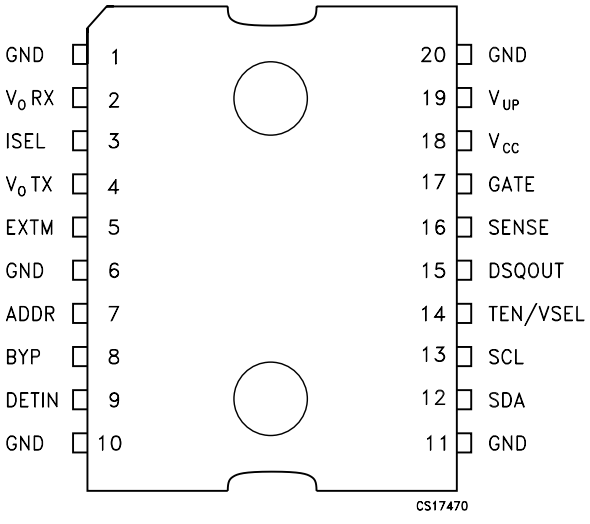


Table 4: Pin Description

PIN N°	SYMBOL	NAME	FUNCTION
18	V_{CC}	Supply Input	8V to 15V IC supply. A 220µF bypass capacitor to GND with a 470nF (ceramic) in parallel is recommended
17	GATE	External Switch Gate	External MOS switch Gate connection of the step-up converter
16	SENSE	Current Sense Input	DC/DC Current Sense comparator input. Connected to current sensing resistor
19	V_{UP}	Step-up Voltage	Input of the linear post-regulator. The voltage on this pin is monitored by internal step-ut controller to keep a minimum dropout across the linear pass transistor.
2	V_ORX	Output Port during 22KHz Tone RX	RX Output to the LNB in DiSEqC 2.0 application. See truth tables for voltage selections and Communication Mode section for details.
12	SDA	Serial Data	Bidirectional data from/to I^2C bus.
13	SCL	Serial Clock	Clock from I^2C bus.
14	TEN/VSEL	DiSEqC or 13/18V TTL Logic Input	Depending on the value set for OM bit this pin enable/disable the internal 22KHz tone generator (OM=0) or switch the output voltage from 13V to 18V and vice versa (OM=1)
9	DETIN	Tone Detector Input	22kHz Tone Detector Input. Must be AC coupled to the DiSEqC 2.0 bus.
15	DSQOUT	DiSEqC Output	Open drain output of the tone Detector to the main µcontroller for DiSEqC 2.0 data decoding. It is set LOW when a 22 KHz tone is detected.
5	EXTM	External Modulator	External Modulation Input acts on V_OTX. Needs DC decoupling to the AC source. If not used, can be left open.
1, 6, 10, 11, 20	GND	GROUND	Pins connected to Ground. Also internally connected to the die frame (exposed pad) for heat dissipation.
8	BYP	Bypass Capacitor	Needed for internal preregulator filtering
3	ISEL	Current Limit Select	Set high or floating for $I_O \leq 750mA$, connect to ground for $I_O \leq 450mA$.
4	V_OTX	Output Port during 22KHz Tone TX	Output of the linear post-regulator/modulator to the LNB. See truth tables for voltage selections.
7	ADDR	Address Setting	Four I^2C bus addresses available by setting the Address Pin level voltage. See address pin characteristics table.

TYPICAL APPLICATION CIRCUITS

Figure 2: Application Circuit for DiSEqC 1.x and Output Current < 450 mA

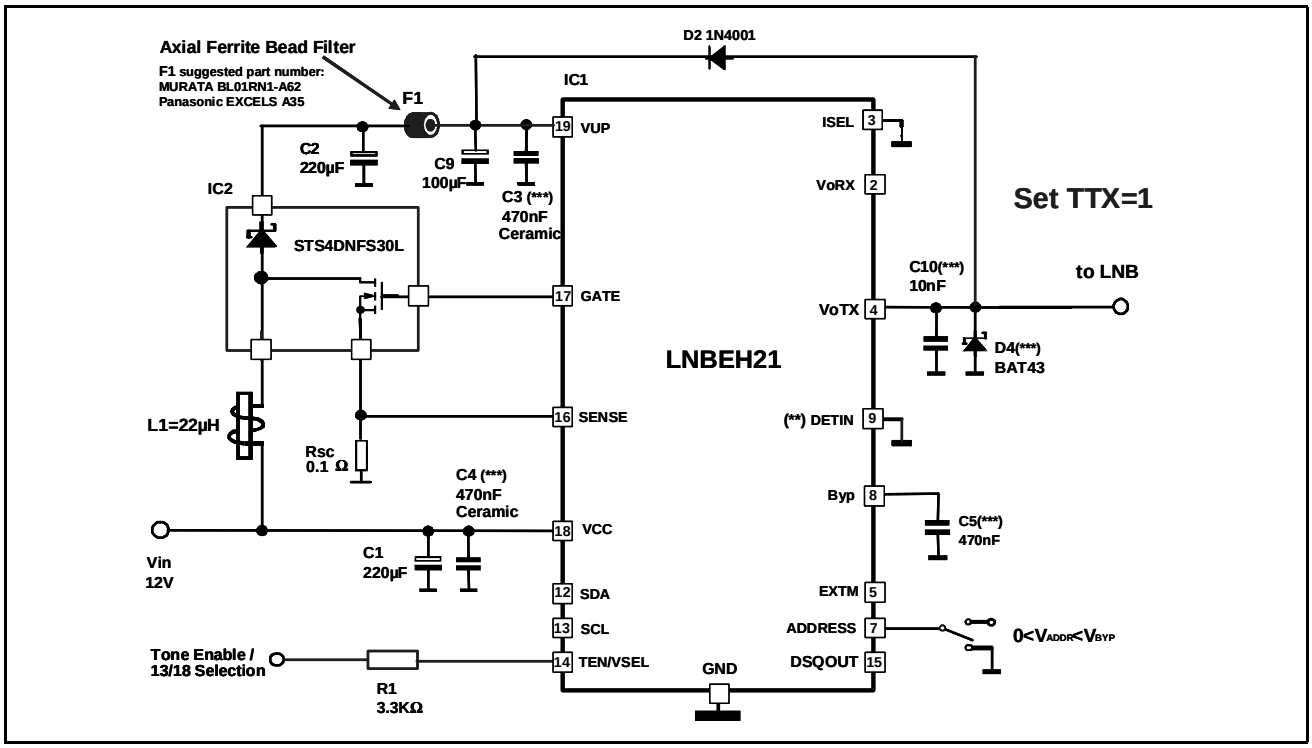
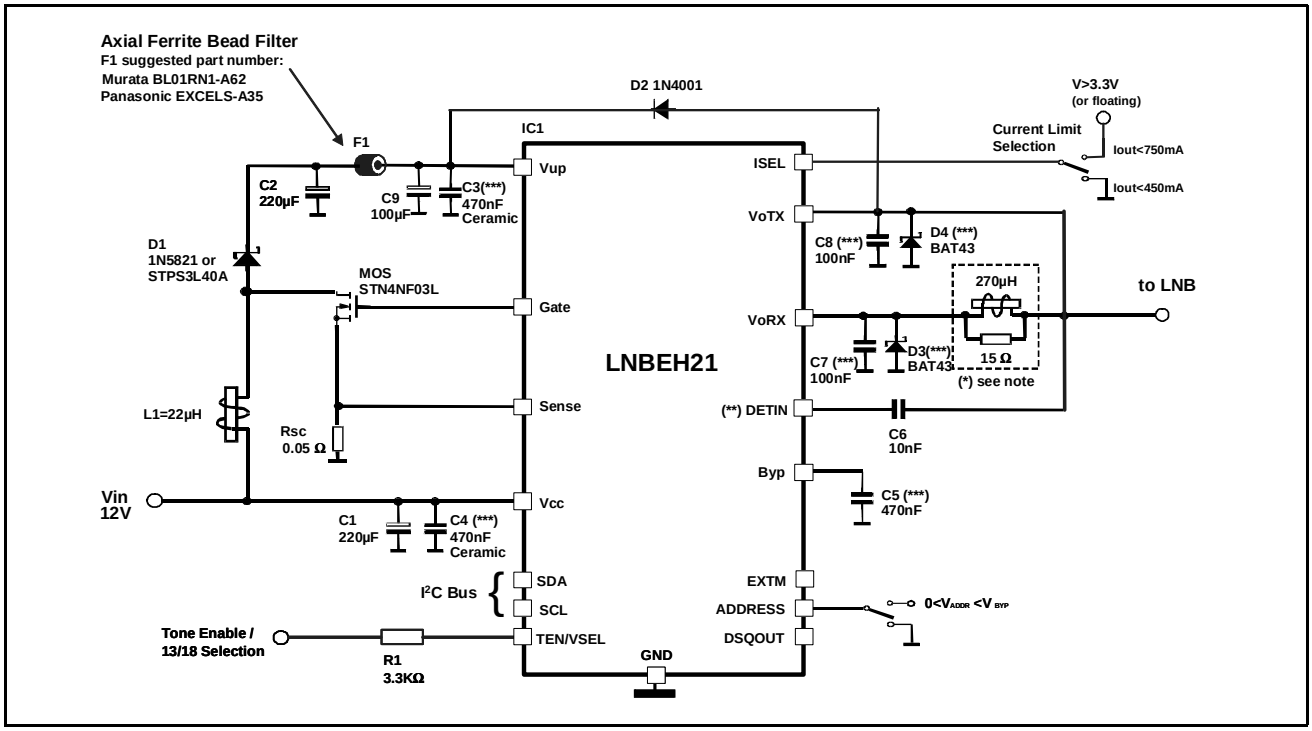


Figure 3: Full Application Circuit for Bi-directional DiSEqC 2.0 and Output Current up to 750mA



(*) R-L Filter to be used according to EUTELSAT recommendation to implement the DiSEqC™ 2.0, (see DiSEqC™ implementation section). If bidirectional DiSEqC™ 2.0 is not implemented the R-L filter can be removed and the above DiSEqC 1.x circuit can be used.

(**) Do not leave these pins floating if not used.

(***) To be soldered as close as possible to relative pins.
-C8 and D3,4 are needed only to protect the output pins from any negative voltage spikes during high speed voltage transitions.

APPLICATION INFORMATION

This IC has a built in DC/DC Step-Up controller that, from a single supply source ranging from 8 to 15V, generates the input voltages (V_{UP}) that let the linear post-regulator to work at a minimum dissipated power of 1.65W typ. @ 750mA load (the linear regulator drop voltage is internally kept at: V_{UP}-V_{OUT}=2.2V typ.). An UnderVoltage Lockout circuit will disable the whole circuit when the supplied V_{CC} drops below a fixed threshold (6.7V typically).

All the functions of this IC are controlled via I^2C^{TM} bus by writing 6 bits on the System Register (SR, 8 bits). The same register can be read back, and two bits will report the diagnostic status. When the IC is put in Stand-by (EN bit LOW), the power blocks are disabled.

The LNBEH21 is compliant both with the DiSEqC™ 2.0 specification and with the 13/18V Control Word Communication Mode. The communication mode is selected by the "OM" I^2C^{TM} bit and, depending on the OM bit status, the TEN/VSEL pin function (see block diagram) is switched to control the 13/18V output voltage level or to enable the internal 22KHz tone generator when in DiSEqC mode. (refer to Communication Mode section for details).

When the regulator blocks are active (EN bit = 1) and in DiSEqC mode (OM=0), the LNB output voltage can also be logic controlled to select 13V or 19.5V by mean of the V_{OM} bit. The control of the V_{OM} bit on the V_{UP} voltage level depends on the OM bit status in order to allow the 13/18V Control Word Communication (see Communication Mode section). Additionally, it is possible to increment by 1V (Typ.) the selected output voltage value to compensate the excess voltage drop along the coaxial cable using the LLC SR bit (LLC=1).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. Also in this case, the V_OTX output must be set ON during the tone transmission by setting the TTX bit High. When the external modulation is not used, the relevant pin can be left open.

The current limitation block is SOA type and it is possible to select two current limit thresholds, by the dedicated ISEL pin. The higher threshold is in the range of 750mA to 1A if the ISEL is left floating or connected a voltage >3.3V. The lower threshold is in the range of 450mA to 700mA when the ISEL pin is connected to ground. When the output port is shorted to ground, the SOA current limitation block limits the short circuit current (I_{SC}) at typically 300mA, to reduce the power dissipation. Moreover, it is possible to set the Short Circuit Current protection either statically (simple current clamp) or dynamically by the PCL bit of the I^2C SR; when the PCL (Pulsed Current Limiting) bit is set to LOW, the overcurrent protection circuit works dynamically, as soon as an overload is detected, the output is shut-down for a time T_{OFF}, typically 900ms. Simultaneously the OLF bit of the System Register is set to HIGH. After this time has elapsed, the output is resumed for a time T_{ON}=1/10T_{OFF} (typ.). At the end of Ton, if the overload is still detected, the protection circuit will cycle again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical T_{ON}+T_{OFF} time is 990ms and it is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up in most conditions.

However, there could be some cases in which an highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=HIGH) and then switching to the dynamic mode (PCL=LOW) after a chosen amount of time. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared.

This IC is also protected against overheating: when the junction temperature exceeds 150°C (typ.), the step-up converter and the linear regulator are shut off, and the OTF SR bit is set to HIGH. Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 135°C (typ.).

(*): External components are needed to comply to bi-directional DiSEqC™ bus hardware requirements. Full compliance of the whole application with DiSEqC™ specifications is not implied by the use of this IC.

I^2C BUS INTERFACE

Data transmission from main µP to the LNBEH21 and vice versa takes place through the 2 wires I^2C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

DATA VALIDITY

As shown in fig. 4, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

START AND STOP CONDITIONS

As shown in fig. 5 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

BYTE FORMAT

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

ACKNOWLEDGE

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 6). The peripheral (LNBEH21) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBEH21 won't generate the acknowledge if the V_{CC} supply is below the Undervoltage Lockout threshold (6.7V typ.)

TRANSMISSION WITHOUT ACKNOWLEDGE

Avoiding to detect the acknowledge of the LNBEH21, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.
This approach of course is less protected from misworking and decreases the noise immunity.

Figure 4: Data Validity On The I^2C Bus

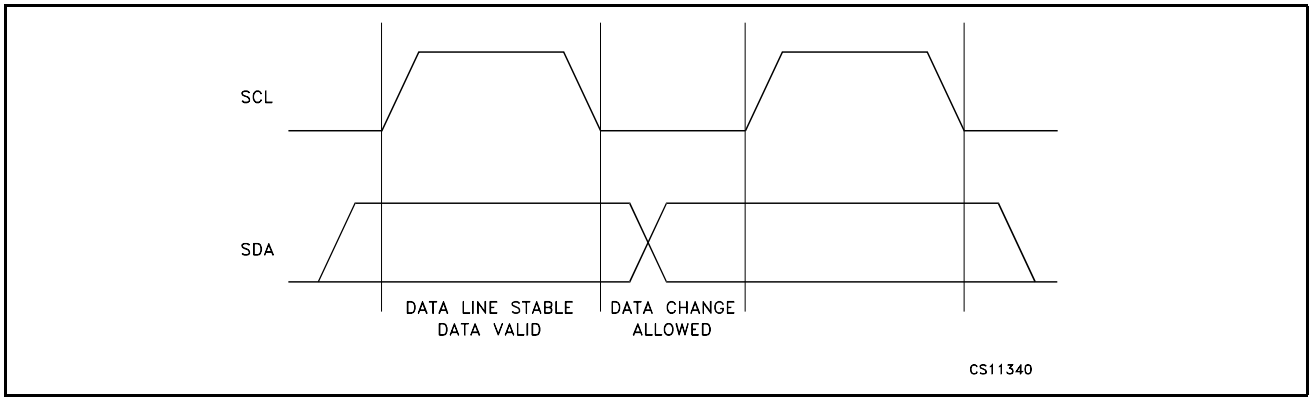


Figure 5: Timing Diagram On I^2C Bus

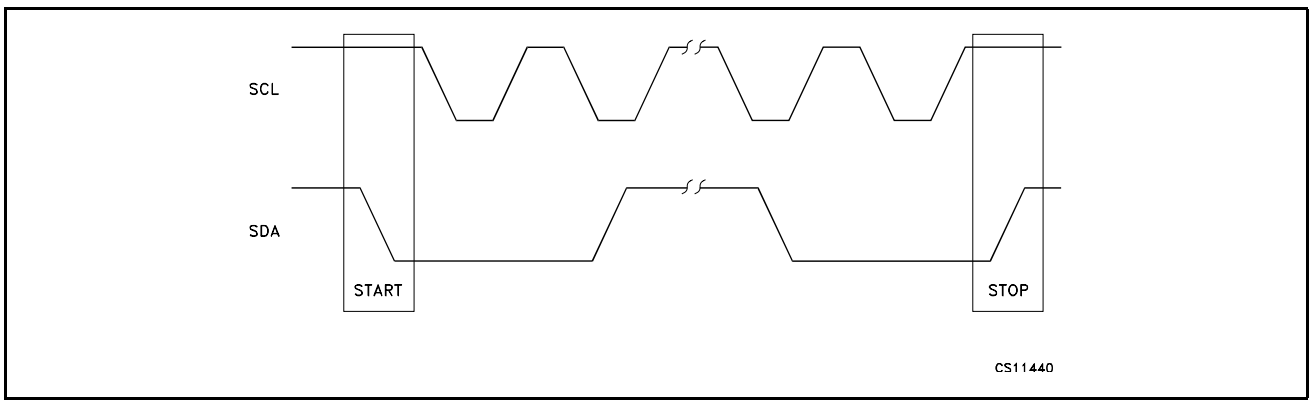
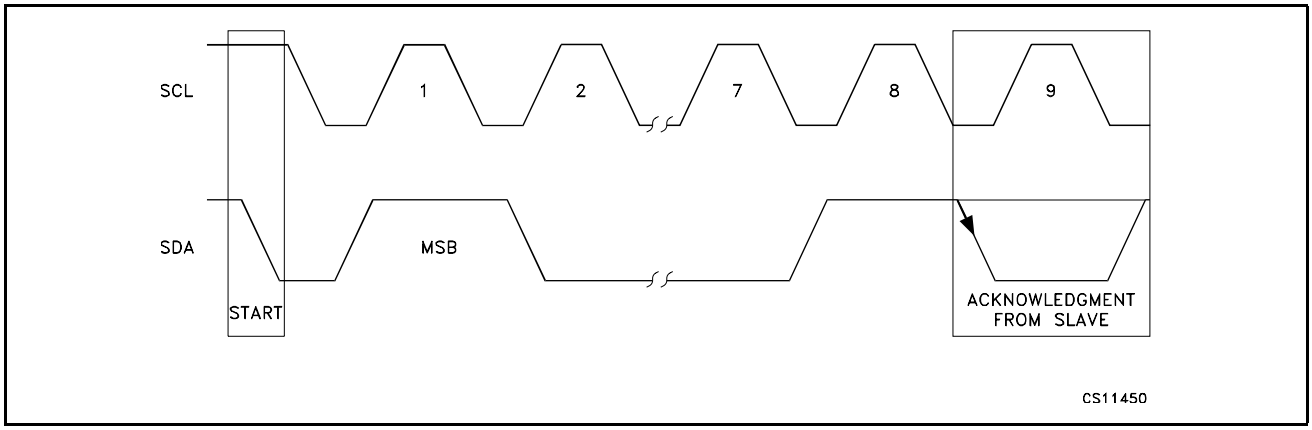


Figure 6: Acknowledge On I^2C Bus



LNBEH21 SOFTWARE DESCRIPTION

INTERFACE PROTOCOL

The interface protocol comprises:
- A start condition (S)
- A chip address byte = hex 10 / 11 (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

	CHIP ADDRESS									DATA									
	MSB							LSB		MSB							LSB		
S	0	0	0	1	0	0	0	R/W	ACK									ACK	P

ACK= Acknowledge; S = Start; P = Stop; R/W = Read/Write

SYSTEM REGISTER (SR, 1 BYTE)

MSB							LSB
R, W	R, W	R, W	R, W	R, W	R, W	R	R
PCL	TTX	OM	LLC	VOM	EN	OTF	OLF

R,W = read and write bit; R = Read-only bit
All bits reset to 0 at Power-On

TRANSMITTED DATA (I^2C BUS WRITE MODE)

When the R/W bit in the chip address is set to 0, the main µP can write on the System Register (SR) of the LNBEH21 via I^2C bus. Only 6 bits out of the 8 available can be written by the µP, since the remaining 2 are left to the diagnostic flags, and are read-only.

RECEIVED DATA (I^2C bus READ MODE)

The LNBEH21 can provide to the Master a copy of the SYSTEM REGISTER information via I^2C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following master generated clocks bits, the LNBEH21 issues a byte on the SDA data bus line (MSB transmitted first).
At the ninth clock bit the MCU master can:
- acknowledge the reception, starting in this way the transmission of another byte from the LNBEH21;
- no acknowledge, stopping the read mode communication.

While the whole register is read back by the µP, only the two read-only bits OLF and OTF convey diagnostic informations about the LNBEH21

PCL	TTX	OM	LLC	VOM	EN	OTF	OLF	Function
These bits are read exactly the same as they were left after last write operation						0		T_J<135°C, normal operation
						1		T_J>150°C, power block disabled
							0	$I_{OUT}<I_{OMAX}$, normal operation
							1	$I_{OUT}>I_{OMAX}$, overload protection triggered

Values are typical unless otherwise specified

POWER-ON I^2C INTERFACE RESET

The I^2C interface built in the LNBEH21 is automatically reset at power-on. As long as the V_{CC} stays below the UnderVoltage Lockout threshold (6.7V typ.), the interface will not respond to any I^2C command and the System Register (SR) is initialized to all zeroes, thus keeping the power blocks disabled. Once the V_{CC} rises above 7.3V typ, the I^2C interface becomes operative and the SR can be configured by the main µP. This is due to 500mV of hysteresis provided in the UVL threshold to avoid false retriggering of the Power-On reset circuit.

ADDRESS PIN

Connecting this pin to GND the Chip I^2C interface address is 0001000, but, it is possible to choice among 4 different addresses simply setting this pin at 4 fixed voltage levels (see table on page 11).

COMMUNICATION MODE SELECTION

I^2C OM bit (Operating Mode selection bit)

The LNBEH21 can work either in DiSEqC™ mode or in 13/18V Control Word mode; the selection of the communication mode is achieved through the dedicated I^2C OM bit that must be respectively set to LOW or to HIGH. Depending on the communication mode selection (OM bit state) the I^2C VOM bit and the TEN/VSEL pin (#14) operation are switched between two different functions:

VOM bit and TEN/VSEL pin functions with OM=0 (DiSEqC™ mode).

- The TEN/VSEL pin controls the 22KHz bursting code, by enabling the internal 22KHz tone generator, to allow immediate DiSEqC™ data encoding.
- In DiSEqC™ mode, the VOM I^2C bit controls simultaneously the post-regulator output voltage (V_{OUT}) and the DC/DC converter output voltage (V_{UP}). The VOM bit function is to select the LNB output voltage to 13.25V or 19.5V respectively if VOM=0 or VOM=1 (14.25V or 20.5V if LLC=1) and V_{UP} is set to V_{OUT}+2.2V typ., according to DiSEqC section in the Truth Table on page 11;

VOM bit and TEN/VSEL pin functions with OM=1 (13/18V Control Word mode).

- When OM=1, the TEN/VSEL controls the 13/18V output voltage level. The usage of the TEN/VSEL pin in combination with the VOM bit allows the 13/18V Control Word Communication (see block diagram on page 1). The TEN/VSEL is a TTL control logic pin.
- in 13/18V Control Word Communication mode, the VOM bit does not control the LNB output voltage but only forces the DC/DC Converter output voltage (V_{UP}) in a steady state (V_{UP}=21.7V typ. if LLC=0 and V_{UP}=22.7V typ. if LLC=1). When OM=VOM=1, the LNB output voltage is controlled only by the TEN/VSEL pin.

COMMUNICATION MODE IMPLEMENTATION

DiSEqC™ 2.0 and 1.x mode, OM=0

When OM=0, the LNBEH21 is suitable both for DiSEqC 2.0 and for unidirectional DiSEqC 1.x applications.

The bi-directional DiSEqC 2.0 protocol implementation is allowed by an easy PWK modulation/ demodulation of the 22KHz carrier. The PWK data are exchanged between the LNBEH21 and the main µP, using logic levels that are compatible with both 3.3 and 5V microcontrollers. This data exchange is made through two dedicated pins, TEN/VSEL (when OM=0) and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the µP, thus leaving to the resident firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC protocol. The fully bi-directional DiSEqC™ 2.0 interfacing is completed by the built-in 22KHz tone detector. Its input pin (DETIN) must be AC coupled to the DiSEqC TM bus and the extracted PWK data are available on the DSQOUT pin biased with a pull-up resistor to a fixed voltage (see Fig. 7 and 8).

Full compliance of the system to the specification is not implied by the bare use of the LNBEH21; the system designer should also take in consideration that, to comply to the bi-directional DiSEqC TM 2.0 bus hardware requirements, an output R-L filter is needed. In order to help the system designer to avoid any distortion during the 22KHz tone transmission, due to the output R-L impedance, the LNBEH21 is provided with two output pins: the V_OTX, to be used during the 22KHz tone transmission; and the V_ORX, to be used when the tone is received (see DiSEqC 2.0 typical application circuit). This allows the 22KHz tone to pass without any losses due to the R-L filter.

During the 22KHz transmission, activated by TEN/VSEL pin, the V_OTX pin must be preventively activated by the TTX I^2C bit, so that, both the power supply and the 22KHz tone, are provided by mean of V_OTX output. As soon as the tone transmission is expired, the V_OTX must can set to OFF by setting the TTX I^2C bit to zero, and the power supply is provided to the LNB by the V_ORX pin through the R-L filter.

Unidirectional DiSEqC 1.x and non-DiSEqC systems normally don't need the output R-L termination, and the V_OTX pin can be directly connected to the LNB supply port of the Tuner (see DiSeqC 1.x typical application circuit). There is also no need of Tone Decoding, thus DETIN and DSQOUT pins can be left connected to ground; both the 22KHz tone and the power supply, are provided by the V_OTX by setting always TTX=1.

When In DiSEqC mode, the Output Voltage level (13.1V,14.1V,19.5V,20.5V) is selected only by the VOM and LLC I^2C bits combinations (refer to DiSEqC section in the Complete Truth Table on page 10 for detailed logic combination and corresponding function description).

Figure 7: DETIN/DSQOUT Circuit

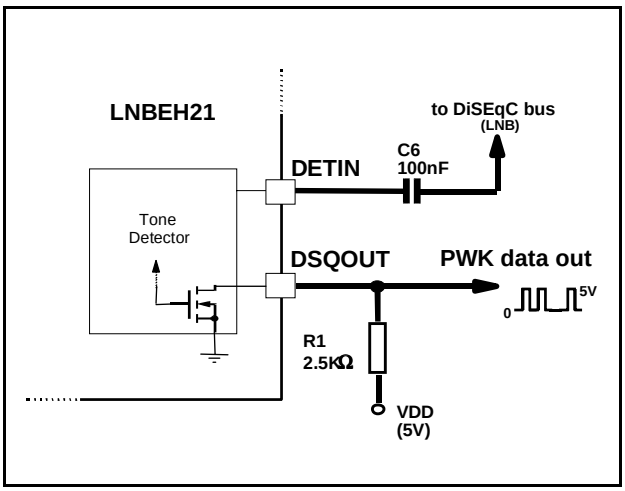
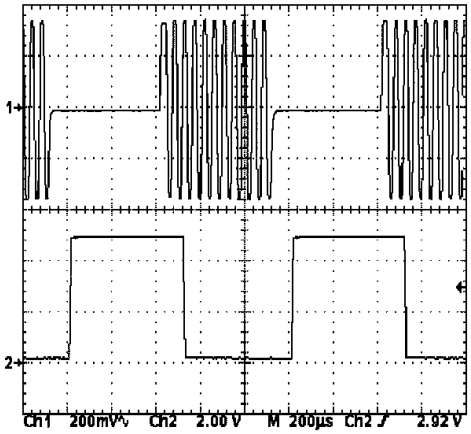


Figure 8: DETIN/DSQOUT Waveform



CH1=22KHz Tone to DETIN, CH2=PWK data at DSQOUT

13/18V Control Word mode, OM=1

When OM=1 the VOM is used to force the DC/DC Converter output voltage (V_{UP}) in a steady state and to control the TEN/VSEL pin function. According to the VOM selection TEN/VSEL will absolve two different functions:

1)VOM=0 - TEN/VSEL pin controls both the post regulator output voltage (V_{OUT}) and the DC/DC Converter output voltage (V_{UP}).

2)VOM=1 - TEN/VSEL pin controls only the post regulator output voltage while the DC/DC Converter output voltage is forced in a steady state, at the high level, 22.7V typ. with LLC=1 and 21.7V typ. if LLC=0. During normal operation, when no 13/18V control word is transmitted, the device must work with VOM=0 and TEN/VSEL pin is used to select the odd or even numbered transponder setting up the post regulator output voltage in a steady state (13.25 or 19.5V); the V_{UP} voltage is selected by the IC according to the V_{OUT} value in order to minimize the power dissipation.

Before the beginning of the 13/18V Control Word Communication, it is mandatory to set VOM at HIGH level forcing the V_{UP} at 21.7V typ.; after a certain setup time the µP can start to send the 13/18V pulses command to the TEN/VSEL pin. During the 13/18V pulses, the V_{OUT} rise and fall time between 13.25V and 19.5V of are fully controlled by the internal voltage reference and they are maintained on a typical value of 575µs, this time is guaranteed with a maximum output capacitance of 330nF and a load current in the range of 6 to 450mA. As soon as the communication has expired VOM bit must be set LOW to avoid any additional power dissipation (See Thermal Design Note). Refer to 13/18V Control Word section in the complete truth table on page 11 for detailed logic combination and corresponding function description.

DiSEqC COMMUNICATION TRUTH TABLE (TEN/VSEL pin controls the internal 22KHz Tone)

PCL	TTX	OM	LLC	VOM	EN	OTF	OLF	Function
		0	0	0	1	X	X	V_O = 13.25 V and V_{UP} = 15.45 V TEN/VSEL = HIGH 22KHz Enabled TEN/VSEL = LOW 22KHz Disabled
		0	0	1	1	X	X	V_O = 19.5V and V_{UP}= 21.7 V TEN/VSEL = HIGH 22KHz Enabled TEN/VSEL = LOW 22KHz Disabled
		0	1	0	1	X	X	V_O = 14.25 V and V_{UP} = 16.45 V TEN/VSEL = HIGH 22KHz Enabled TEN/VSEL = LOW 22KHz Disabled
		0	1	1	1	X	X	V_O = 20.5 V and V_{UP} = 22.7 V TEN/VSEL = HIGH 22KHz Enabled TEN/VSEL = LOW 22KHz Disabled

13/18V CONTROL WORD COMMUNICATION TRUTH TABLE (TEN/VSEL pin function depends on VOM bit state)

PCL	TTX	OM	LLC	VOM	EN	OTF	OLF	Function
		1	0	0	1	X	X	TEN/VSEL pin controls both the LNB output voltage and the DC/DC Converter Voltage (V_{UP}) TEN/VSEL = LOW, V_O = 13.25 V and V_{UP} = 15.45 V TEN/VSEL = HIGH, V_O = 19.5V and V_{UP}= 21.7 V
		1	0	1	1	X	X	TEN/VSEL pin controls only the LNB output voltage and the DC/DC Converter output is forced always at 21.7 V TEN/VSEL = LOW, V_O = 13.25 V and V_{UP} = 21.7 V TEN/VSEL = HIGH, V_O = 19.5V and V_{UP}= 21.7 V
		1	1	0	1	X	X	TEN/VSEL pin controls both the LNB output voltage and the DC/DC Converter Voltage (V_{UP}) TEN/VSEL = LOW, V_O = 14.25 V and V_{UP} = 16.45 V TEN/VSEL = HIGH, V_O = 20.5V and V_{UP}= 22.7 V
		1	1	1	1	X	X	TEN/VSEL pin used to set only the LNB output voltage. DC/DC Converter output voltage forced always at 22.7 V TEN/VSEL = LOW, V_O = 14.25 V and V_{UP} = 22.7 V TEN/VSEL = HIGH, V_O = 20.5V and V_{UP}= 22.7 V

GENERAL FEATURES TRUTH TABLE

PCL	TTX	OM	LLC	VOM	EN	OTF	OLF	Function
	0	X			1	X	X	When TTX = 0 the device is set in receiving mode, the TX output is partially OFF the V_ORX pin is ON: V_OTX = OFF, V_ORX = ON
	1	X			1	X	X	When TTX = 1 the device is set in receiving mode, the RX output is partially OFF the V_OTX pin is ON: V_OTX = ON, V_ORX = OFF
0					1	X	X	Pulsed (dynamic) current limiting is selected
1					1	X	X	Static current limiting is selected
X	X	X	X	X	0	X	X	Power blocks disabled

X = don't care; values are typical unless otherwise specified.

Table 5: Electrical Characteristics T_J = 0 to 85°C, EN=1, LLC=PCL=OM=VOM=0, 22KHz Tone Disabled, TTX=0/1, ISEL=High, V_I=12V, I_O=50mA, unless otherwise specified. See software description section for I^2C access to the system register**.**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_I	Supply Voltage	V_O = 20.5V, I_O = 750 mA Tone enabled		8		15	V
I_I	Supply Current	V_O = 20.5V, Tone Enabled, NO LOAD	EN=1		20	40	mA
			EN=0		3.5	7	
V_O	Output Voltage	OM=0, VOM=1 (or OM=1, VOM=0), I_O=750mA, TEN/VSEL=High	LLC=0	18.7	19.5	20.3	V
			LLC=1		20.5		
V_O	Output Voltage	OM=0, VOM=1 (or OM=1, VOM=0), I_O=750 mA, TEN/VSEL=Low	LLC=0	12.75	13.25	13.75	V
			LLC=1		14.25		
ΔV_O	Line Regulation	V_I= 8 to 15V, OM=0, VOM=0			5	40	mV
		V_I= 8 to 15V, OM=0, VOM=1			5	60	
ΔV_O	Load Regulation	OM=0, VOM=0/1, I_O = 50 to 750mA				200	mV
13/18V t_r- t_f	13/18V Rise and Fall transition Time (to be measured at the 90% and 10% voltage range)	OM=VOM=1, TEN/VSEL from low to high, I_O = 6 to 450 mA, C_O = 10 to 330 nF			575		µs
I_{MAX}	Output Current Limiting	ISEL ≥ 3.3V or Floating		750		1000	mA
		ISEL = GND		450		700	
I_{SC}	Output Short Circuit Current				300		mA
t_{OFF}	Dynamic Overload protection OFF Time	PCL=0 Output Shorted			900		ms
t_{ON}	Dynamic Overload protection ON Time	PCL=0 Output Shorted			t_{OFF}/10		ms
f_{TONE}	Tone Frequency	OM=0, TEN/VSEL=High		20	22	24	KHz
A_{TONE}	Tone Amplitude	OM=0, TEN/VSEL=High		0.55	0.72	0.9	V_{PP}
D_{TONE}	Tone Duty Cycle	OM=0, TEN/VSEL=High		40	50	60	%
t_r, t_f	Tone Rise and Fall Time	OM=0, TEN/VSEL=High		5	8	15	µs
G_{EXTM}	External Modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 50KHz			6		
V_{EXTM}	External Input Voltage	AC Coupling				400	mV_{PP}
Z_{EXTM}	External Modulation Impedance	f = 10Hz to 50KHz			260		Ω
f_{SW}	DC/DC Converter Switching Frequency				220		kHz
f_{DETIN}	Tone Detector Frequency Capture Range	0.4Vpp sinewave		18		24	kHz
V_{DETIN}	Tone Detector Input Amplitude	f_{IN}=22kHz sinewave		0.2		1.5	V_{PP}
Z_{DETIN}	Tone Detector Input Impedance				150		kΩ
V_{OL}	DSQOUT Pin Logic LOW	Tone present I_{OL}=2mA			0.3	0.5	V
I_{OZ}	DSQOUT Pin Leakage Current	Tone absent V_{OH} = 6V				10	µA
V_{IL}	TEN/VSEL Input Pin Logic LOW					0.8	V
V_{IH}	TEN/VSEL Input Pin Logic HIGH			2			V
I_{IH}	TEN/VSEL Pin Input Current	V_{IH} = 5V			15		µA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OBK}	Output Backward Current	EN=0 V_{OBK} = 18V		-6	-15	mA
T_{SHDN}	Temperature Shutdown Threshold			150		°C
ΔT_{SHDN}	Temperature Shutdown Hysteresis			15		°C

Table 6: Gate And Sense Electrical Characteristics (T_J = 0 to 85°C, V_I = 12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{DSON-L}	Gate LOW R_{DSON}	I_{GATE}= -100mA		4.5		Ω
R_{DSON-H}	Gate HIGH R_{DSON}	I_{GATE}= 100mA		4.5		Ω
V_{SENSE}	Current Limit Sense Voltage			200		mV

Table 7: I^2C Electrical Characteristics (T_J = 0 to 85°C, V_I = 12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	LOW Level Input Voltage	SDA, SCL			0.8	V
V_{IH}	HIGH Level Input Voltage	SDA, SCL	2			V
I_I	Input Current	SDA, SCL, V_I = 0.4 to 4.5V	-10		10	µA
V_{OL}	Low Level Output Voltage	SDA (open drain), I_{OL} = 6mA			0.6	V
f_{MAX}	Maximum Clock Frequency	SCL	500			KHz

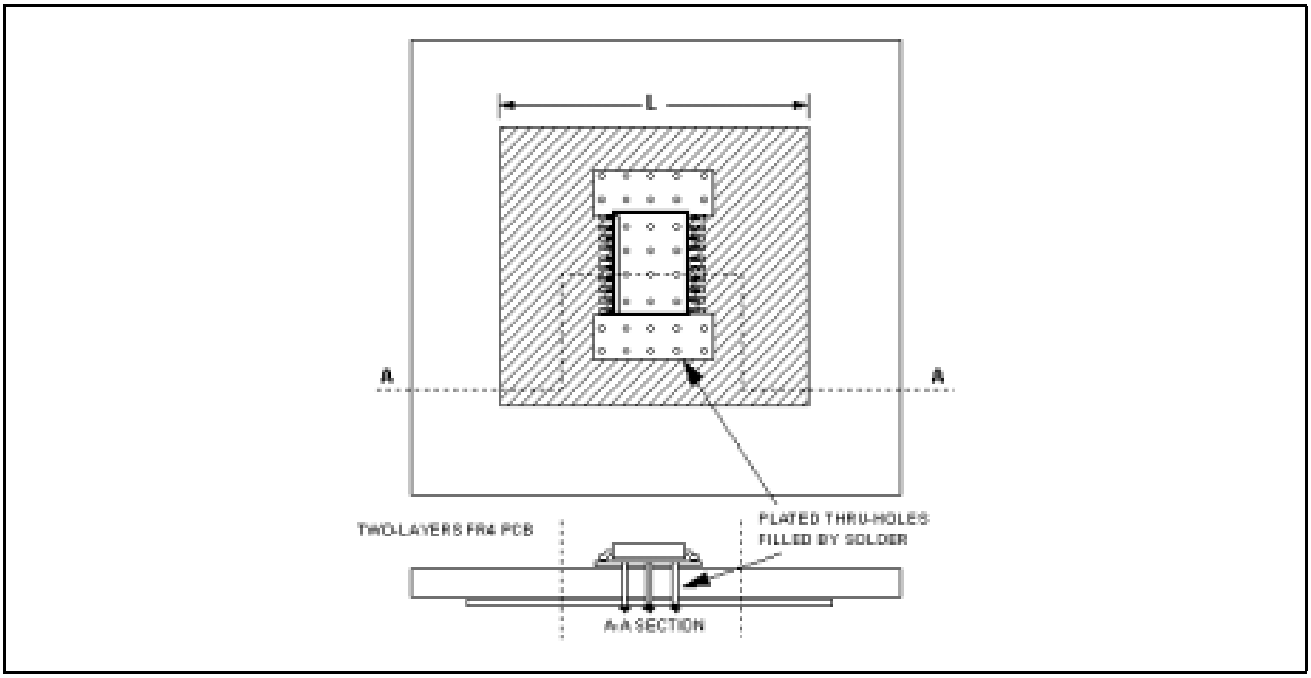
Table 8: Address Pin Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ADDR-1}	"0001000" Addr Pin Voltage		0		0.7	V
V_{ADDR-2}	"0001001" Addr Pin Voltage		1.3		1.7	V
V_{ADDR-3}	"0001010" Addr Pin Voltage		2.3		2.7	V
V_{ADDR-4}	"0001011" Addr Pin Voltage		3.3		5	V

THERMAL DESIGN NOTES

During normal operation, this device dissipates some power. The power dissipation depends on the selected communication mode (DiSEqC or 13/18 control word communication).
When the device is used in DiSEqC mode, at maximum rated output current (750mA), the voltage drop on the linear regulator lead to a total dissipated power that is about 1.65W.
If the control word communication mode is selected, at maximum rated current of 450mA, the total power dissipated is about 1W. By the way, during the 13/18V pulses code transmission (OM=VOM=1) the average power dissipation is higher than 1W because, in this case, before to start sending the 13/18V pulses code, the V_{UP} voltage must be forced in steady state at 21.7V by VOM=1, (22.7V if LLC=1) in order to ensure the proper code transition rise and fall timing while the V_{OUT} voltage is continuously switched between 13V and 18V; this means that, in the 13V half period the peak of power dissipation is about 3.8W typ. (@ Iout=450mA max.). Obviously this is the peak power dissipation as the average value during the code transmission has to be calculated taking into account the 0/1 bits combination.
The heat generated requires a suitable heatsink to keep the junction temperature below the overtemperature protection threshold. Assuming a 45°C temperature inside the Set-Top-Box case and a max continuos power dissipation of 1.65W, the total $R_{thj-amb}$ has to be less than 48°C/W.
While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the pcb ground layer to dissipate the heat coming from the IC body by mean the ground exposed pad present on the bottom side of the PSO-20 package.
Given for the PSO-20 an $R_{thj-case}$ equal to 2°C/W, a maximum of 46°C/W are left to the PCB heatsink.
This figure is achieved if a minimum of 6.5cm^2 copper area is placed just below the IC body. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In figure 9, is shown a suggested layout for the PSO-20 package with a dual layer PCB, where the IC exposed pad connected to GND and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when L=25mm, achieves an R_{thc-a} of about 32°C/W.
Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground exposed pad approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

Figure 9: PowerSO-20 Suggested Pcb Heatsink Layout



TYPICAL CHARACTERISTICS (unless otherwise specified T_j = 25°C)

Figure 10: Output Voltage vs Temperature

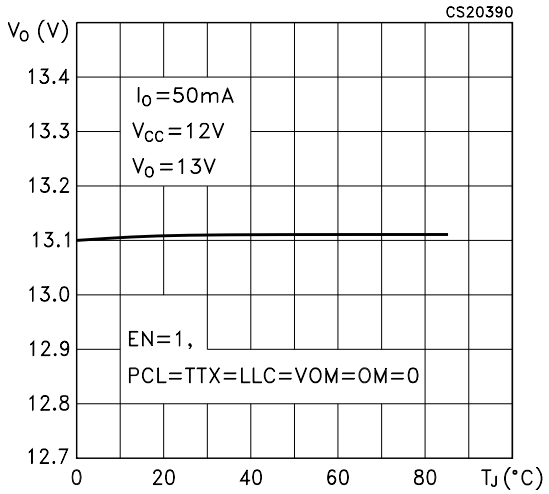


Figure 11: Output Voltage vs Temperature

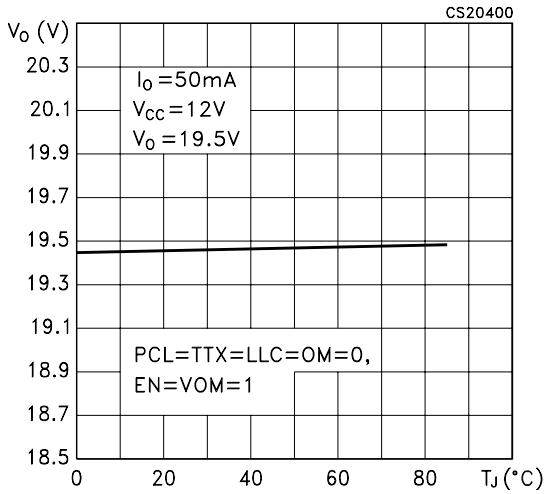


Figure 12: Load Regulation vs Temperature

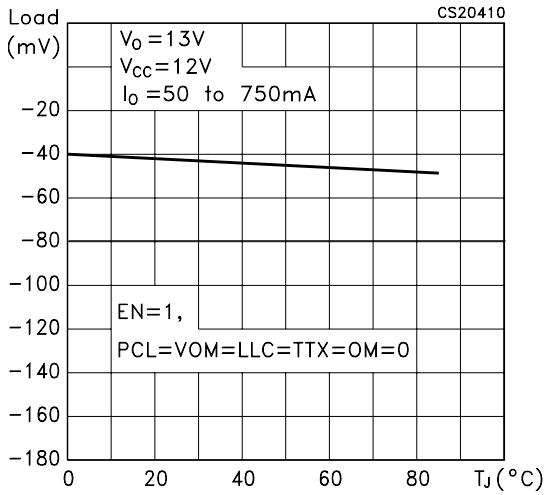


Figure 13: Supply Current vs Temperature

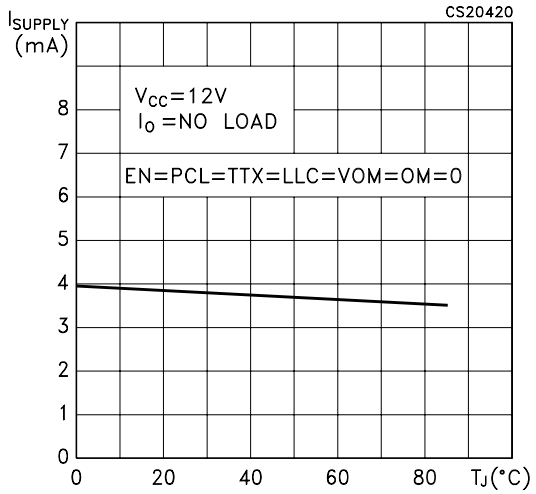


Figure 14: Supply Current vs Temperature

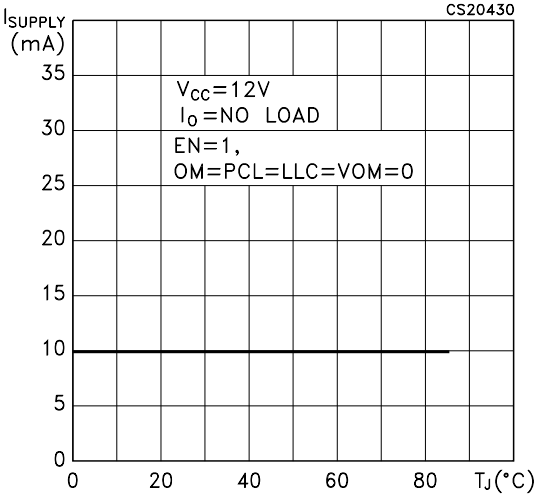


Figure 15: Supply Current vs Temperature

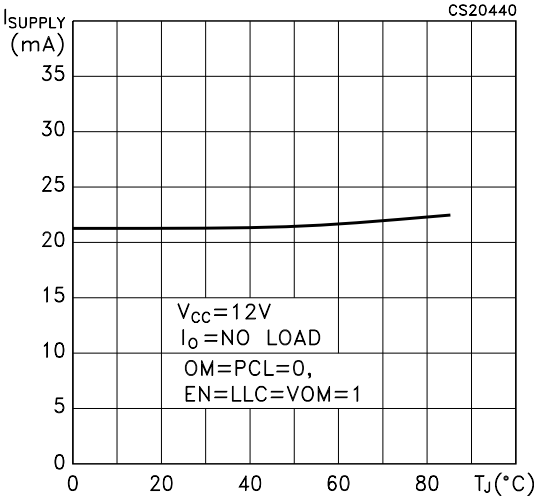


Figure 16: Dynamic Overload Protection ON Time vs Temperature

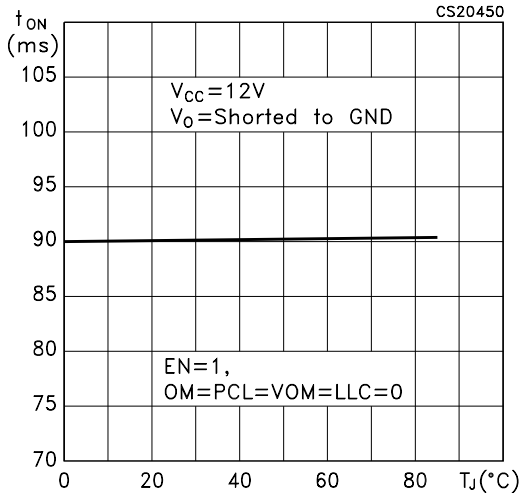


Figure 17: Dynamic Overload Protection OFF Time vs Temperature

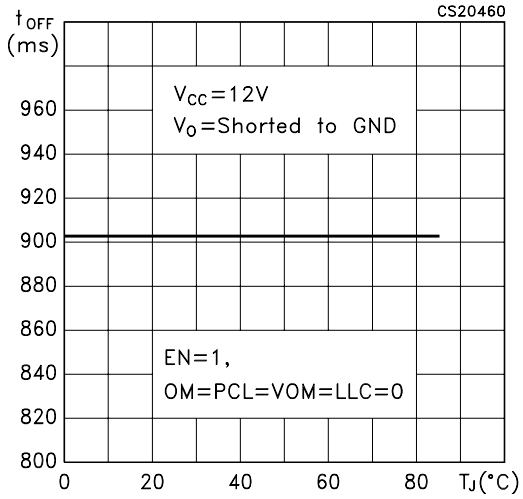


Figure 18: Output Current Limiting vs Temperature

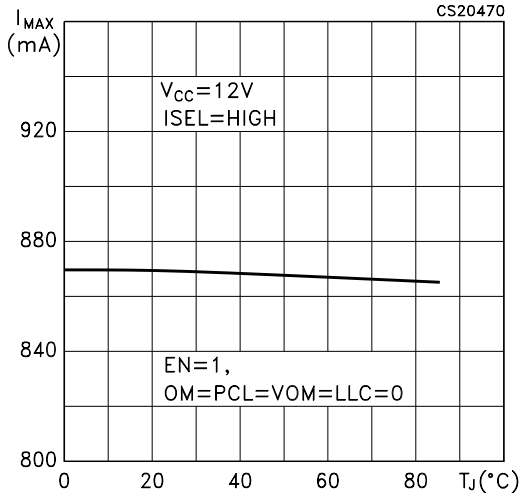


Figure 19: Output Current Limiting vs Temperature

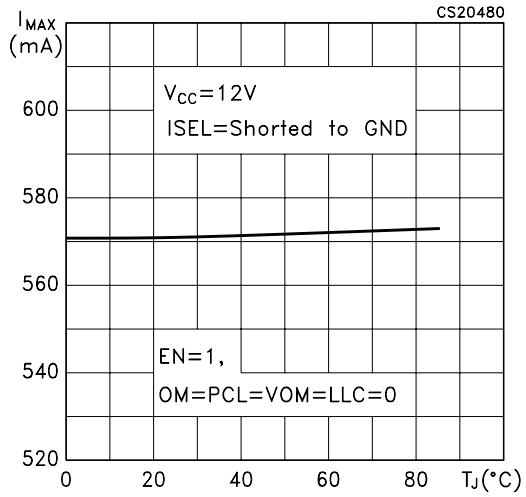


Figure 20: Tone Frequency vs Temperature

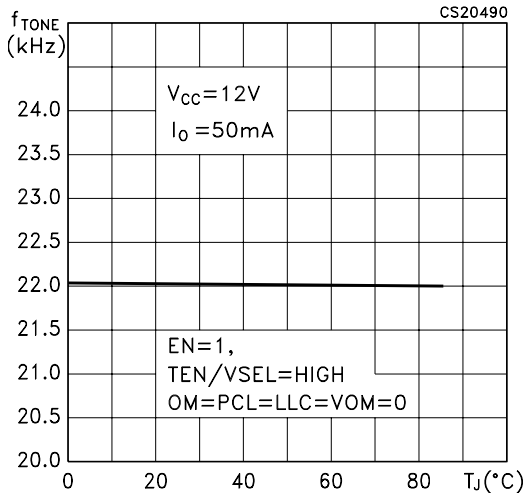


Figure 21: Tone Amplitude vs Temperature

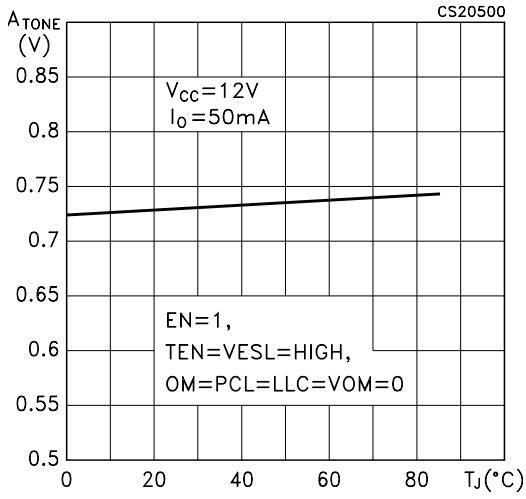


Figure 22: Tone Duty Cycle vs Temperature

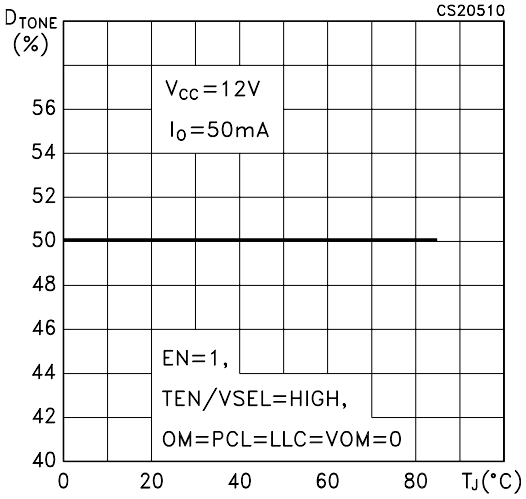


Figure 23: Tone Rise Time vs Temperature

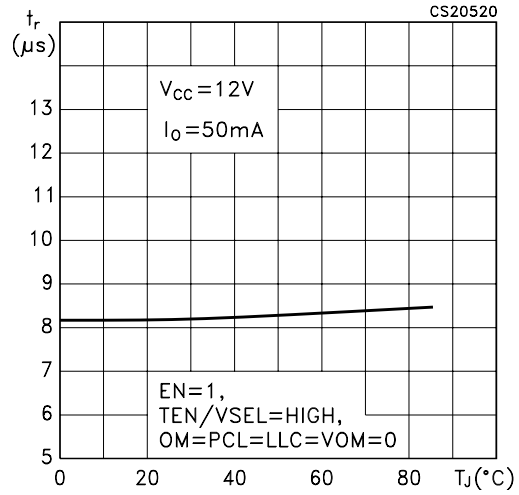


Figure 24: Tone Fall Time vs Temperature

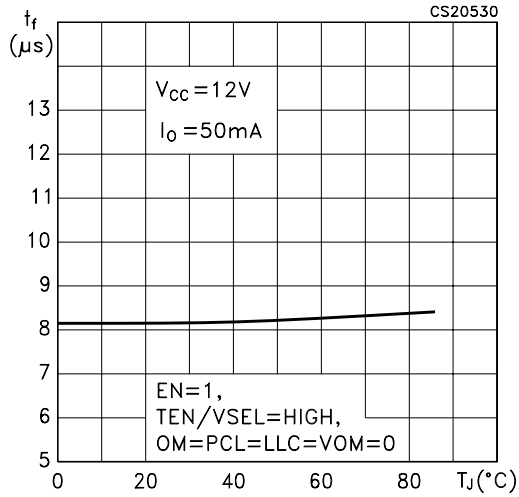


Figure 25: Undervoltage Lockout Threshold vs Temperature

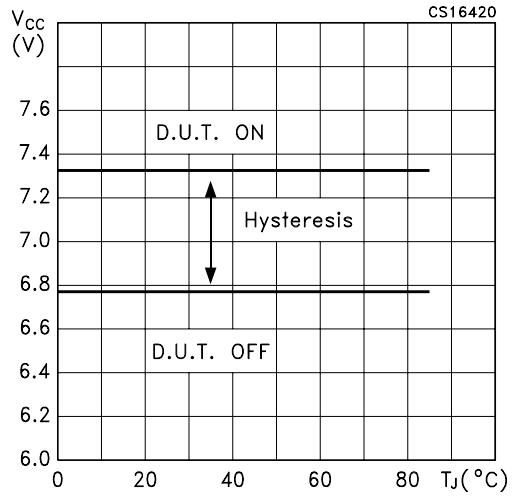


Figure 26: Output Backward Current vs Temperature

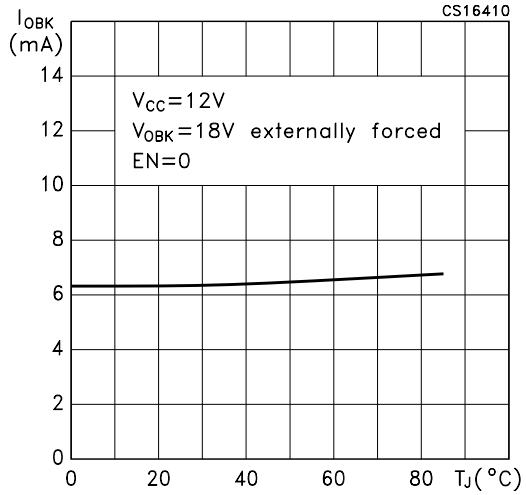


Figure 27: DC/DC Converter Efficiency vs Temperature

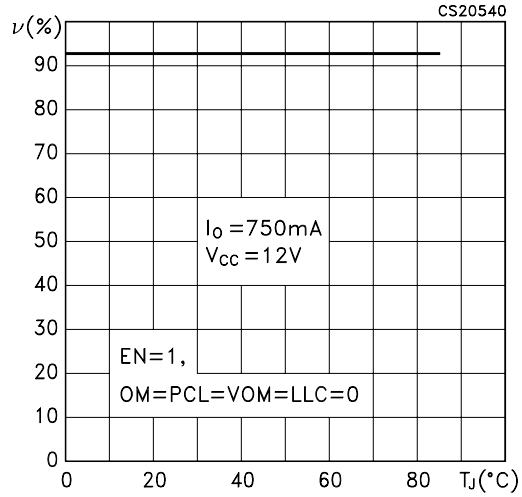


Figure 28: Current Limit Sense Voltage vs Temperature

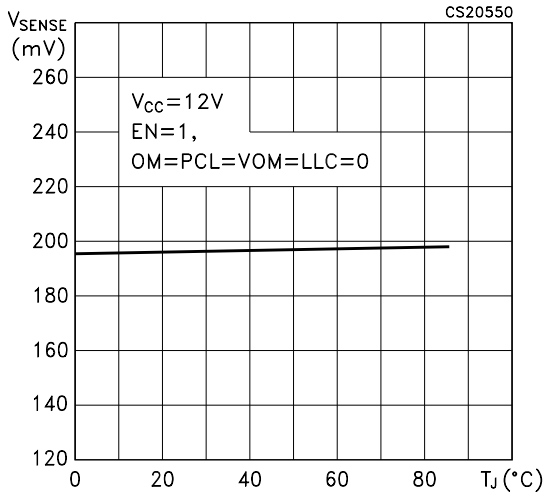
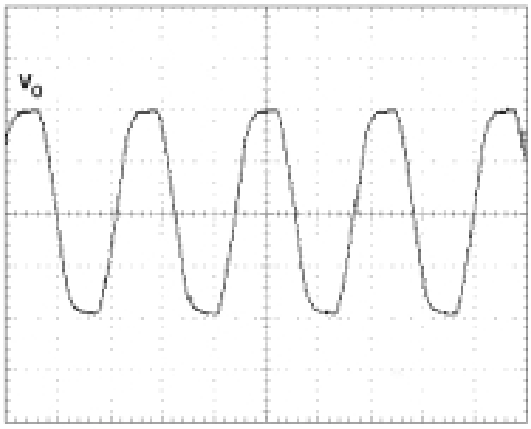
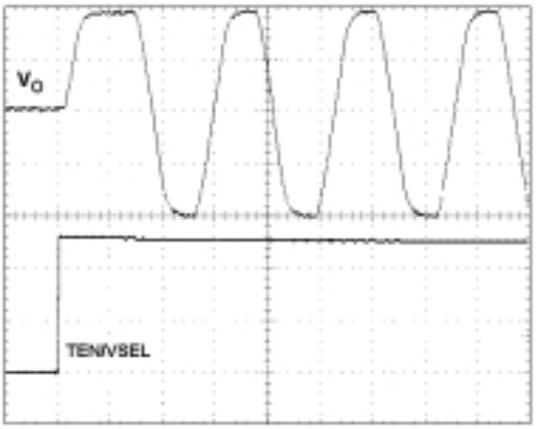


Figure 29: 22kHz Tone Waveform



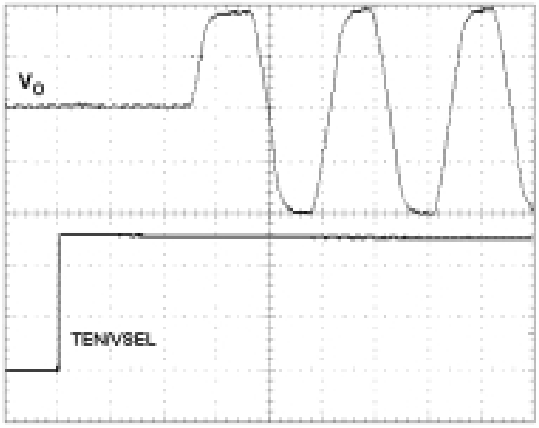
V_{CC}=12V, I_O=50mA, EN=TEN=1

Figure 30: TEN/VSEL Tone Enable Transient Response



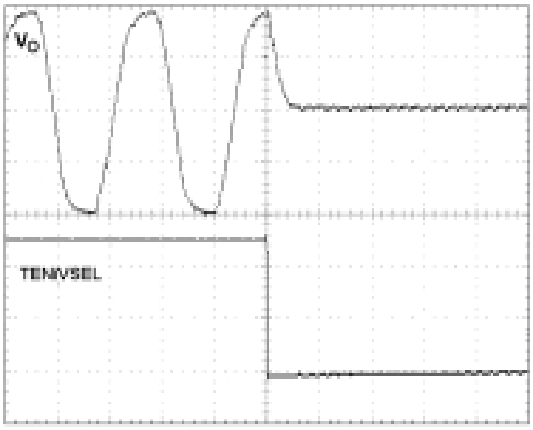
V_{CC}=12V, I_O=50mA, EN=1, Tone enabled by DSQIN Pin

Figure 31: TEN/VSEL Tone Enable Transient Response



V_{CC}=12V, I_O=50mA, EN=1, OM=0

Figure 32: TEN/VSEL Tone Disable Transient Response

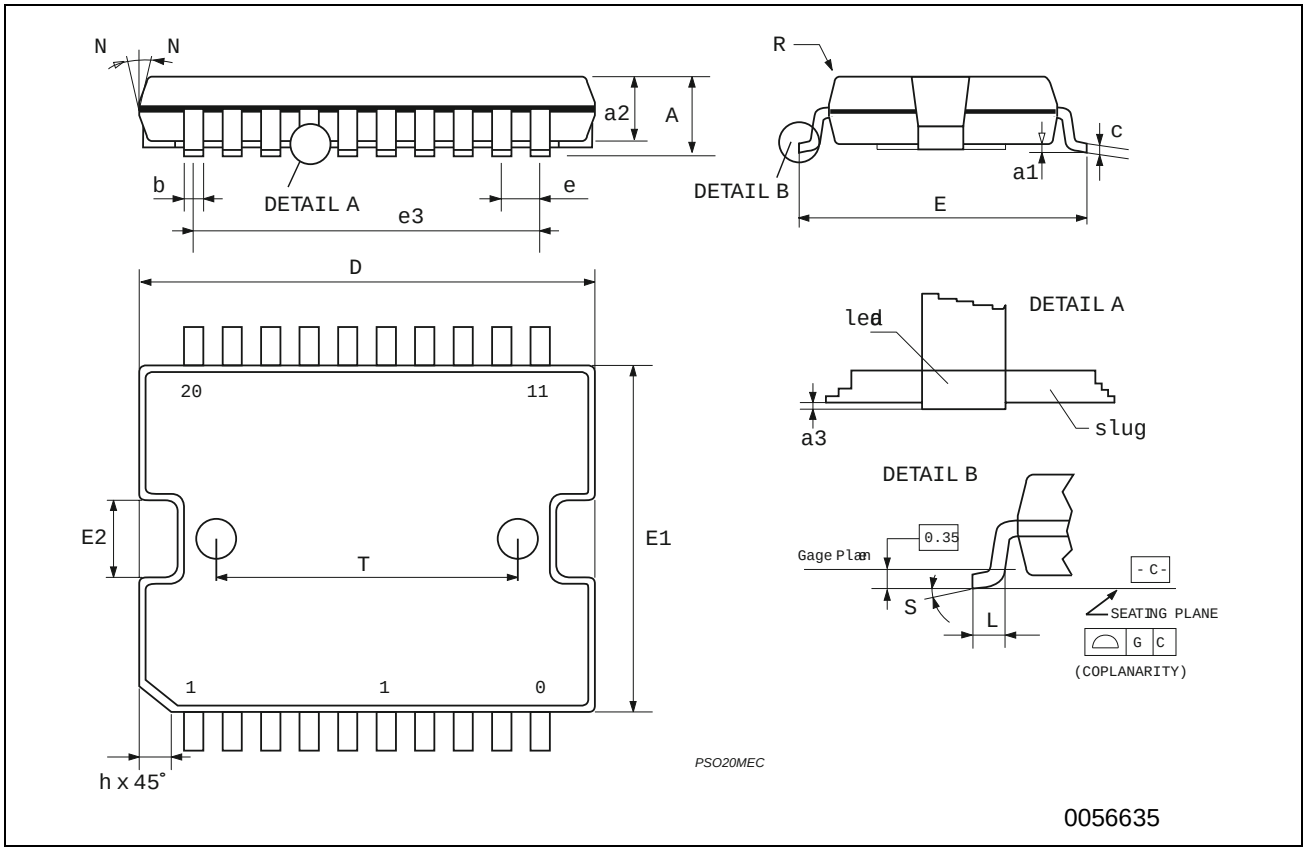


V_{CC}=12V, I_O=50mA, EN=1, OM=0

PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.0090		0.0013
D (1)	15.80		16.00	0.6220		0.630
E	13.90		14.50	0.5472		0.5710
e		1.27			0.0500	
e3		11.43			0.4500	
E1 (1)	10.90		11.10	0.4291		0.4370
E2			2.90			0.1141
G	0		0.10	0.0000		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N			10°			10°
S	0°		8°	0°		8°
T		10.0			0.3937	

(1) “D and E1” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.006”)



Tape & Reel PowerSO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	15.1		15.3	0.594		0.602
Bo	16.5		16.7	0.650		0.658
Ko	3.8		4.0	0.149		0.157
Po	3.9		4.1	0.153		0.161
P	23.9		24.1	0.941		0.949
W	23.7		24.3	0.933		0.957

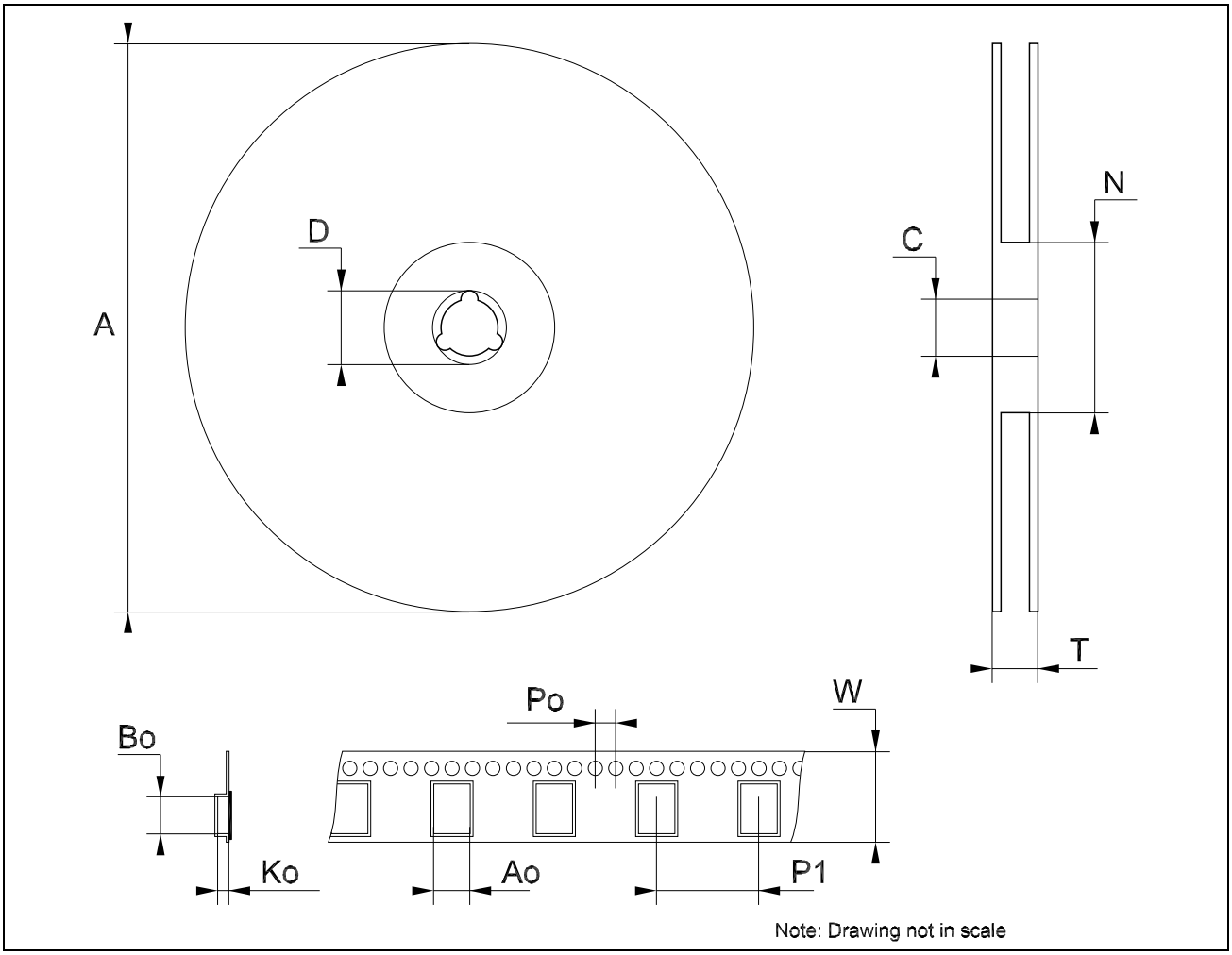


Table 9: Revision History

Date	Revision	Description of Changes
05-Jul-2004	1	First Release.