



MMC 22925/6/7/8

4-DIGIT COUNTERS WITH MULTIPLEXED 7-SEGMENT OUTPUT DRIVERS

GENERAL DESCRIPTION

These CMOS counters consist of a 4-counter, an internal output latch, NPN output sourcing drivers for a 7-segment display and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MMC 22925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs (16 pins package).

The MMC 22926 is like the MMC 22925 except that it has a Display Select and a Carry-Out used for cascading counters.

The Carry-Out signal goes high at 6000 and goes back low at 0000.

The MMC 22927 is like the MMC 22926 except that the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59:9).

The MMC 22928 is like the MMC 22926 except that the most significant digit divides by 2 rather than 10 and the Carry Out is an overflow indicator which goes high at 2000, and goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

FEATURES

- Supply voltage range 3 V to 6 V
- Internal multiplexing circuitry
- High segment sourcing current: 40 mA at $V_{out} = V_{DD} - 1.6$ V, $V_{DD} = 5$ V
- Guaranteed noise margin 1 V

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage	-0.3	to	6.5	V
V_i	Input voltage	-0.3	to	$V_{DD} + 0.3$	V
I_i	DC input current (any one input)			± 10	mA
P_{tot}	Total power dissipation	Refer to $P_{D(MAX)}$		vs T_A	Graph
T_A	Operating temperature	0	to	70	C
T_{stg}	Storage temperature	-40	to	125	C

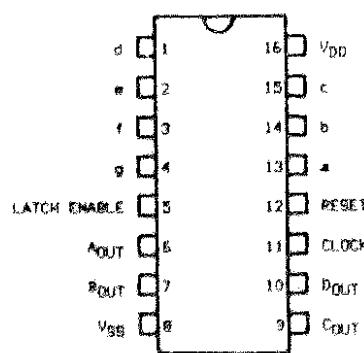
RECOMMENDED OPERATING CONDITIONS

V_{DD}^*	Supply voltage	3	to	6	V
V_i	Input voltage	0	to	V_{DD}	V
T_A	Operating temperature	0	to	70	C

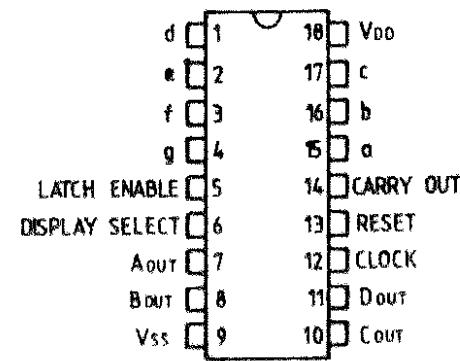
* All voltage values are referred to V_{SS} pin voltage

CONNECTION DIAGRAM - MMC 22925

MMC 22925

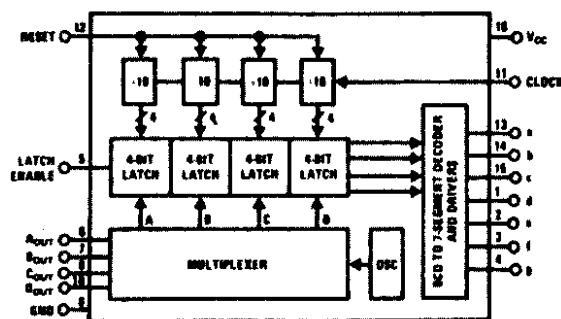
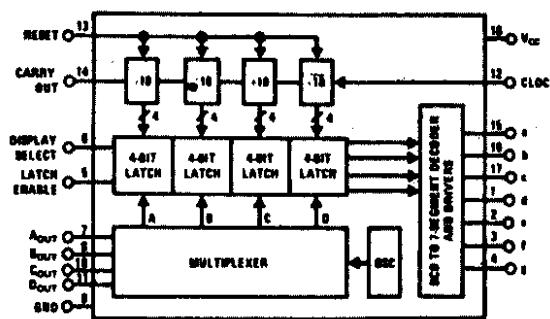
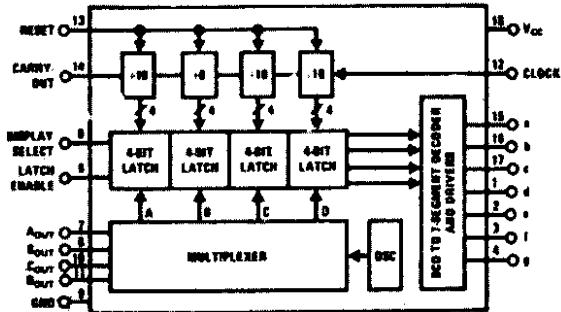
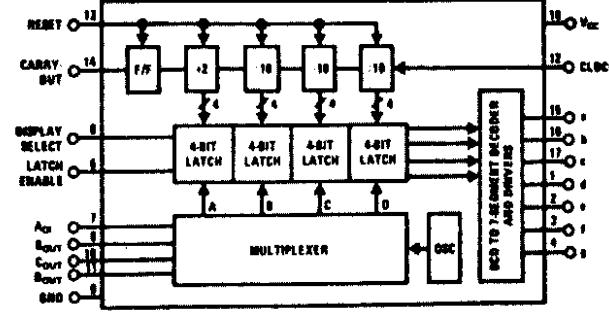


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FUNCTIONAL DESCRIPTION

- Reset** — Asynchronous, active high
Display Select — High, displays output of counter
Latch Enable — Low, displays output of latch
Clock — High, flow through condition
Clock — Low, latch condition
Clock — Negative edge sensitive
Digit Output — Current sourcing with 1 mA $V_{OUT} = 1.75$ V. Also sink capability = 2 LTTL loads
Carry-out — 2 LTTL loads (see carry-out waveforms)
Segment Output — Current sourcing with 80 mA $V_{OUT} = V_{DD} - 1.6$ V typical ($T_i = 25$ C). Also sink capability = 2 LTTL loads.

BLOCK DIAGRAM**MMC 22925****MMC 22926****MMC 22927****MMC 22928****STATIC ELECTRICAL CHARACTERISTICS**

(over recommended operating conditions)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS TO CMOS INTERFACE					
V_{IN} (1) Logical "1" Input Voltage	$V_{CC} = 5.0$ V	3.5		1.5	V
V_{IN} (0) Logical "0" Input Voltage	$V_{CC} = 5.0$ V			1.0	V
V_{OUT} (1) Logical "1" Output Voltage (Carry-Out and Digit Output Only)	$V_{CC} = 5.0$ V, $I_O = -10\mu A$	4.5			V
V_{OUT} (0) Logical "0" Output Voltage	$V_{CC} = 5.0$ V, $I_O = 10 \mu A$		0.5		V
I_{IN} (1) Logical "1" Input Current	$V_{CC} = 5.0$ V, $V_{IN} = 5$ V		0.005	1.0	μA
I_{IN} (0) Logical "0" Input Current	$V_{CC} = 5.0$ V, $V_{IN} = 0$ V	-1.0	-0.005		μA
I_{CC} Supply Current	$V_{CC} = 5.0$ V, Outputs Open Circuit, $V_{IN} = 0$ V or 5 V	20	1000		μA

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DRIVE					
V _{OUT}	Output Voltage (Segment Sourcing Output) $I_{OUT} = -65\text{mA}$, $V_{CC} = 5\text{V}$, $T_j = 25^\circ\text{C}$		$V_{CC} - 1.3$		V
	$I_{OUT} = -40\text{mA}$, $\begin{cases} T_j = 100^\circ\text{C} \\ V_{CC} = 5\text{V} \end{cases} V_{CC} - 1.6$ $\begin{cases} T_j = 150^\circ\text{C} \\ V_{CC} = 5\text{V} \end{cases} V_{CC} - 2$		$V_{CC} - 1.2$		V
R _{ON}	Output Resistance (Segment Sourcing Output) $I_{OUT} = -65\text{mA}$, $V_{CC} = 5\text{V}$, $T_j = 25^\circ\text{C}$	20	$V_{CC} - 1.4$		V
	$I_{OUT} = -40\text{mA}$, $\begin{cases} T_j = 100^\circ\text{C} \\ V_{CC} = 5\text{V} \end{cases} 30$ $\begin{cases} T_j = 150^\circ\text{C} \\ V_{CC} = 5\text{V} \end{cases} 35$	0.6	40	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.8	%/ $^\circ\text{C}$
I _{SOURCE}	Output Source Current (Digit Output) $V_{CC} = 4.75\text{V}$, $V_{OUT} = 1.75\text{V}$, -1 $T_j = 150^\circ\text{C}$		-2		mA
I _{SOURCE}	Output Source Current (Carry-out) $V_{CC} = 5\text{V}$, $V_{OUT} = 0\text{V}$ $T_j = 25^\circ\text{C}$	-1.75	-3.3		mA
I _{SINK}	Output Sink Current (All Outputs) $V_{CC} = 5\text{V}$, $V_{OUT} = V_{CC}$ $T_j = 25^\circ\text{C}$	1.75	3.6		mA
ϕ_{JA}^*	Thermal Resistance MMC 22925 MMC 22926/7/8		75	100	$^\circ\text{C}/\text{W}$
			70	90	$^\circ\text{C}/\text{W}$

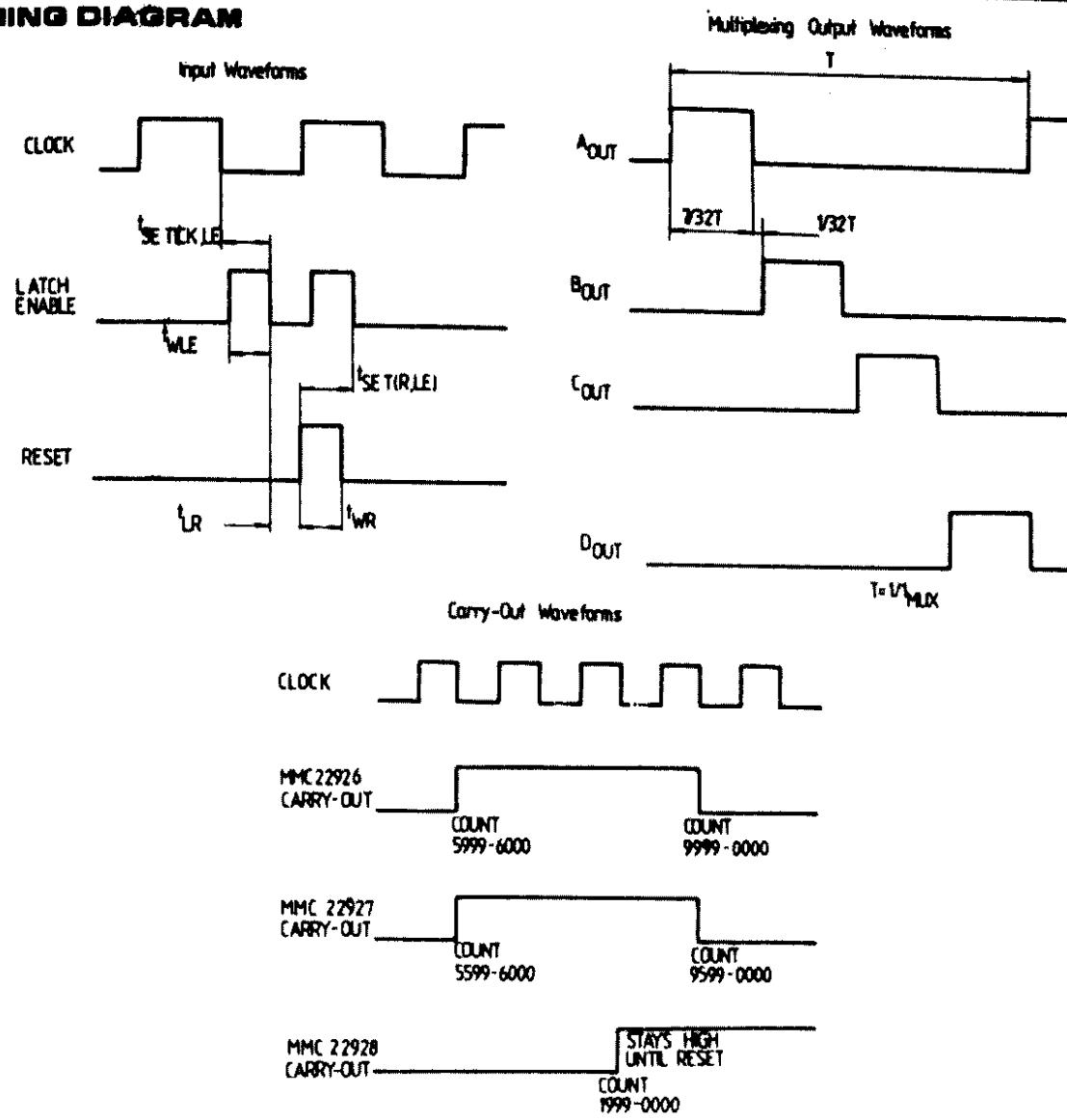
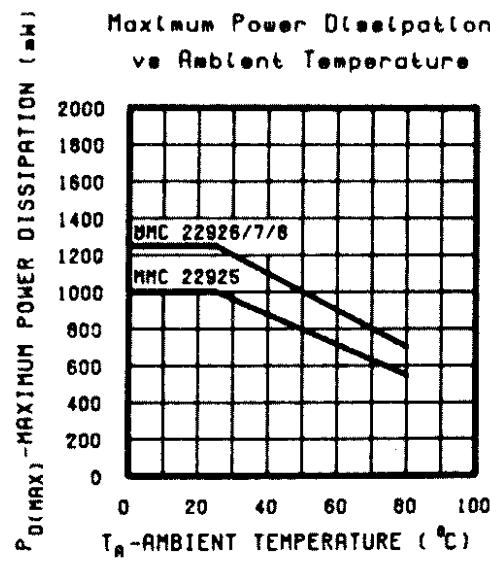
* ϕ_{JA} measured in free-air with device soldered into printed circuit board

DYNAMIC ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{MAX}	Maximum Clock Frequency $V_{CC} = 5.0\text{V}$ $T_j = 25^\circ\text{C}$ Square Wave Clock $T_j = 100^\circ\text{C}$	2	4		MHz
t _r , t _f	Maximum Clock Rise or Fall Time $V_{CC} = 5.0\text{V}$	1.5	3	15	μs
t _{WR}	Reset Pulse Width $V_{CC} = 5.0\text{V}$	$T_j = 25^\circ\text{C}$ 250	10		ns
		$T_j = 100^\circ\text{C}$ 320	125		ns
t _{WLE}	Latch Enable Pulse Width $V_{CC} = 5.0\text{V}$	$T_j = 25^\circ\text{C}$ 250	100		ns
		$T_j = 100^\circ\text{C}$ 320	125		ns
t _{SETICK,LE}	Clock Latch Enable Set-Up Time $V_{CC} = 5.0\text{V}$	$T_j = 25^\circ\text{C}$ 2500	1250		ns
		$T_j = 100^\circ\text{C}$ 3200	1600		ns
t _{LR}	Latch Enable to Reset Wait Time $V_{CC} = 5.0\text{V}$	$T_j = 25^\circ\text{C}$ 0	-100		ns
		$T_j = 100^\circ\text{C}$ 0	-100		ns
t _{SETIRLE}	Reset to Latch Enable Set-Up Time $V_{CC} = 5.0\text{V}$	$T_j = 25^\circ\text{C}$ 320	160		ns
		$T_j = 100^\circ\text{C}$ 400	200		ns
f _{MUX}	Multiplexing Output Frequency $V_{CC} = 5.0\text{V}$		1000		Hz
C _{IN}	Input Capacitance Any Input		5		pF

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TIMING DIAGRAM**TYPICAL PERFORMANCE CHARACTERISTICS**

TYPICAL APPLICATION