Freescale Semiconductor
Data Sheet: Advance Information

MCF5329DS
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MCF5329 ColdFire® Microprocessor Data Sheet

Supports MCF5327, MCF5328, & MCF5329

by: Microcontroller Division

The MCF532*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 3 ColdFire microarchitecture. All MCF532*x* devices contain a 32-Kbyte internal SRAM, an LCD controller, USB host and On-the-Go controllers, a 2-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, as well as other peripherals that enable the MCF532*x* family for use in general purpose industrial control applications. Optional peripherals include a Fast Ethernet controller, a CAN module, and cryptography hardware accelerators.

This document provides an overview of the MCF532*x* microprocessor family, focusing on its highly diverse feature set. It was written from the perspective of the MCF5329 device. However, it also pertains to the MCF5327, and MCF5328. See the following section for a summary of differences between the various devices of the MCF532*x* family.

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1 MCF532*x* Family Configurations

The following table compares the various device derivatives available within the MCF532*x* family.

Table 1. MCF532*x* Family Configurations

Module	MCF5327	MCF5328	MCF5329
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x
Core (System) Clock	up to 240 MHz		
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 80 MHz		
Performance (Dhrystone/2.1 MIPS)	up to 211		
Unified Cache	16 Kbytes		
Static RAM (SRAM)	32 Kbytes		
LCD Controller	x	x	x
SDR/DDR SDRAM Controller	x	x	x
USB 2.0 Host	x	x	x
USB 2.0 On-the-Go	x	x	x
UTMI+ Low Pin Interface (ULPI)	—	x	x
Synchronous Serial Interface (SSI)	—	x	x
Fast Ethernet Controller (FEC)	—	x	x
Cryptography Hardware Accelerators	—	—	x
FlexCAN 2.0B communication module	—	—	x
UARTs	3	3	3
I^2C	x	x	x
QSPI	x	x	x
PWM Module	x	x	x
Real Time Clock	x	x	x
32-bit DMA Timers	4	4	4
Watchdog Timer (WDT)	x	x	x
Periodic Interrupt Timers (PIT)	4	4	4
Edge Port Module (EPORT)	x	x	x
Interrupt Controllers (INTC)	2	2	2
16-channel Direct Memory Access (DMA)	x	x	x
FlexBus External Interface	x	x	x
General Purpose I/O Module (GPIO)	x	x	x
JTAG - IEEE® 1149.1 Test Access Port	x	x	x
Package	196 MAPBGA	256 MAPBGA	256 MAPBGA

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2 Ordering Information

Table 2. Orderable Part Numbers

Freescale Part Number	Description	Speed	Temperature
MCF5327CVM240	MCF5327 RISC Microprocessor, 196 MAPBGA	240 MHz	–40° to +85° C
MCF5328CVM240	MCF5328 RISC Microprocessor, 256 MAPBGA	240 MHz	–40° to +85° C
MCF5329CVM240	MCF5329 RISC Microprocessor, 256 MAPBGA	240 MHz	–40° to +85° C

3 Signal Descriptions

The following table lists all the MCF532*x* pins grouped by function. The "Dir" column is the direction for the primary function of the pin only. Refer to Section 4, "Mechanicals and Pinouts," for package diagrams. For a more detailed discussion of the MCF532*x* signals, consult the *MCF5329 Reference Manual* (MCF5329RM).

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A23), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 3. MCF5327/8/9 Signal Information and Muxing

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
Reset							
$\overline{\text{RESET}}$[2]	—	—	—	I	M12	N15	N15
$\overline{\text{RSTOUT}}$	—	—	—	O	P14	P14	P14
Clock							
EXTAL	—	—	—	I	L14	P16	P16
XTAL[2]	—	—	—	O	K14	N16	N16
EXTAL32K	—	—	—	I	M11	P13	P13
XTAL32K	—	—	—	O	N11	R13	R13

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
FB_CLK	—	—	—	O	L1	T2	T2
Mode Selection							
$\overline{\text{RCON}}$[2]	—	—	—	I	N7	M8	M8
DRAMSEL	—	—	—	I	G10	H12	H12
FlexBus							
A[23:22]	—	$\overline{\text{FB\_CS}}$[5:4]	—	O	B11,C11	C13, D13	C13, D13
A[21:16]	—	—	—	O	B12, A12, D11, C12, B13, A13	E13, A14, B14, C14, A15, B15	E13, A14, B14, C14, A15, B15
A[15:14]	—	SD_BA[1:0]	—	O	A14, B14	D14, B16	D14, B16
A[13:11]	—	SD_A[13:11]	—	O	C13, C14, D12	C15, C16, D15	C15, C16, D15
A10	—	—	—	O	D13	D16	D16
A[9:0]	—	SD_A[9:0]	—	O	D14, E11–14, F11–F14, G14	E14–E16, F13–F16, G16– G14	E14–E16, F13–F16, G16– G14
D[31:16]	—	SD_D[31:16][3]	—	O	H3–H1, J4–J1, K1, L4, M2, M3, N1, N2, P1, P2, N3	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5	M1–M4, N1–N4, T3, P4, R4, T4, N5, P5, R5, T5
D[15:1]	—	FB_D[31:17][3]	—	O	F4–F1, G4–G2, L5, N4, P4, M5, N5, P5, M6	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8	J3–J1, K4–K1, L2, R6, N7, P7, R7, T7, P8, R8
D0[2]	—	FB_D[16][3]	—	O	N6	T8	T8
$\overline{\text{BE/BWE}}$[3:0]	PBE[3:0]	$\overline{\text{SD\_DQM}}$[3:0]	—	O	H4, P3, G1, M4	L4, P6, L3, N6	L4, P6, L3, N6
$\overline{\text{OE}}$	PBUSCTL3	—	—	O	L7	R9	R9
$\overline{\text{TA}}$[2]	PBUSCTL2	—	—	I	G13	G13	G13
R/$\overline{\text{W}}$	PBUSCTL1	—	—	O	P6	N8	N8
$\overline{\text{TS}}$	PBUSCTL0	$\overline{\text{DACK0}}$	—	O	D2	H4	H4
Chip Selects							
$\overline{\text{FB\_CS}}$[5:4]	PCS[5:4]	—	—	O	—	B13, A13	B13, A13
FB_CS[3:1]	PCS[3:1]			O	A11, D10, C10	A12, B12, C12	A12, B12, C12

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
FB_CS0	—	—	—	O	B10	D12	D12
SDRAM Controller							
SD_A10	—	—	—	O	L2	P2	P2
SD_CKE	—	—	—	O	E1	H2	H2
SD_CLK	—	—	—	O	K3	R1	R1
SD_CLK	—	—	—	O	K2	R2	R2
SD_CS1	—	—	—	O	—	J4	J4
SD_CS0	—	—	—	O	E2	H1	H1
SD_DQS3	—	—	—	O	H5	L1	L1
SD_DQS2	—	—	—	O	L6	T6	T6
SD_SCAS	—	—	—	O	L3	P3	P3
SD_SRAS	—	—	—	O	M1	R3	R3
SD_SDR_DQS	—	—	—	O	K4	P1	P1
SD_WE	—	—	—	O	D1	H3	H3
External Interrupts Port[4]							
IRQ7[2]	PIRQ7[2]	—	—	I	H14	J13	J13
IRQ6[2]	PIRQ6[2]	USBHOST_VBUS_EN[2]	—	I	—	J14	J14
IRQ5[2]	PIRQ5[2]	USBHOST_VBUS_OC[2]	—	I	—	J15	J15
IRQ4[2]	PIRQ4[2]	SSI_MCLK[2]	—	I	H13	J16	J16
IRQ3[2]	PIRQ3[2]	—	—	I	H12	K14	K14
IRQ2[2]	PIRQ2[2]	USB_CLKIN[2]	—	I	J14	K15	K15
IRQ1[2]	PIRQ1[2]	DREQ1[2]	SSI_CLKIN[2]	I	J13	K16	K16
FEC							
FEC_MDC	PFECI2C3	I2C_SCL[2]	—	O	—	C1	C1
FEC_MDIO	PFECI2C2	I2C_SDA[2]	—	I/O	—	C2	C2
FEC_TXCLK	PFECH7	—	—	I	—	A2	A2
FEC_TXEN	PFECH6	—	—	O	—	B2	B2
FEC_TXD0	PFECH5	ULPI_DATA0	—	O	—	E4	E4
FEC_COL	PFECH4	ULPI_CLK	—	I	—	A8	A8
FEC_RXCLK	PFECH3	ULPI_NXT	—	I	—	C8	C8
FEC_RXDV	PFECH2	ULPI_STP	—	I	—	D8	D8

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
FEC_RXD0	PFECH1	ULPI_DATA4	—	I	—	C6	C6
FEC_CRS	PFECH0	ULPI_DIR	—	I	—	B8	B8
FEC_TXD[3:1]	PFECL[7:5]	ULPI_DATA[3:1]	—	O	—	D3–D1	D3–D1
FEC_TXER	PFECL4	—	—	O	—	B1	B1
FEC_RXD[3:1]	PFECL[3:1]	ULPI_DATA[7:5]	—	I	—	E7, A6, B6	E7, A6, B6
FEC_RXER	PFECL0	—	—	I	—	D4	D4
LCD Controller							
LCD_D17	PLCDDH1	CANTX	—	O	—	—	C9
LCD_D16	PLCDDH0	CANRX	—	O	—	—	D9
LCD_D17	PLCDDH1	—	—	O	A6	C9	—
LCD_D16	PLCDDH0	—	—	O	B6	D9	—
LCD_D15	PLCDDM7	FEC_COL	—	O	C6	A7	A7
LCD_D14	PLCDDM6	FEC_CRS	—	O	D6	B7	B7
LCD_D13	PLCDDM5	FEC_RXCLK	—	O	A5	C7	C7
LCD_D12	PLCDDM4	FEC_RXDV	—	O	B5	D7	D7
LCD_D[11:8]	PLCDDM[3:0]	FEC_RXD[3:0]	—	O	C5, D5, A4, B4	D6, E6, A5, B5	D6, E6, A5, B5
LCD_D7	PLCDDL7	FEC_RXER	—	O	C4	C5	C5
LCD_D6	PLCDDL6	FEC_TXCLK	—	O	B3	D5	D5
LCD_D5	PLCDDL5	FEC_TXEN	—	O	A3	A4	A4
LCD_D4	PLCDDL4	FEC_TXER	—	O	A2	A3	A3
LCD_D[3:0]	PLCDDL[3:0]	FEC_TXD[3:0]	—	O	D4, C3, D3, B2	B4, C4, B3, C3	B4, C4, B3, C3
LCD_ACD/ LCD_OE	PLCDCTLH0	—	—	O	D7	B9	B9
LCD_CLS	PLCDCTLL7	—	—	O	C7	A9	A9
LCD_CONTRAST	PLCDCTLL6	—	—	O	B7	D10	D10
LCD_FLM/ LCD_VSYNC	PLCDCTLL5	—	—	O	A7	C10	C10
LCD_LP/ LCD_HSYNC	PLCDCTLL4	—	—	O	A8	B10	B10
LCD_LSCLK	PLCDCTLL3	—	—	O	B8	A10	A10
LCD_PS	PLCDCTLL2	—	—	O	C8	A11	A11
LCD_REV	PLCDCTLL1	—	—	O	D8	B11	B11
LCD_SPL_SPR	PLCDCTLL0	—	—	O	B9	C11	C11

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
USB Host & USB On-the-Go							
USBOTG_M	—	—	—	I/O	J12	L15	L15
USBOTG_P	—	—	—	I/O	K13	L16	L16
USBHOST_M	—	—	—	I/O	L12	M15	M15
USBHOST_P	—	—	—	I/O	M13	M16	M16
FlexCAN (MCF5329 only)							
CANRX and CANTX do not have dedicated bond pads. Please refer to the following pins for muxing: I2C_SDA, SSI_RXD, or LCD_D16 for CANRX and I2C_SCL, SSI_TXD, or LCD_D17 for CANTX.							
PWM							
PWM7	PPWM7	—	—	I/O	—	H13	H13
PWM5	PPWM5	—	—	I/O	—	H14	H14
PWM3	PPWM3	DT3OUT	DT3IN	I/O	G12	H15	H15
PWM1	PPWM1	DT2OUT	DT2IN	I/O	G11	H16	H16
SSI							
SSI_MCLK	PSSI4	—	—	I/O	—	G4	G4
SSI_BCLK	PSSI3	$\overline{\text{U2CTS}}$	PWM7	I/O	—	F4	F4
SSI_FS	PSSI2	$\overline{\text{U2RTS}}$	PWM5	I/O	—	G3	G3
SSI_RXD[2]	PSSI1	U2RXD	CANRX	I	—	—	G2
SSI_TXD[2]	PSSI0	U2TXD	CANTX	O	—	—	G1
SSI_RXD[2]	PSSI1	U2RXD	—	I	—	G2	—
SSI_TXD[2]	PSSI0	U2TXD	—	O	—	G1	—
I²C							
I2C_SCL[2]	PFECI2C1	CANTX	U2TXD	I/O	—	—	F3
I2C_SDA[2]	PFECI2C0	CANRX	U2RXD	I/O	—	—	F2
I2C_SCL[2]	PFECI2C1	—	U2TXD	I/O	E3	F3	—
I2C_SDA[2]	PFECI2C0	—	U2RXD	I/O	E4	F2	—
DMA							
$\overline{\text{DACK}}$[1:0] and $\overline{\text{DREQ}}$[1:0] do not have dedicated bond pads. Please refer to the following pins for muxing: $\overline{\text{TS}}$ for $\overline{\text{DACK0}}$, DT0IN for $\overline{\text{DREQ0}}$, DT1IN for $\overline{\text{DACK1}}$, and $\overline{\text{IRQ1}}$ for $\overline{\text{DREQ1}}$.							
QSPI							
QSPI_CS2	PQSPI5	$\overline{\text{U2RTS}}$	—	O	P10	T12	T12
QSPI_CS1	PQSPI4	PWM7	USBOTG_ PU_EN	O	L11	T13	T13

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
QSPI_CS0	PQSPI3	PWM5	—	O	—	P11	P11
QSPI_CLK	PQSPI2	I2C_SCL[2]	—	O	N10	R12	R12
QSPI_DIN	PQSPI1	$\overline{\text{U2CTS}}$	—	I	L10	N12	N12
QSPI_DOUT	PQSPI0	I2C_SDA	—	O	M10	P12	P12
UARTs							
$\overline{\text{U1CTS}}$	PUARTL7	SSI_BCLK	—	I	C9	D11	D11
$\overline{\text{U1RTS}}$	PUARTL6	SSI_FS	—	O	D9	E10	E10
U1TXD	PUARTL5	SSI_TXD[2]	—	O	A9	E11	E11
U1RXD	PUARTL4	SSI_RXD[2]	—	I	A10	E12	E12
$\overline{\text{U0CTS}}$	PUARTL3	—	—	I	P13	R15	R15
$\overline{\text{U0RTS}}$	PUARTL2	—	—	O	N12	T15	T15
U0TXD	PUARTL1	—	—	O	P12	T14	T14
U0RXD	PUARTL0	—	—	I	P11	R14	R14
Note: The UART2 signals are multiplexed on the QSPI, SSI, DMA Timers, and I2C pins.							
DMA Timers							
DT3IN	PTIMER3	DT3OUT	U2RXD	I	C1	F1	F1
DT2IN	PTIMER2	DT2OUT	U2TXD	I	B1	E1	E1
DT1IN	PTIMER1	DT1OUT	$\overline{\text{DACK1}}$	I	A1	E2	E2
DT0IN	PTIMER0	DT0OUT	$\overline{\text{DREQ0}}$[2]	I	C2	E3	E3
BDM/JTAG[5]							
JTAG_EN[6]	—	—	—	I	J11	M13	M13
DSCLK	—	$\overline{\text{TRST}}$[2]	—	I	N14	P15	P15
PSTCLK	—	TCLK[2]	—	O	M7	T9	T9
$\overline{\text{BKPT}}$	—	TMS[2]	—	I	N13	R16	R16
DSI	—	TDI[2]	—	I	M14	N14	N14
DSO	—	TDO	—	O	P9	N11	N11
DDATA[3:0]	—	—	—	O	P7, L8, M8, N8	N9, P9, N10, P10	N9, P9, N10, P10
PST[3:0]	—	—	—	O	P8, L9, M9, N9	R10, T10, R11, T11	R10, T10, R11, T11

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Table 3. MCF5327/8/9 Signal Information and Muxing (continued)

Signal Name	GPIO	Alternate 1	Alternate 2	Dir.[1]	MCF5327 196 MAPBGA	MCF5328 256 MAPBGA	MCF5329 256 MAPBGA
Test							
TEST[6]	—	—	—	I	E10	A16	A16
PLL_TEST[7]	—	—	—	I	—	N13	N13
Power Supplies							
EVDD	—	—	—		E6, E7, F5–F7, H9, J8, J9, K8, K9	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10	E8, F5–F8, G5, G6, H5, H6, J11, K11, K12, L9–L11, M9, M10
IVDD	—	—	—		E5, K5, K10	E5, G12, M5, M11, M12	E5, G12, M5, M11, M12
PLL_VDD	—	—	—		H10	J12	J12
SD_VDD	—	—	—		E8, E9, F8–F10, J6, K6, J7, K7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7	E9, F9–F11, G11, H11, J5, J6, K5, K6, L5–L8, M6, M7
USBOTG_VDD	—	—	—		K12	L14	L14
VSS	—	—	—		G6–G9, H6–H8, P9	G7–G10, H7–H10, J7–10, K7–K10, L12, L13	G7–G10, H7–H10, J7–10, K7–K10, L12, L13
PLL_VSS	—	—	—		H11	K13	K13
USBHOST_VSS	—	—	—		L13	M14	M14

NOTES:
1 Refers to pin's primary function.
2 Pull-up enabled internally on this signal for this mode.
3 Primary functionality selected by asserting the DRAMSEL signal (SDR mode). Alternate functionality selected by negating the DRAMSEL signal (DDR mode). The GPIO module is not responsible for assigning these pins.
4 GPIO functionality is determined by the edge port module. The GPIO module is only responsible for assigning the alternate functions.
5 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.
6 Pull-down enabled internally on this signal for this mode.
7 Must be left floating for proper operation of the PLL.

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4 Mechanicals and Pinouts

This section contains drawings showing the pinout and the packaging and mechanical characteristics of the MCF532*x* devices.

NOTE

The mechanical drawings are the latest revisions at the time of publication of this document. The most up-to-date mechanical drawings can be found at the product summary page located at http://www.freescale.com/coldfire.

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4.1 Pinout—256 MAPBGA

Figure 1 shows a pinout of the MCF5328CVM240 and MCF5329CVM240 devices.

NOTE

The pin at location N13 (PLL_TEST) must be left floating, else improper operation of the PLL module will occur.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	NC	FEC_ TXCLK	LCD_ D4	LCD_ D5	LCD_ D9	FEC_ RXD2	LCD_ D15	FEC_ COL	LCD_ CLS	LCD_ LSCLK	LCD_ PS	FB_CS3	FB_CS4	A20	A17	TEST	A
B	FEC_ TXER	FEC_ TXEN	LCD_ D1	LCD_ D3	LCD_ D8	FEC_ RXD1	LCD_ D14	FEC_ CRS	LCD_ ACD/OE	LCD_LP/ HSYNC	LCD_ REV	FB_CS2	FB_CS5	A19	A16	A14	B
C	FEC_ MDC	FEC_ MDIO	LCD_ D0	LCD_ D2	LCD_ D7	FEC_ RXD0	LCD_ D13	FEC_ RXCLK	LCD_ D17	LCD_FLM/ VSYNC	LCD_ SPL_SPR	FB_CS1	A23	A18	A13	A12	C
D	FEC_ TXD1	FEC_ TXD2	FEC_ TXD3	FEC_ RXER	LCD_ D6	LCD_ D11	LCD_ D12	FEC_ RXDV	LCD_ D16	LCD_CON TRAST	U1CTS	FB_CS0	A22	A15	A11	A10	D
E	DT2IN	DT1IN	DT0IN	FEC_ TXD0	IVDD	LCD_ D10	FEC_ RXD3	EVDD	SD_VDD	U1RTS	U1TXD	U1RXD	A21	A9	A8	A7	E
F	DT3IN	I2C_ SDA	I2C_ SCL	SSI_ BCLK	EVDD	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	NC	A6	A5	A4	A3	F
G	SSI_ TXD	SSI_ RXD	SSI_FS	SSI_ MCLK	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	IVDD	TA	A0	A1	A2	G
H	SD_ CS0	SD_CKE	SD_WE	TS	EVDD	EVDD	VSS	VSS	VSS	VSS	SD_VDD	DRAM SEL	PWM7	PWM5	PWM3	PWM1	H
J	D13	D14	D15	SD_CS1	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	PLL_ VDD	IRQ7	IRQ6	IRQ5	IRQ4	J
K	D9	D10	D11	D12	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	EVDD	EVDD	PLL_ VSS	IRQ3	IRQ2	IRQ1	K
L	SD_ DQS3	D8	BE/ BWE1	BE/ BWE3	SD_VDD	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	EVDD	VSS	USB_ VSS	USBOTG _VDD	USB OTG_M	USB OTG_P	L
M	D31	D30	D29	D28	IVDD	SD_VDD	SD_VDD	RCON	EVDD	EVDD	IVDD	IVDD	JTAG_ EN	USBHOST _VSS	USB HOST_M	USB HOST_P	M
N	D27	D26	D25	D24	D19	BE/ BWE0	D6	R/W	DDATA3	DDATA1	TDO/ DSO	QSPI_ DIN	PLL_ TEST	TDI/DSI	RESET	XTAL	N
P	SD_DR _DQS	SD_A10	SD_CAS	D22	D18	BE/ BWE2	D5	D2	DDATA2	DDATA0	QSPI_ CS0	QSPI_ DOUT	EXTAL 32K	RSTOUT	TRST/ DSCLK	EXTAL	P
R	SD_CLK	SD_CLK	SD_RAS	D21	D17	D7	D4	D1	OE	PST3	PST1	QSPI_ CLK	XTAL 32K	U0RXD	U0CTS	TMS/ BKPT	R
T	NC	FB_CLK	D23	D20	D16	SD_ DQS2	D3	D0	TCLK/ PSTCLK	PST2	PST0	QSPI_ CS2	QSPI_ CS1	U0TXD	U0RTS	NC	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 1. MCF5328CVM240 and MCF5329CVM240 Pinout Top View (256 MAPBGA)

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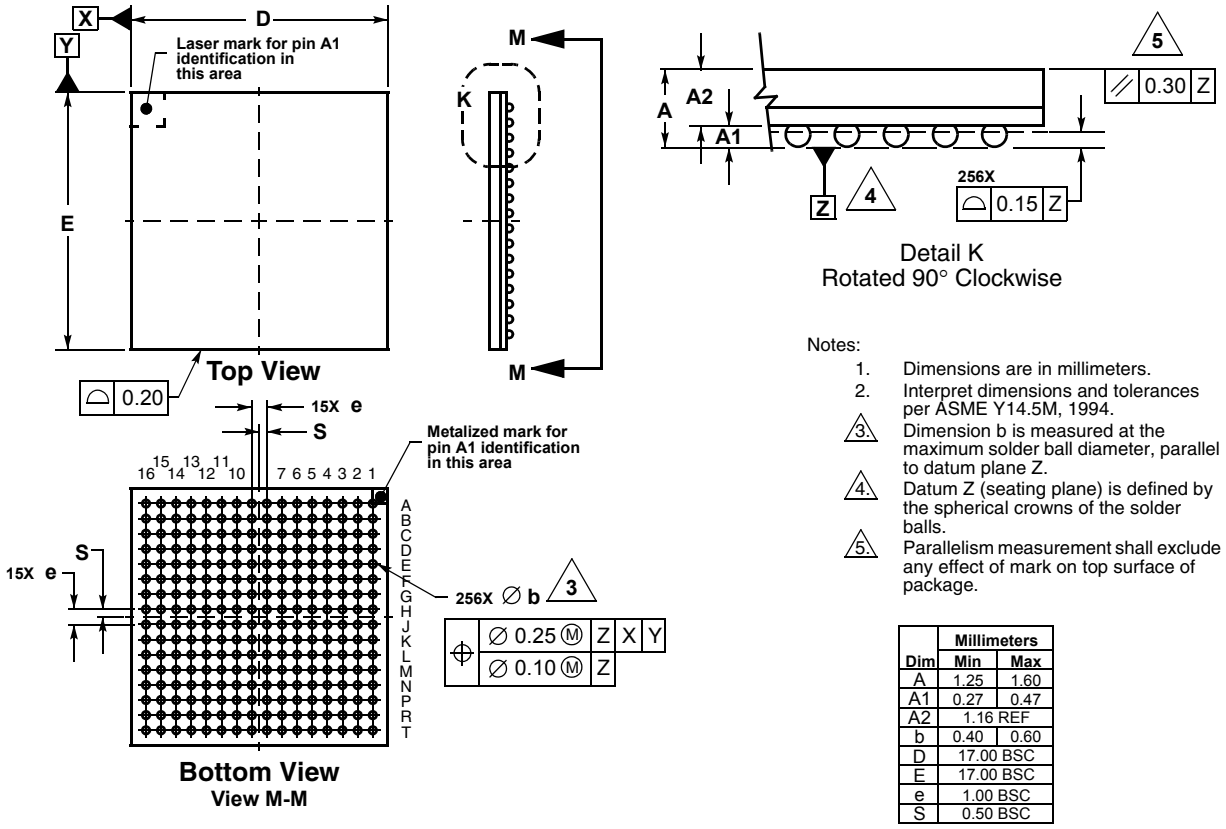
4.2 Package Dimensions—256 MAPBGA

Figure 2 shows MCF5328CVM240 and MCF5329CVM240 package dimensions.



Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Dim	Millimeters	
	Min	Max
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 2. 256 MAPBGA Package Outline

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4.3 Pinout—196 MAPBGA

The pinout for the MCF5327CVM240 package is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DT1IN	LCD_ D4	LCD_ D5	LCD_ D9	LCD_ D13	LCD_ D17	LCD_FLM/ VSYNC	LCD_LP/ HSYNC	U1TXD	U1RXD	FB_CS3	A20	A16	A15	A
B	D2TIN	LCD_ D0	LCD_ D6	LCD_ D8	LCD_ D12	LCD_ D16	LCD_CON TRAST	LCD_ LSCLK	LCD_ SPL_SPR	FB_CS0	A23	A21	A17	A14	B
C	DT3IN	DT0IN	LCD_ D2	LCD_ D7	LCD_ D11	LCD_ D15	LCD_ CLS	LCD_ PS	U1CTS	FB_CS1	A22	A18	A13	A12	C
D	SD_WE	TS	LCD_ D1	LCD_ D3	LCD_ D10	LCD_ D14	LCD_ ACD/OE	LCD_ REV	U1RTS	FB_CS2	A19	A11	A10	A9	D
E	SD_CKE	SD_CS0	I2C_SCL	I2C_SDA	IVDD	EVDD	EVDD	SD_VDD	SD_VDD	TEST	A8	A7	A6	A5	E
F	D12	D13	D14	D15	EVDD	EVDD	EVDD	SD_VDD	SD_VDD	SD_VDD	A4	A3	A2	A1	F
G	BE/ BWE1	D8	D9	D10	D11	VSS	VSS	VSS	VSS	DRAM SEL	PWM1	PWM3	TA	A0	G
H	D29	D30	D31	BE/ BWE3	SD_ DQS3	VSS	VSS	VSS	EVDD	PLL_ VDD	PLL_ VSS	IRQ3	IRQ4	IRQ7	H
J	D25	D26	D27	D28	SD_VDD	SD_VDD	SD_VDD	EVDD	EVDD	IVDD	JTAG_ EN	USB OTG_M	IRQ1	IRQ2	J
K	D24	SD_CLK	SD_CLK	SD_DR_ DQS	IVDD	SD_ DQS2	SD_VDD	EVDD	EVDD	IVDD	EVDD	USBHOST _VDD	USB OTG_P	XTAL	K
L	FB_CLK	SD_A10	SD_CAS	D23	D7	D1	TCLK/ PSTCLK	DDATA1	PST1	QSPI_ DIN	QSPI_ CS1	USB HOST_M	USBHOST _VSS	EXTAL	L
M	SD_RAS	D22	D21	BE/ BWE0	D4	D0	RCON	DDATA0	PST0	QSPI_ DOUT	EXTAL 32K	RESET	USB HOST_P	TDI/DSI	M
N	D20	D19	D16	D6	D3	R/W	DDATA3	PST3	TDO/ DSO	QSPI_ CLK	XTAL 32K	U0RTS	TMS/ BKPT	TRST/ DSCLK	N
P	D18	D17	BE/ BWE2	D5	D2	OE	DDATA2	PST2	VSS	QSPI_ CS2	U0RXD	U0TXD	U0CTS	RSTOUT	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 3. MCF5327CVM240 Pinout Top View (196 MAPBGA)

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4.4 Package Dimensions—196 MAPBGA

Figure 4 shows the MCF5327CVM240 package dimensions.

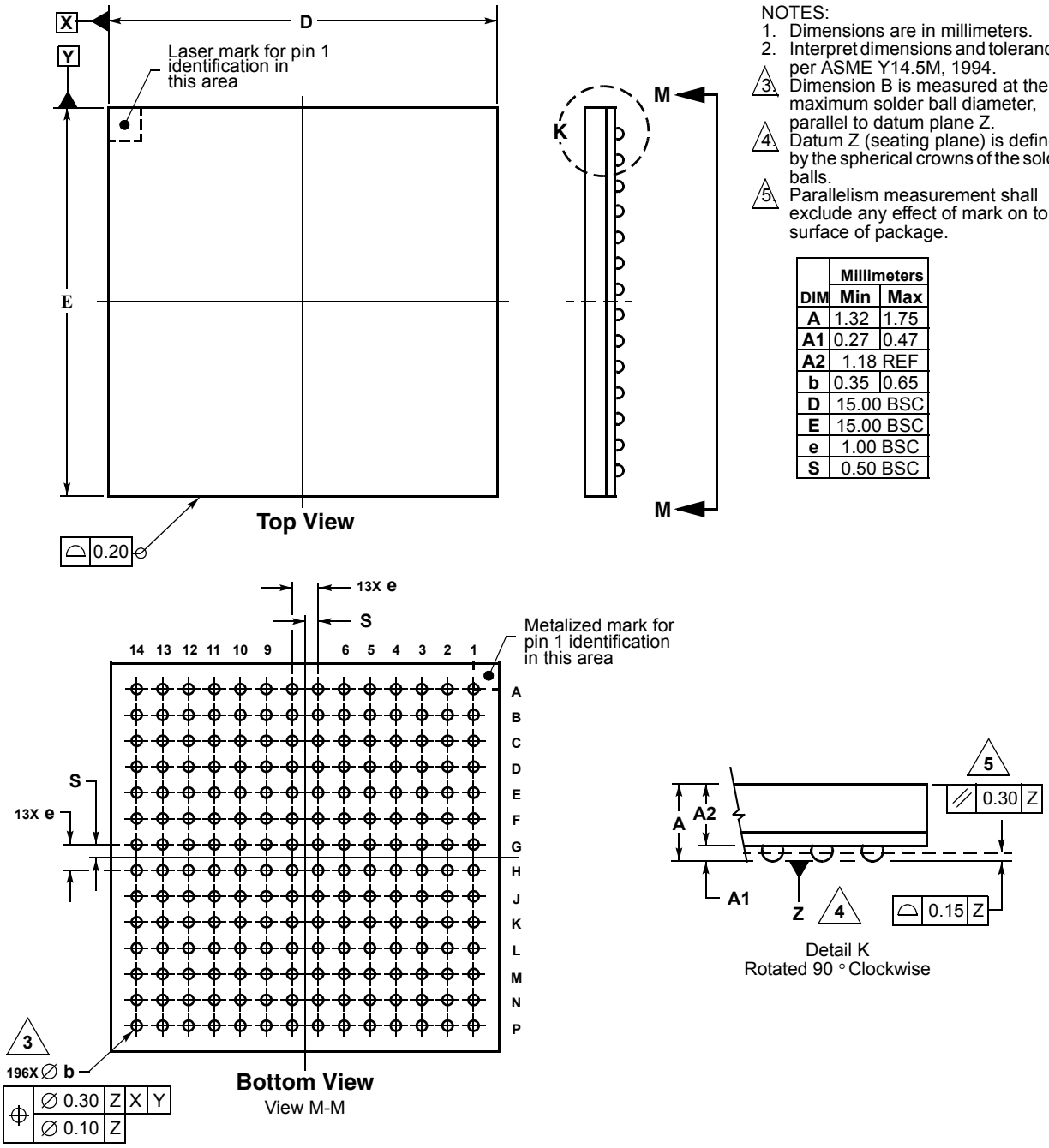

Figure 4. 196 MAPBGA Package Dimensions (Case No. 1128A-01)

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5 Preliminary Electrical Characteristics

This document contains electrical specification tables and reference timing diagrams for the MCF5329 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5329.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this MCU document supersede any values found in the module specifications.

5.1 Maximum Ratings

Table 4. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	IV_{DD}	– 0.5 to +2.0	V
CMOS Pad Supply Voltage	EV_{DD}	– 0.3 to +4.0	V
DDR/Memory Pad Supply Voltage	SDV_{DD}	– 0.3 to +4.0	V
PLL Supply Voltage	$PLLV_{DD}$	– 0.3 to +2.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to +3.6	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [3, 4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to +85	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

NOTES:
1. Functional operating conditions are given in Section 5.4, “DC Electrical Specifications.” Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Continued operation at these levels may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or EV_{DD}).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and EV_{DD}.

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5 Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > EV_{DD}$) is greater than I_{DD}, the injection current may flow out of EV_{DD} and could result in external power supply going out of regulation. Insure external EV_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock). Power supply must maintain regulation within operating EV_{DD} range during instantaneous and operating maximum current conditions.

5.2 Thermal Characteristics

Table 5. Thermal Characteristics

Characteristic		Symbol	256MBGA	196MBGA	Unit
Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JMA}	26[1,2]	32[1,2]	°C/W
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	23[1,2]	29[1,2]	°C/W
Junction to board		θ_{JB}	15[3]	20[3]	°C/W
Junction to case		θ_{JC}	10[4]	10[4]	°C/W
Junction to top of package		Ψ_{jt}	2[1,5]	2[1,5]	°C/W
Maximum operating junction temperature		T_j	105	105	°C

NOTES:
1 θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2 Per JEDEC JESD51-6 with the board horizontal.
3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \qquad \textit{Eqn. 1}$$

Where:

T_A = Ambient Temperature, °C

Q_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = P_{INT} + $P_{I/O}$

P_{INT} = $I_{DD} \times IV_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

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For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = \frac{K}{(T_J + 273°C)} \quad \textit{Eqn. 2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A \times 273°C) + Q_{JMA} \times P_D^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

5.3 ESD Protection

Table 6. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V

NOTES:
1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

5.4 DC Electrical Specifications

Table 7. DC Electrical Specifications

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	IV_{DD}	1.4	1.6	V
PLL Supply Voltage	$PLLV_{DD}$	1.4	1.6	V
CMOS Pad Supply Voltage	EV_{DD}	3.0	3.6	V
Mobile DDR/Bus Pad Supply Voltage	SDV_{DD}	1.65	1.95	V
DDR/Bus Pad Supply Voltage	SDV_{DD}	2.25	2.75	V
SDR/Bus Pad Supply Voltage	SDV_{DD}	3.0	3.6	V
USB Supply Voltage	$USBV_{DD}$	3.0	3.6	V
CMOS Input High Voltage	EV_{IH}	2	EV_{DD} + 0.05	V
CMOS Input Low Voltage	EV_{IL}	-0.05	0.8	V
Mobile DDR/Bus Input High Voltage	SDV_{IH}	TBD	SDV_{DD} + 0.05	V
Mobile DDR/Bus Input Low Voltage	SDV_{IL}	-0.05	TBD	V
DDR/Bus Input High Voltage	SDV_{IH}	2	SDV_{DD} + 0.05	V
DDR/Bus Input Low Voltage	SDV_{IL}	-0.05	0.8	V

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Table 7. DC Electrical Specifications (continued)

Characteristic	Symbol	Min	Max	Unit
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	-1.0	1.0	µA
CMOS Output High Voltage I_{OH} = –5.0 mA	EV_{OH}	EV_{DD} - 0.4	—	V
CMOS Output Low Voltage I_{OL} = 5.0 mA	EV_{OL}	—	0.4	V
DDR/Bus Output High Voltage I_{OH} = –5.0 mA	SDV_{OH}	SDV_{DD} - 0.4	—	V
DDR/Bus Output Low Voltage I_{OL} = 5.0 mA	SDV_{OL}	—	0.4	V
Weak Internal Pull-Up Device Current, tested at V_{IL} Max.[1]	I_{APU}	-10	-130	µA
Input Capacitance [2] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

NOTES:
1 Refer to the signals section for pins having weak internal pull-up devices.
2 This parameter is characterized before qualification rather than 100% tested.

5.4.1 PLL Power Filtering

To further enhance noise isolation, an external filter is strongly recommended for PLL analog V_{DD} pins. The filter shown in Figure 5 should be connected between the board V_{DD} and the $PLLV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $PLLV_{DD}$ pin as possible.

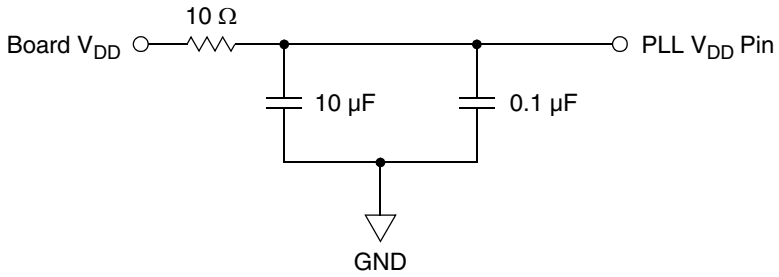

Figure 5. System PLL V_{DD} Power Filter

5.4.2 USB Power Filtering

To minimize noise, external filters are required for each of the USB power pins. The filter shown in Figure 6 should be connected between the board EV_{DD} or IV_{DD} and each of the $USBV_{DD}$ pins. The resistor and capacitors should be placed as close to the dedicated $USBV_{DD}$ pin as possible.

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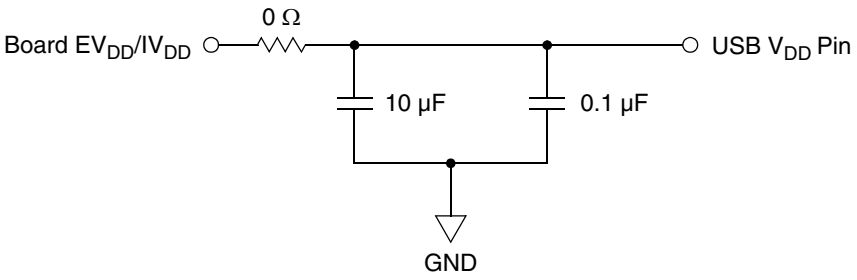


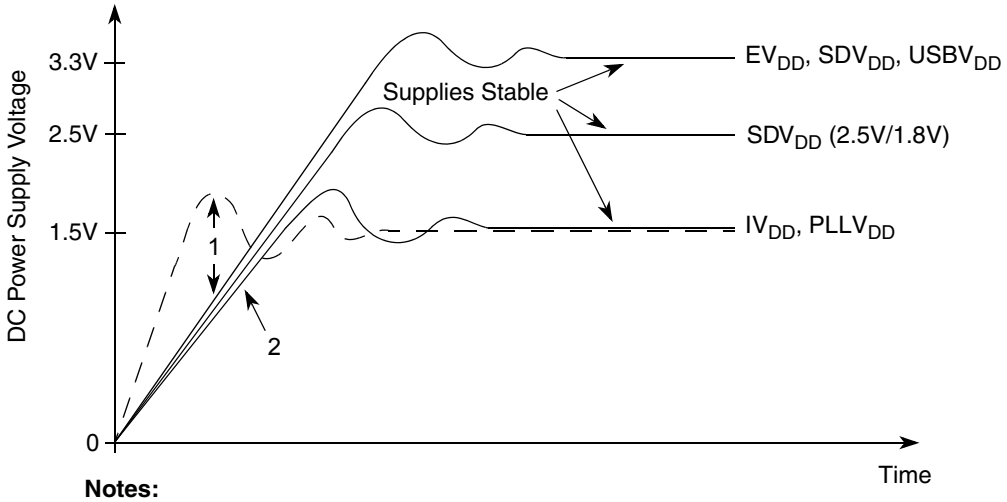
Figure 6. USB V_{DD} Power Filter

NOTE

In addition to the above filter circuitry, a 0.01 F capacitor is also recommended in parallel with those shown.

5.4.3 Supply Voltage Sequencing and Separation Cautions

Figure 7 shows situations in sequencing the I/O V_{DD} (EV_{DD}), SDRAM V_{DD} (SDV_{DD}), PLL V_{DD} ($PLLV_{DD}$), and Core V_{DD} (IV_{DD}).



Notes:
1. IVDD should not exceed EVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that IVDD/PLLVDD should track EVDD/SDVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (EVDD, SDVDD, IVDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

Figure 7. Supply Voltage Sequencing and Separation Cautions

The relationship between SDV_{DD} and EV_{DD} is non-critical during power-up and power-down sequences. Both SDV_{DD} (2.5V or 3.3V) and EV_{DD} are specified relative to IV_{DD}.

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5.4.3.1 Power Up Sequence

If EV_{DD}/SDV_{DD} are powered up with IV_{DD} at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the EV_{DD}/SDV_{DD} to be in a high impedance state. There is no limit on how long after EV_{DD}/SDV_{DD} powers up before IV_{DD} must powered up. IV_{DD} should not lead the EV_{DD}, SDV_{DD} or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 μs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 μs or slower rise time for all supplies.
2. $IV_{DD}/PLLV_{DD}$ and EV_{DD}/SDV_{DD} should track up to 0.9 V, then separate for the completion of ramps with $EV_{DD}/SD\ V_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

5.4.3.2 Power Down Sequence

If $IV_{DD}/PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after IV_{DD} and $PLLV_{DD}$ power down before EV_{DD} or SDV_{DD} must power down. IV_{DD} should not lag EV_{DD}, SDV_{DD}, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $IV_{DD}/PLLV_{DD}$ to 0 V.
2. Drop EV_{DD}/SDV_{DD} supplies.

5.5 Power Consumption Specifications

Estimated maximum RUN mode power consumption measurements are shown in the below figure.

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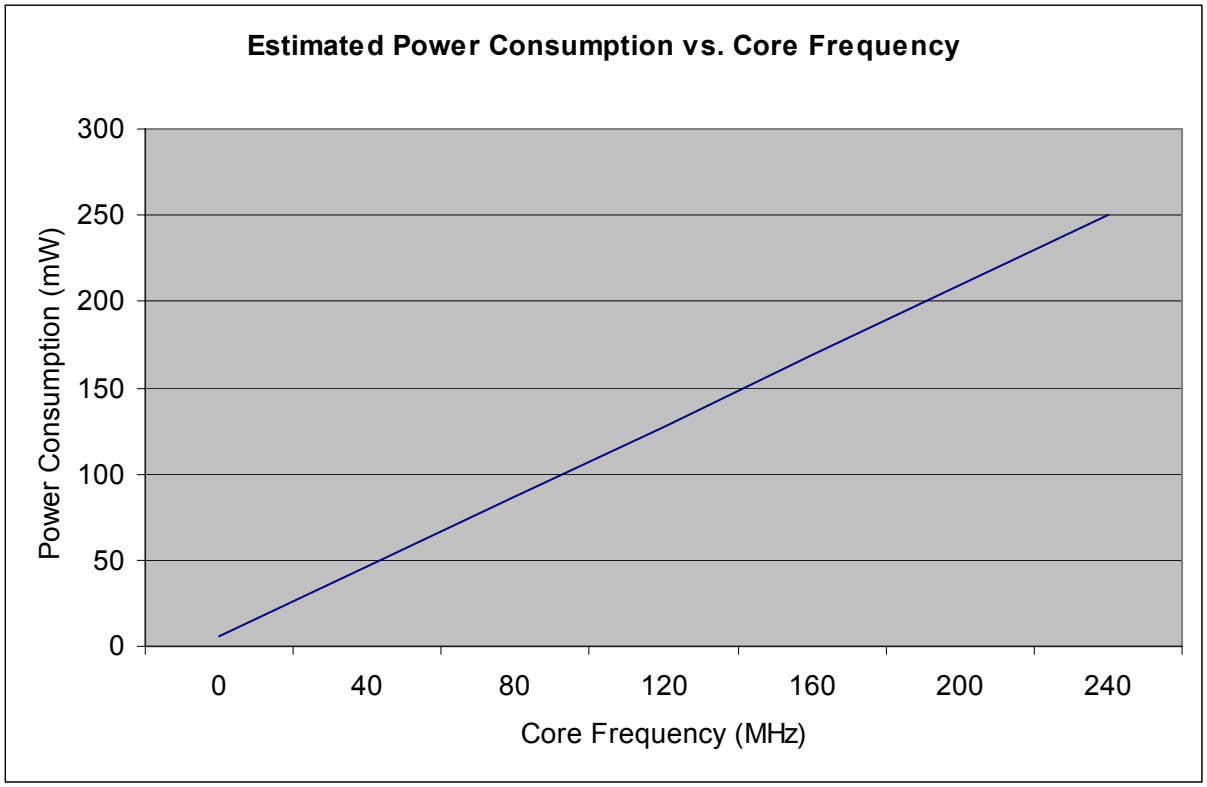

Figure 8. Estimated Maximum RUN Mode Power Consumption

Table 8 lists estimated maximum power and current consumption for the device in various operating modes.

Table 8. Estimated Maximum Power Consumption Specifications

Characteristic	Symbol	Typical	Max	Unit
Run Mode - Total Power Dissipation Static Dynamic		— — —	250 5.74 244	mW mW mW
Core Operating Supply Current [1] Run Mode	I_{DD}	—	TBD	mA
Pad Operating Supply Current Run Mode (application dependent) Wait Mode Stop Mode	EI_{DD}	— — —	144 96 1	mA mA mA

NOTES:
1 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

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5.6 Oscillator and PLL Electrical Characteristics

Table 9. PLL Electrical Characteristics

Num	Characteristic	Symbol	Min. Value	Max. Value	Unit
1	PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 TBD TBD	 16 16	 MHz MHz
2	Core frequency CLKOUT Frequency[1]	f_{sys} $f_{sys/3}$	TBD TBD	240 80	MHz MHz
3	Crystal Start-up Time[2, 3]	t_{cst}	—	10	ms
4	EXTAL Input High Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{IHEXT} V_{IHEXT}	 TBD TBD	 TBD TBD	 V V
5	EXTAL Input Low Voltage Crystal Mode[4] All other modes (External, Limp)	 V_{ILEXT} V_{ILEXT}	 TBD TBD	 TBD TBD	 V V
6	XTAL Load Capacitance[2]		5	30	pF
7	PLL Lock Time [2, 5]	t_{lpll}	—	1	ms
8	Duty Cycle of reference [2]	t_{dc}	40	60	%

NOTES:
1 All internal registers retain data at 0 Hz.
2 This parameter is guaranteed by characterization before qualification rather than 100% tested.
3 Proper PC board layout procedures must be followed to achieve specifications.
4 This parameter is guaranteed by design rather than 100% tested.
5 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

5.7 External Interface Timing Characteristics

Table 10 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the FB_CLK output.

All other timing relationships can be derived from these values. Timings listed in Table 10 are shown in Figure 10 and Figure 11.

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* The timings are also valid for inputs sampled on the negative clock edge.

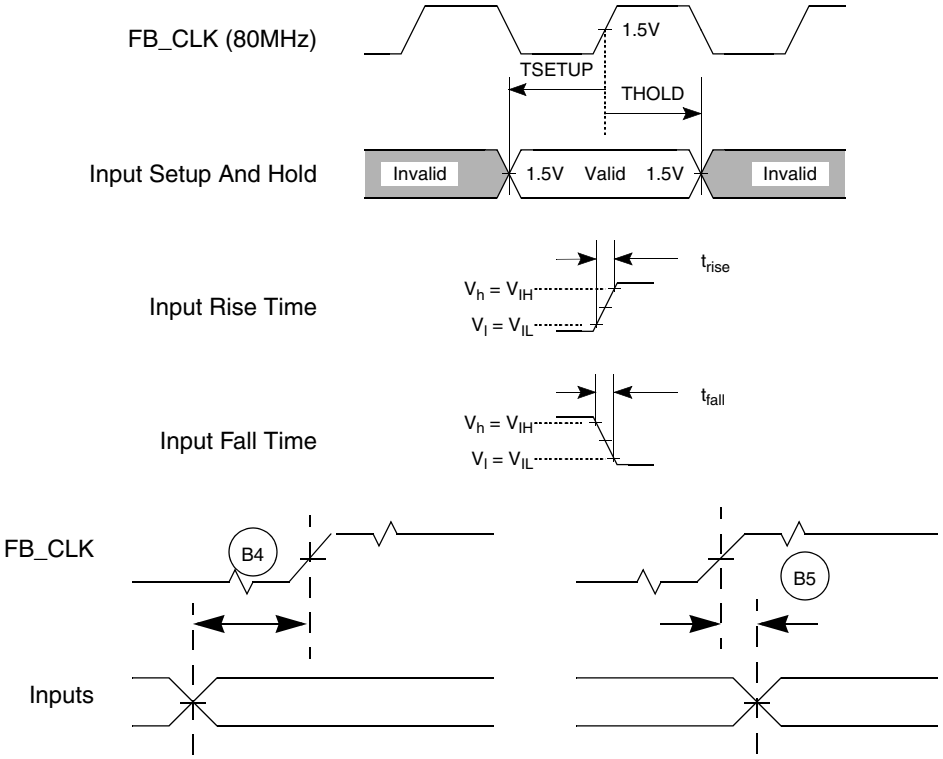

Figure 9. General Input Timing Requirements

5.7.1 FlexBus

A multi-function external bus interface called FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 80MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used. The FlexBus interface has six general purpose chip-selects ($\overline{\text{FB\_CS}}$[5:0]) which can be configured to be distributed between the FlexBus or SDRAM memory interfaces. Chip-select, $\overline{\text{FB\_CS0}}$ can be dedicated to boot ROM access and can be programmed to be byte (8 bits), word (16 bits), or longword (32 bits) wide. Control signal timing is compatible with common ROM/flash memories.

5.7.1.1 FlexBus AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the system clock.

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Table 10. FlexBus AC Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		—	80	Mhz	$f_{sys/3}$
FB1	Clock Period (FB_CLK)	t_{FBCK}	—	12.5	ns	t_{cyc}
FB2	Address, Data, and Control Output Valid (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0] and $\overline{OE}$)	$t_{FBCHDCV}$	—	7.0	ns	1
FB3	Address, Data, and Control Output Hold (A[23:0], D[31:0], $\overline{FB\_CS}$[5:0], R/$\overline{W}$, $\overline{TS}$, $\overline{BE/BWE}$[3:0], and $\overline{OE}$)	$t_{FBCHDCI}$	1	—	ns	1, 2
FB4	Data Input Setup	t_{DVFBCH}	3.5	—	ns	
FB5	Data Input Hold	t_{DIFBCH}	0	—	ns	
FB6	Transfer Acknowledge ($\overline{TA}$) Input Setup	t_{CVFBCH}	4	—	ns	
FB7	Transfer Acknowledge ($\overline{TA}$) Input Hold	t_{CIFBCH}	0	—	ns	
FB8	Address Output Valid (A[23:0])	t_{FBCHAV}	—	6.0	ns	3
FB9	Address Output Hold (A[23:0])	t_{FBCHAI}	1	—	ns	

NOTES:
1 Timing for chip selects only applies to the $\overline{FB\_CS}$[5:0] signals. Please see Section 5.8.2, "DDR SDRAM AC Timing Characteristics" for SD_CS[3:0] timing.
2 The FlexBus supports programming an extension of the address hold. Please consult the *MCF5329 Reference Manual* for more information.
3 These specs are used when the A[23:0] signals are configured as 23-bit, non-muxed FlexBus address signals.

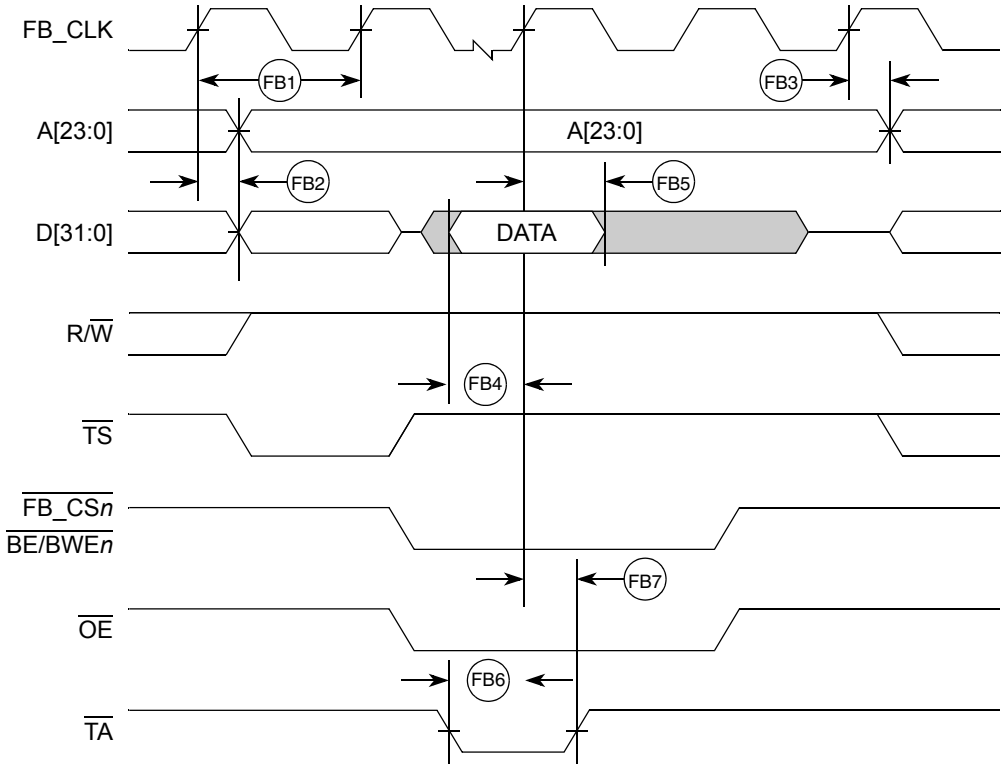

Figure 10. FlexBus Read Timing.

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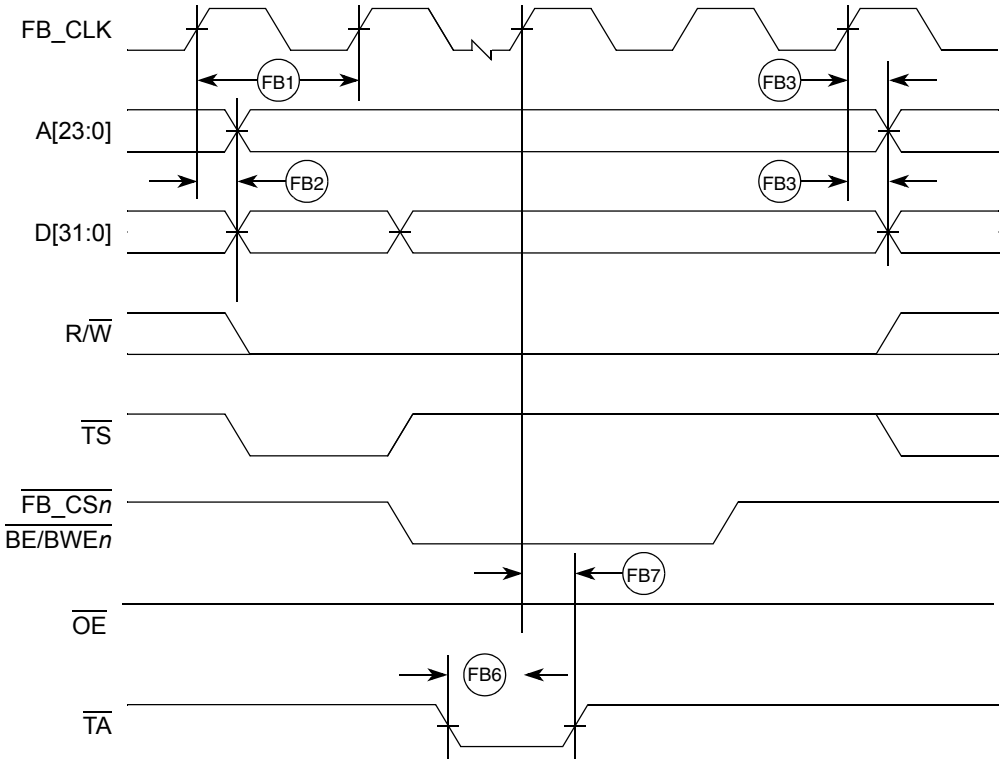

Figure 11. Flexbus Write Timing

5.8 SDRAM Bus

The SDRAM controller supports accesses to main SDRAM memory from any internal master. It supports either standard SDRAM or double data rate (DDR) SDRAM, but it does not support both at the same time.

5.8.1 SDR SDRAM AC Timing Characteristics

The following timing numbers indicate when data will be latched or driven onto the external bus, relative to the memory bus clock, when operating in SDR mode on write cycles and relative to SD_DQS on read cycles. The device's SDRAM controller is a DDR controller that has an SDR mode. Because it is designed to support DDR, a DQS pulse must still be supplied to device for each data beat of an SDR read. Te processor accomplishes this by asserting a signal named SD_DQS during read cycles. Care must be taken during board design to adhere to the following guidelines and specs with regard to the SDR_DQS signal and its usage.

Table 11. SDR Timing Specifications

Symbol	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation		TBD	80	Mhz	1
SD1	Clock Period	t_{SDCK}	12.5	TBD	ns	2
SD2	Clock Skew	t_{SDSK}	—	TBD		
SD3	Pulse Width High	t_{SDCKH}	0.45	0.55	SD_CLK	3

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Table 11. SDR Timing Specifications (continued)

Symbol	Characteristic	Symbol	Min	Max	Unit	Notes
SD4	Pulse Width Low	t_{SDCKH}	0.45	0.55	SD_CLK	4
SD5	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, SD_BA, SD_CS[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	
SD6	Address, SD_CKE, $\overline{SD\_CAS}$, $\overline{SD\_RAS}$, $\overline{SD\_WE}$, SD_BA, SD_CS[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
SD7	SD_SDR_DQS Output Valid	t_{DQSOV}	—	Self timed	ns	5
SD8	SD_DQS[3:0] input setup relative to SD_CLK	$t_{DQVSDCH}$	0.25 × SD_CLK	0.40 × SD_CLK	ns	6
SD9	SD_DQS[3:2] input hold relative to SD_CLK	$t_{DQISDCH}$	Does not apply. 0.5×SD_CLK fixed width.			7
SD10	Data (D[31:0]) Input Setup relative to SD_CLK (reference only)	t_{DVSDCH}	0.25 × SD_CLK	—	ns	8
SD11	Data Input Hold relative to SD_CLK (reference only)	t_{DISDCH}	1.0	—	ns	
SD12	Data (D[31:0]) and Data Mask(SD_DQM[3:0]) Output Valid	$t_{SDCHDMV}$	—	0.75 × SD_CLK + 0.5	ns	
SD13	Data (D[31:0]) and Data Mask (SD_DQM[3:0]) Output Hold	$t_{SDCHDMI}$	1.5	—	ns	

NOTES:
1. The device supports same frequency of operation for both FlexBus and SDRAM clock operates as that of the internal bus clock. Please see the PLL chapter of the *MCF5329 Reference Manual* for more information on setting the SDRAM clock rate.
2. SD_CLK is one SDRAM clock in (ns).
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Pulse width high plus pulse width low cannot exceed min and max clock period.
5. SD_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This is a guideline only. Subtle variation from this guideline is expected. SD_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
6. SDR_DQS is designed to pulse 0.25 clock before the rising edge of the memory clock. This spec is a guideline only. Subtle variation from this guideline is expected. SDR_DQS will only pulse during a read cycle and one pulse will occur for each data beat.
7. The SDR_DQS pulse is designed to be 0.5 clock in width. The timing of the rising edge is most important. The falling edge does not affect the memory controller.
8. Since a read cycle in SDR mode still uses the DQS circuit within the device, it is most critical that the data valid window be centered 1/4 clk after the rising edge of DQS. Ensuring that this happens will result in successful SDR reads. The input setup spec is just provided as guidance.

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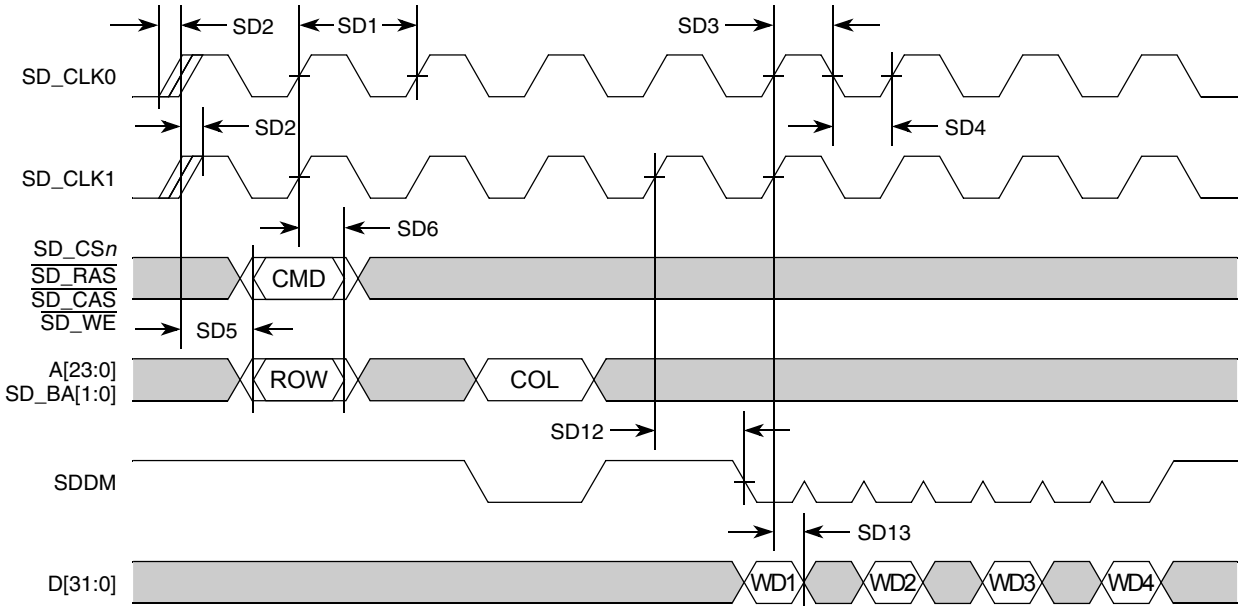

Figure 12. SDR Write Timing

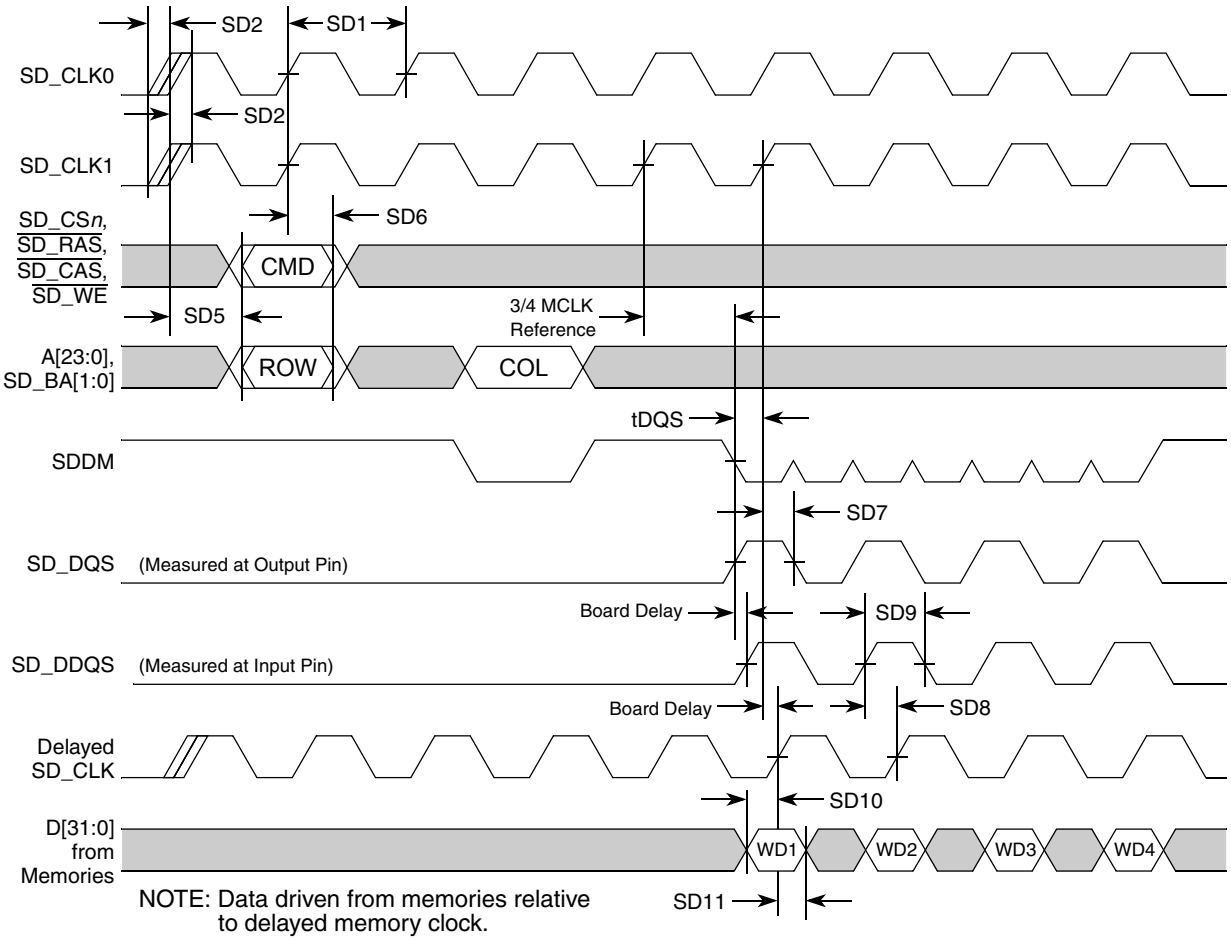

Figure 13. SDR Read Timing

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5.8.2 DDR SDRAM AC Timing Characteristics

When using the SDRAM controller in DDR mode, the following timing numbers must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the four DQS byte lanes. The following timing numbers are subject to change at anytime, and are only provided to aid in early board design. Please contact your local Freescale representative if questions develop.

Table 12. DDR Timing Specifications

Num	Characteristic	Symbol	Min	Max	Unit	Notes
	Frequency of Operation	t_{DDCK}	80	TBD	Mhz	1
DD1	Clock Period	t_{DDSK}	TBD	12.5	ns	2
DD2	Pulse Width High	t_{DDCKH}	0.45	0.55	SD_CLK	3
DD3	Pulse Width Low	t_{DDCKL}	0.45	0.55	SD_CLK	3
DD4	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Valid	$t_{SDCHACV}$	—	0.5 × SD_CLK + 1.0	ns	4
DD5	Address, SD_CKE, $\overline{\text{SD\_CAS}}$, $\overline{\text{SD\_RAS}}$, $\overline{\text{SD\_WE}}$, $\overline{\text{SD\_CS}}$[1:0] - Output Hold	$t_{SDCHACI}$	2.0	—	ns	
DD6	Write Command to first DQS Latching Transition	t_{CMDVDQ}	—	1.25	SD_CLK	
DD7	Data and Data Mask Output Setup (DQ-->DQS) Relative to DQS (DDR Write Mode)	t_{DQDMV}	1.5	—	ns	5 6
DD8	Data and Data Mask Output Hold (DQS-->DQ) Relative to DQS (DDR Write Mode)	t_{DQDMI}	1.0	—	ns	7
DD9	Input Data Skew Relative to DQS (Input Setup)	t_{DVDQ}	—	1	ns	8
DD10	Input Data Hold Relative to DQS.	t_{DIDQ}	0.25 × SD_CLK + 0.5ns	—	ns	9
DD11	DQS falling edge from SDCLK rising (output hold time)	$t_{DQLSDCH}$	0.5	—	ns	
DD12	DQS input read preamble width	t_{DQRPRE}	0.9	1.1	SD_CLK	
DD13	DQS input read postamble width	t_{DQRPST}	0.4	0.6	SD_CLK	
DD14	DQS output write preamble width	t_{DQWPRE}	0.25		SD_CLK	
DD15	DQS output write postamble width	t_{DQWPST}	0.4	0.6	SD_CLK	

NOTES:
1. The frequency of operation is either 2x or 4x the FB_CLK frequency of operation. FlexBus and SDRAM clock operate at the same frequency as the internal bus clock.
2. SD_CLK is one SDRAM clock in (ns).
3. Pulse width high plus pulse width low cannot exceed min and max clock period.
4. Command output valid should be 1/2 the memory bus clock (SD_CLK) plus some minor adjustments for process, temperature, and voltage variations.
5. This specification relates to the required input setup time of today's DDR memories. Rigoletto's output setup should be larger than the input setup of the DDR memories. If it is not larger, then the input setup on the memory will be in violation. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].
6. The first data beat will be valid before the first rising edge of DQS and after the DQS write preamble. The remaining data beats will be valid for each subsequent DQS edge.
7. This specification relates to the required hold time of today's DDR memories. MEM_DATA[31:24] is relative to MEM_DQS[3], MEM_DATA[23:16] is relative to MEM_DQS[2], MEM_DATA[15:8] is relative to MEM_DQS[1], and MEM_[7:0] is relative MEM_DQS[0].

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[8] Data input skew is derived from each DQS clock edge. It begins with a DQS transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

[9] Data input hold is derived from each DQS clock edge. It begins with a DQS transition and ends when the first data line becomes invalid.

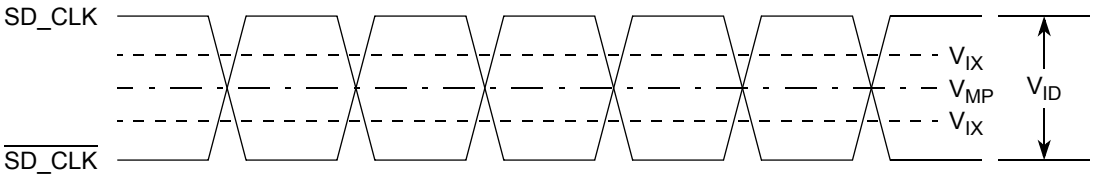

Figure 14. SD_CLK and $\overline{\text{SD\_CLK}}$ crossover timing

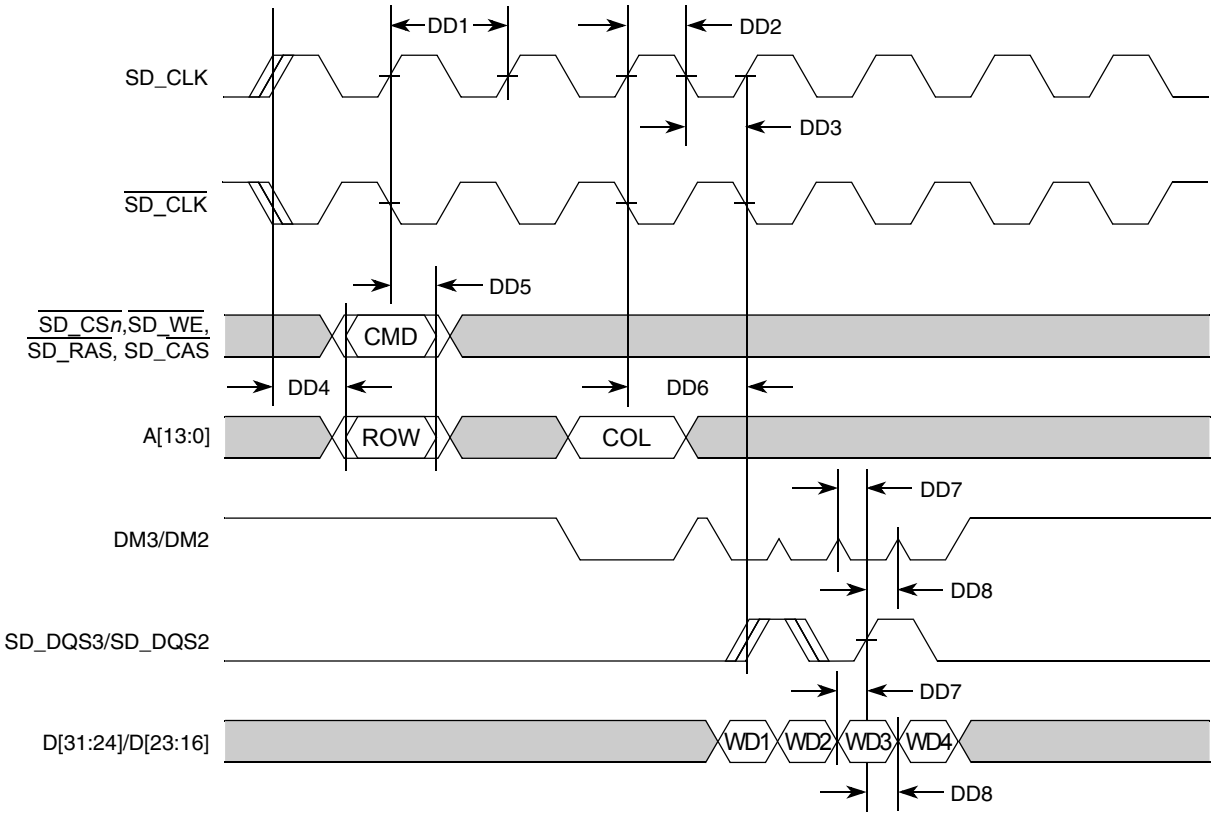

Figure 15. DDR Write Timing

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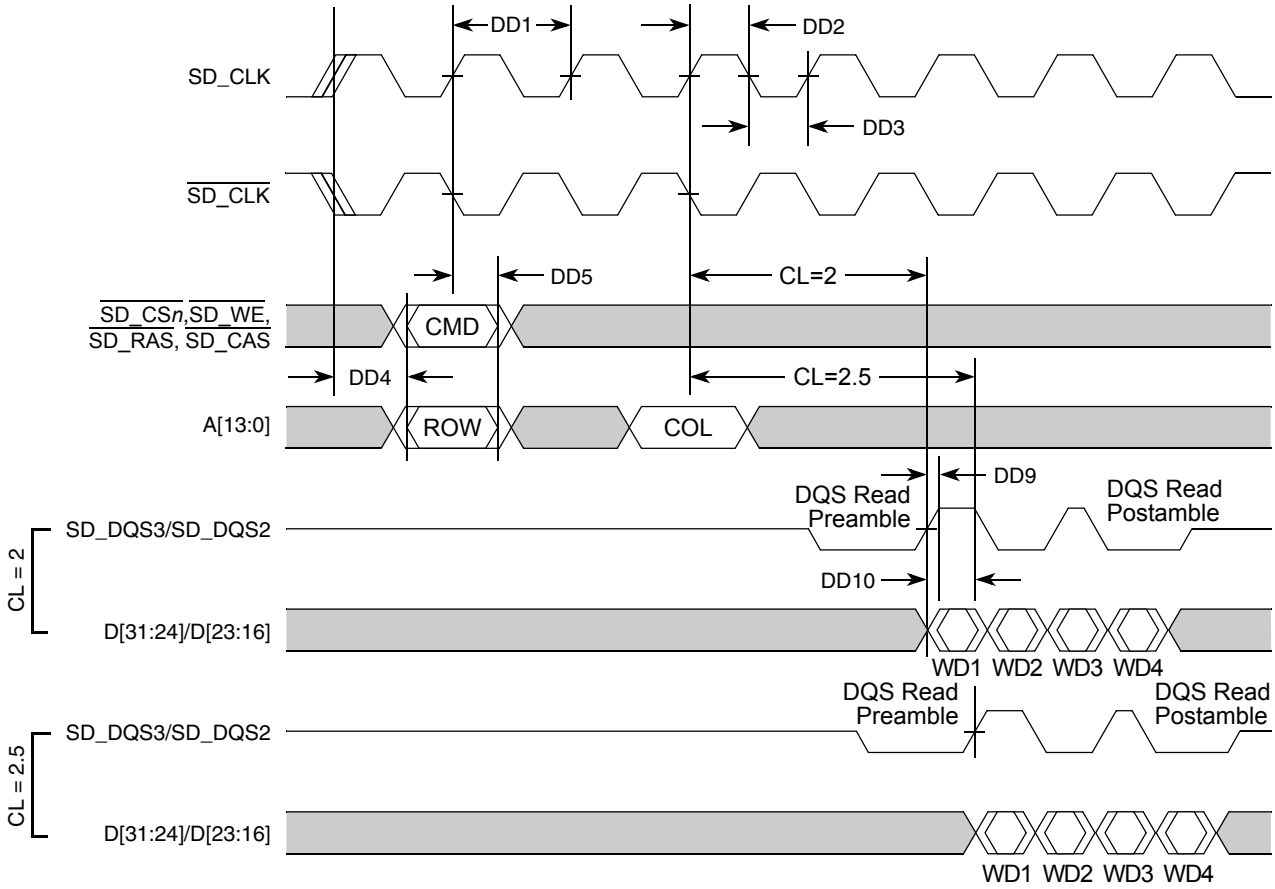

Figure 16. DDR Read Timing

5.9 General Purpose I/O Timing

Table 13. GPIO Timing[1]

Num	Characteristic	Symbol	Min	Max	Unit
G1	FB_CLK High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	FB_CLK High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to FB_CLK High	t_{PVCH}	9	—	ns
G4	FB_CLK High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

NOTES:
1 GPIO pins include: $\overline{IRQn}$, PWM, UART, FlexCAN, and Timer pins.

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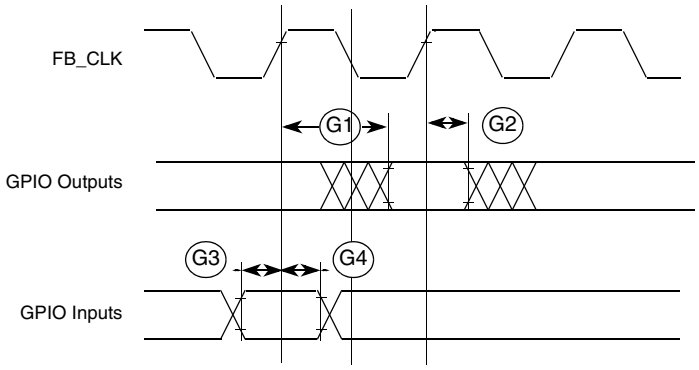

Figure 17. GPIO Timing

5.10 Reset and Configuration Override Timing

Table 14. Reset and Configuration Override Timing

Num	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to FB_CLK High	t_{RVCH}	9	—	ns
R2	FB_CLK High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RESET}}$ Input valid Time [1]	t_{RIVT}	5	—	t_{CYC}
R4	FB_CLK High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	—	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	—	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	—	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	—	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	—	1	t_{CYC}

NOTES:
1 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.

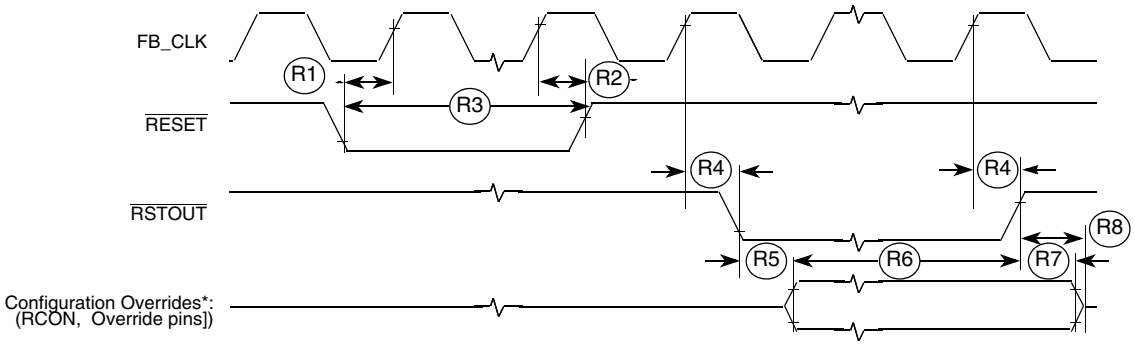

Figure 18. $\overline{\text{RESET}}$ and Configuration Override Timing

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NOTE

Refer to the CCM chapter of the *MCF5329 Reference Manual* for more information.

5.11 LCD Controller Timing Specifications

This sections lists the timing specifications for the LCD Controller.

Table 15. LCD_LSCLK Timing

Num	Parameter	Minimum	Maximum	Unit
T1	LCD_LSCLK Period	25	2000	ns
T2	Pixel data setup time	11	—	ns
T3	Pixel data up time	11	—	ns

Note: The pixel clock is equal to LCD_LSCLK / (PCD + 1). When it is in CSTN, TFT or monochrome mode with bus width = 1,LCD_LSCLK is equal to the pixel clock. When it is in monochrome with other bus width settings, LCD_LSCLK is equal to the pixel clock divided by bus width. The polarity of LCD_LSCLK and LCD_LD signals can also be programmed.

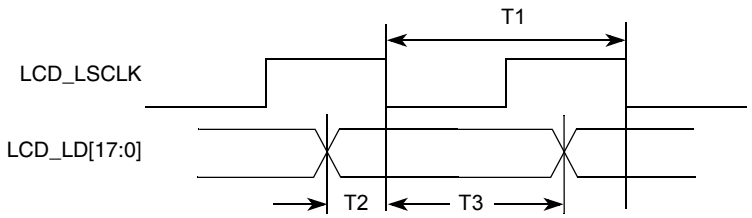

Figure 19. LCD_LSCLK to LCD_LD[17:0] timing diagram

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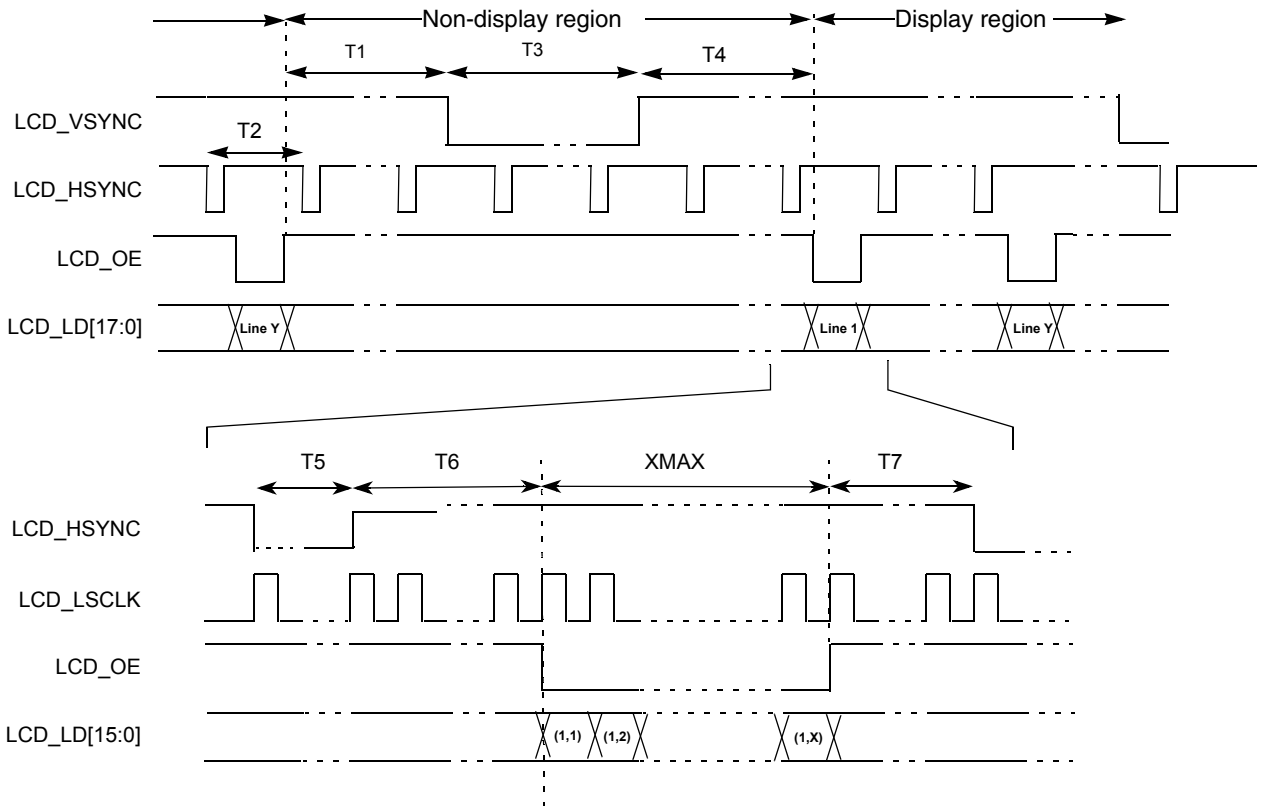

Figure 20. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Table 16. 4/8/12/16/18 Bit/Pixel TFT Color Mode Panel Timing

Number	Description	Minimum	Value	Unit
T1	End of LCD_OE to beginning of LCD_VSYNC	T5+T6+T7-1	(VWAIT1·T2)+T5+T6+T7-1	Ts
T2	LCD_HSYNC period	—	XMAX+T5+T6+T7	Ts
T3	LCD_VSYNC pulse width	T2	VWIDTH·T2	Ts
T4	End of LCD_VSYNC to beginning of LCD_OE	1	(VWAIT2·T2)+1	Ts
T5	LCD_HSYNC pulse width	1	HWIDTH+1	Ts
T6	End of LCD_HSYNC to beginning to LCD_OE	3	HWAIT2+3	Ts
T7	End of LCD_OE to beginning of LCD_HSYNC	1	HWAIT1+1	Ts

Note: Ts is the LCD_LSCLK period. LCD_VSYNC, LCD_HSYNC and LCD_OE can be programmed as active high or active low. In Figure 20, all 3 signals are active low. LCD_LSCLK can be programmed to be deactivated during the LCD_VSYNC pulse or the LCD_OE deasserted period. In Figure 20, LCD_LSCLK is always active.

Note: XMAX is defined in number of pixels in one line.

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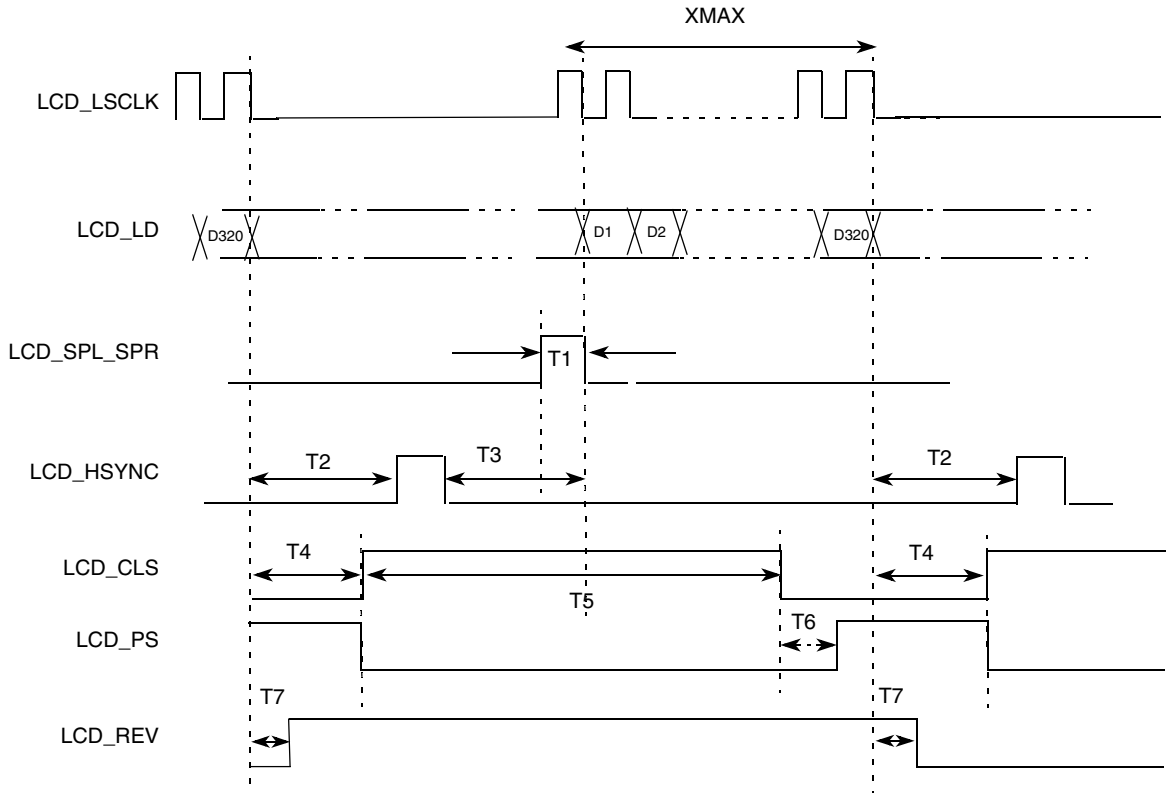

Figure 21. Sharp TFT Panel Timing

Table 17. Sharp TFT Panel Timing

Num	Description	Minimum	Value	Unit
T1	LCD_SPL/LCD_SPR pulse width	—	1	Ts
T2	End of LCD_LD of line to beginning of LCD_HSYNC	1	HWAIT1+1	Ts
T3	End of LCD_HSYNC to beginning of LCD_LD of line	4	HWAIT2 + 4	Ts
T4	LCD_CLS rise delay from end of LCD_LD of line	3	CLS_RISE_DELAY+1	Ts
T5	LCD_CLS pulse width	1	CLS_HI_WIDTH+1	Ts
T6	LCD_PS rise delay from LCD_CLS negation	0	PS_RISE_DELAY	Ts
T7	LCD_REV toggle delay from last LCD_LD of line	1	REV_TOGGLE_DELAY+1	Ts

Note: Falling of LCD_SPL/LCD_SPR aligns with first LCD_LD of line.
Note: Falling of LCD_PS aligns with rising edge of LCD_CLS.
Note: LCD_REV toggles in every LCD_HSYN period.

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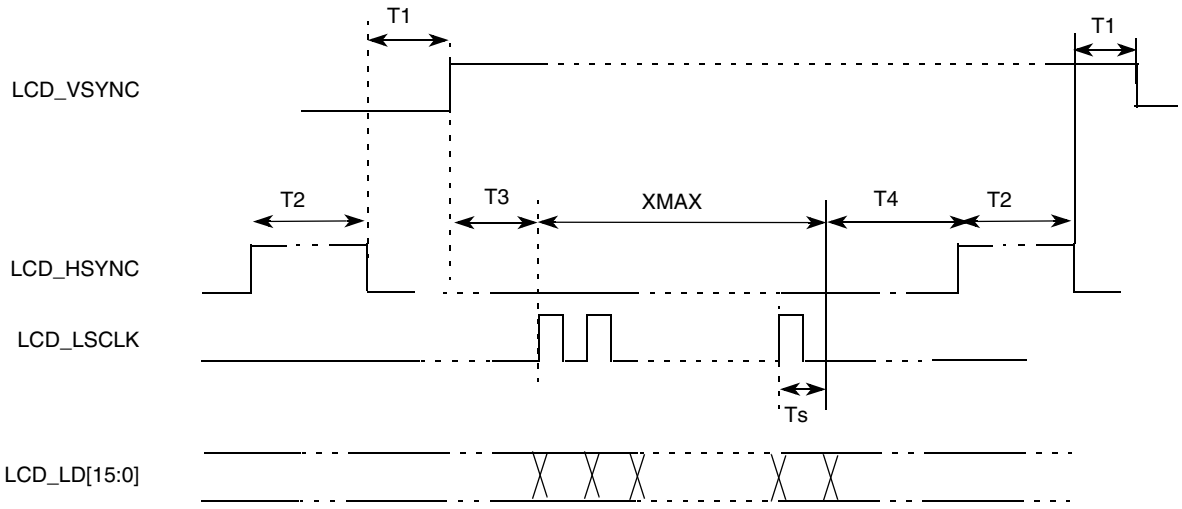

Figure 22. Non-TFT Mode Panel Timing

Table 18. Non-TFT Mode Panel Timing

Num	Description	Minimum	Value	Unit
T1	LCD_HSYNC to LCD_VSYNC delay	2	HWAIT2 + 2	Tpix
T2	LCD_HSYNC pulse width	1	HWIDTH + 1	Tpix
T3	LCD_VSYNC to LCD_LSCLK	—	0 ≤ T3 ≤ Ts	—
T4	LCD_LSCLK to LCD_HSYNC	1	HWAIT1 + 1	Tpix

Note: Ts is the LCD_LSCLK period while Tpix is the pixel clock period. LCD_VSYNC, LCD_HSYNC and LCD_LSCLK can be programmed as active high or active low. In Figure 22, all these 3 signals are active high. When it is in CSTN mode or monochrome mode with bus width = 1, T3 = Tpix = Ts. When it is in monochrome mode with bus width = 2, 4 and 8, T3 = 1, 2 and 4 Tpix respectively.

5.12 USB On-The-Go

The MCF5329 device is compliant with industry standard USB 2.0 specification.

5.13 ULPI Timing Specification

Control and data timing requirements for the ULPI pins are given in Table 19. These timings apply in synchronous mode only. All timings are measured with either a 60 MHz input clock from the USB_CLKIN pin or a 60MHz output clock at the ULPI_CLK pin. Both clocks need to maintain a 50% duty cycle. Control signals and 8-bit data are always clocked on the rising edge, while the optional double-edge 4-bit data signals are clocked on rising and falling edges.

The ULPI interface on the MCF5329 processor is compliant with the industry standard definition.

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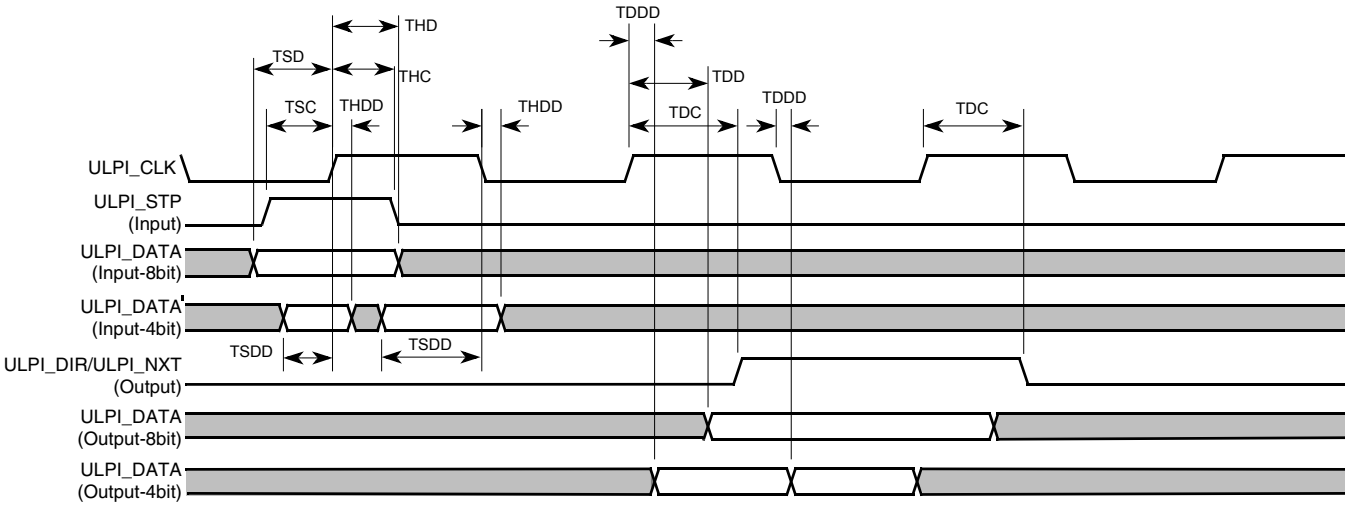

Figure 23. ULPI Timing Diagram

Table 19. ULPI Interface Timing

Parameter	Symbol	Min	Max	Units
Timing with reference to ULPI_CLK				
Setup time (control in, 8-bit data in)	TSC, TSD	—	6.0	ns
Setup time (control in, 8-bit data in)	THC, THD	0.0	—	ns
Output delay (control out, 8-bit data out)	TDC, TDD	—	9.0	ns
Timing with reference to USB_CLKIN				
Setup time (control in, 8-bit data in)	TSC, TSD	—	3.0	ns
Hold time (control in, 8-bit data in)	THC, THD	-1.5	—	ns
Output delay (control out, 8-bit data out)	TDC, TDD	—	6.0	ns

5.14 SSI Timing Specifications

The following figure and table lists the specifications for the SSI module.

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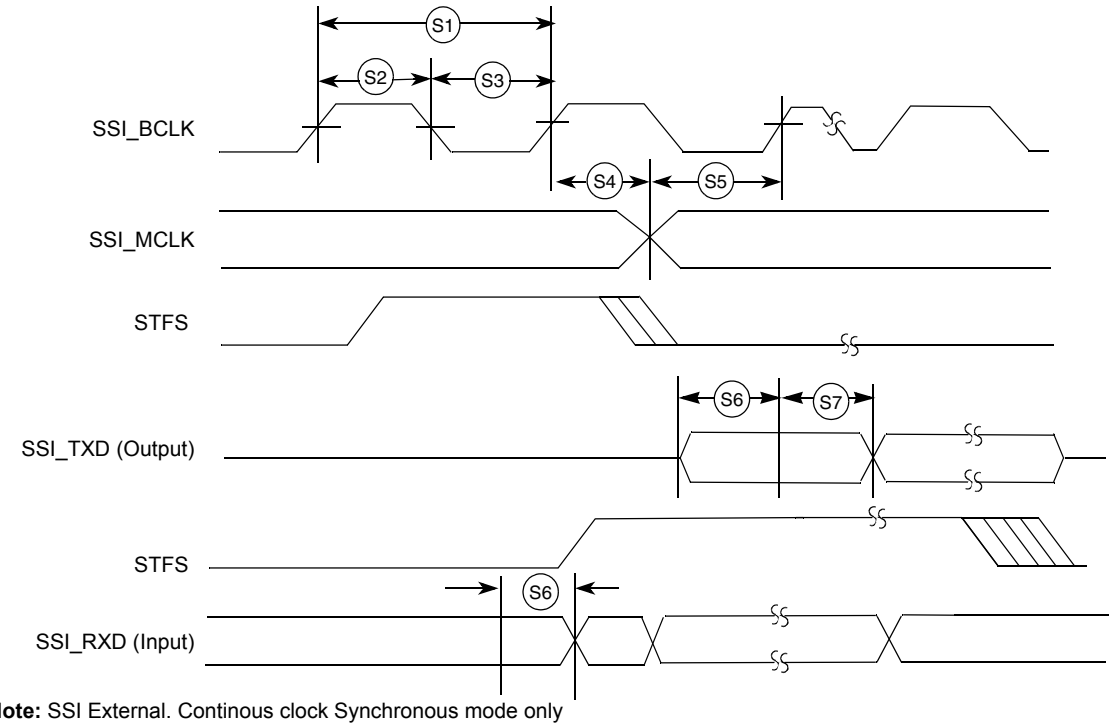

Note: SSI External. Continous clock Synchronous mode only

Figure 24. SSI External Continous Clock Timing Diagram

Table 20. SSI Timing

Num	Description	1.8 +/- 0.10V		Unit
		Minimum	Maximum	
S1	SSI_BCLK clock period	$1/(64f_s)$[1]	49	ns
S2	SSI_BCK high-level time	35	—	ns
S3	SSI_BCK low-level time	35	—	ns
S4	SSI_BCK rising edge to SSI_MCLK edge	10	—	ns
S5	SSI_MCLK edge to SSI_BCLK rising edge	10	—	ns
S6	SSI_TXD/SSI_RXD data set-up time	10	—	ns
S7	SSI_TXD/SSI_RXD data hold time	10	—	ns

NOTES:
[1] f_s is the sampling frequency. SSI_BCLK can be operated upto 512 times the sampling frequency to a max frequency of 49.152MHz

5.15 I²C Input/Output Timing Specifications

Table 21 lists specifications for the I²C input timing parameters shown in Figure 25.

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Table 21. I^2C Input Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2	—	t_{cyc}
I2	Clock low period	8	—	t_{cyc}
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	ms
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	ms
I6	Clock high time	4	—	t_{cyc}
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2	—	t_{cyc}
I9	Stop condition setup time	2	—	t_{cyc}

Table 22 lists specifications for the I^2C output timing parameters shown in Figure 25.

Table 22. I^2C Output Timing Specifications between SCL and SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6	—	t_{cyc}
I2 [1]	Clock low period	10	—	t_{cyc}
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µs
I4 [1]	Data hold time	7	—	t_{cyc}
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10	—	t_{cyc}
I7 [1]	Data setup time	2	—	t_{cyc}
I8 [1]	Start condition setup time (for repeated start condition only)	20	—	t_{cyc}
I9 [1]	Stop condition setup time	10	—	t_{cyc}

NOTES:
1. Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 22. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 22 are minimum values.
2. Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 50-pF load.

Figure 25 shows timing for the values in Table 22 and Table 21.

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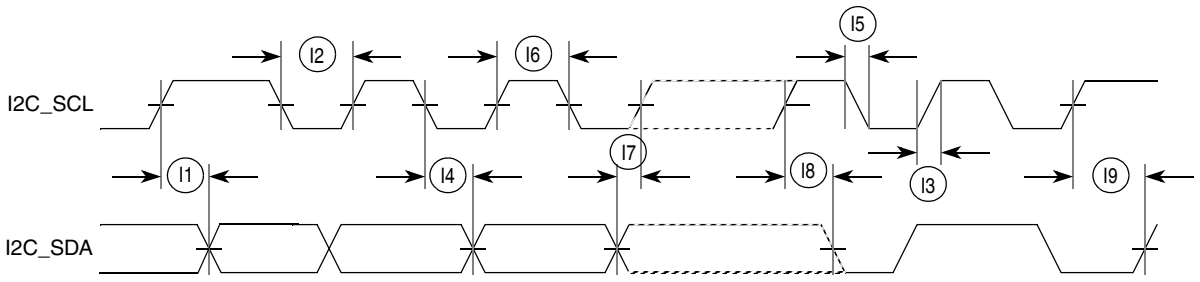

Figure 25. I²C Input/Output Timings

5.16 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

5.16.1 MII Receive Signal Timing (FEC_RXD[3:0], FEC_RXDV, FEC_RXER, and FEC_RXCLK)

The receiver functions correctly up to a FEC_RXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_RXCLK frequency.

Table 23 lists MII receive channel timings.

Table 23. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RXDV, FEC_RXER to FEC_RXCLK setup	5	—	ns
M2	FEC_RXCLK to FEC_RXD[3:0], FEC_RXDV, FEC_RXER hold	5	—	ns
M3	FEC_RXCLK pulse width high	35%	65%	FEC_RXCLK period
M4	FEC_RXCLK pulse width low	35%	65%	FEC_RXCLK period

Figure 26 shows MII receive signal timings listed in Table 23.

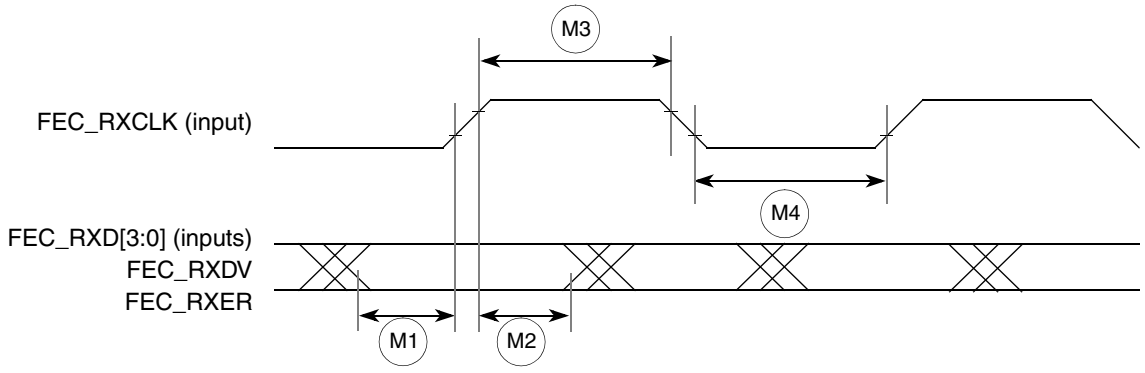

Figure 26. MII Receive Signal Timing Diagram

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5.16.2 MII Transmit Signal Timing (FEC_TXD[3:0], FEC_TXEN, FEC_TXER, FEC_TXCLK)

Table 24 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC_TXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TXCLK frequency.

The transmit outputs (FEC_TXD[3:0], FEC_TXEN, FEC_TXER) can be programmed to transition from either the rising or falling edge of FEC_TXCLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 24. MII Transmit Signal Timing

Num	Characteristic	Min	Max	Unit
M5	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER invalid	5	—	ns
M6	FEC_TXCLK to FEC_TXD[3:0], FEC_TXEN, FEC_TXER valid	—	25	ns
M7	FEC_TXCLK pulse width high	35%	65%	FEC_TXCLK period
M8	FEC_TXCLK pulse width low	35%	65%	FEC_TXCLK period

Figure 27 shows MII transmit signal timings listed in Table 24.

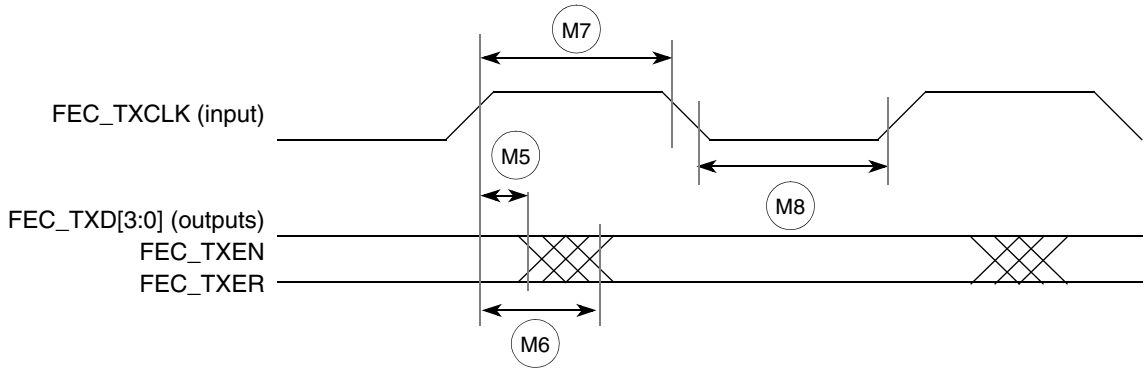

Figure 27. MII Transmit Signal Timing Diagram

5.16.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 25 lists MII asynchronous inputs signal timing.

Table 25. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9	FEC_CRS, FEC_COL minimum pulse width	1.5	—	FEC_TXCLK period

Figure 28 shows MII asynchronous input timings listed in Table 25.

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Figure 28. MII Async Inputs Timing Diagram

5.16.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 26 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 26. MII Serial Management Channel Timing

Num	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max prop delay)	—	25	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	10	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

Figure 29 shows MII serial management channel timings listed in Table 26.

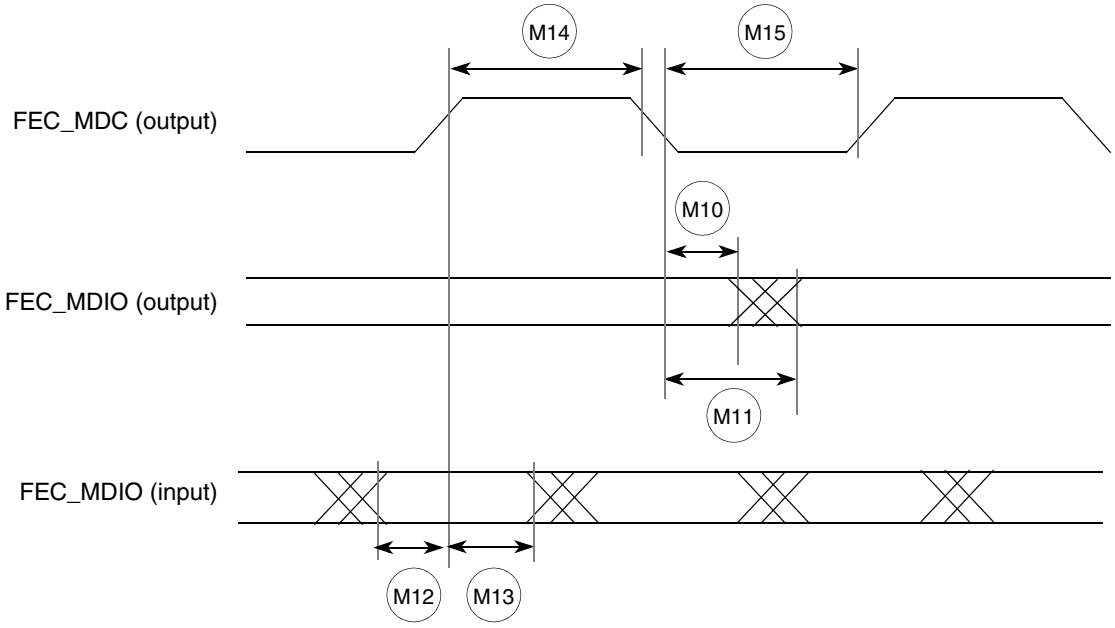

Figure 29. MII Serial Management Channel Timing Diagram

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5.17 32-Bit Timer Module Timing Specifications

Table 27 lists timer module AC timings.

Table 27. Timer Module AC Timing Specifications

Name	Characteristic			Unit
		Min	Max	
T1	DT0IN / DT1IN / DT2IN / DT3IN cycle time	3	—	t_{CYC}
T2	DT0IN / DT1IN / DT2IN / DT3IN pulse width	1	—	t_{CYC}

5.18 QSPI Electrical Specifications

Table 28 lists QSPI timings.

Table 28. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid. (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 28 correspond to Figure 30.

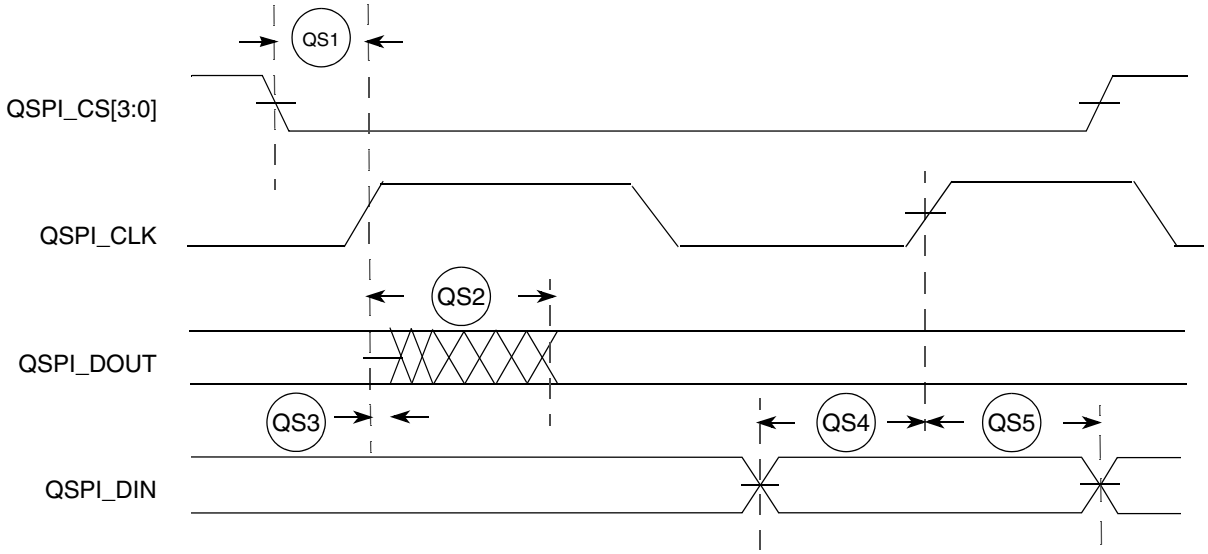

Figure 30. QSPI Timing

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5.19 JTAG and Boundary Scan Timing

Table 29. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/3}$
J2	TCLK Cycle Period	t_{JCYC}	4	—	t_{CYC}
J3	TCLK Clock Pulse Width	t_{JCW}	26	—	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	—	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	—	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	—	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	—	ns

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, specific timing is not associated with it.

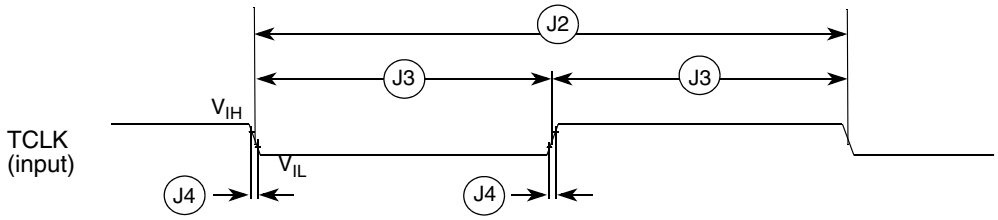

Figure 31. Test Clock Input Timing

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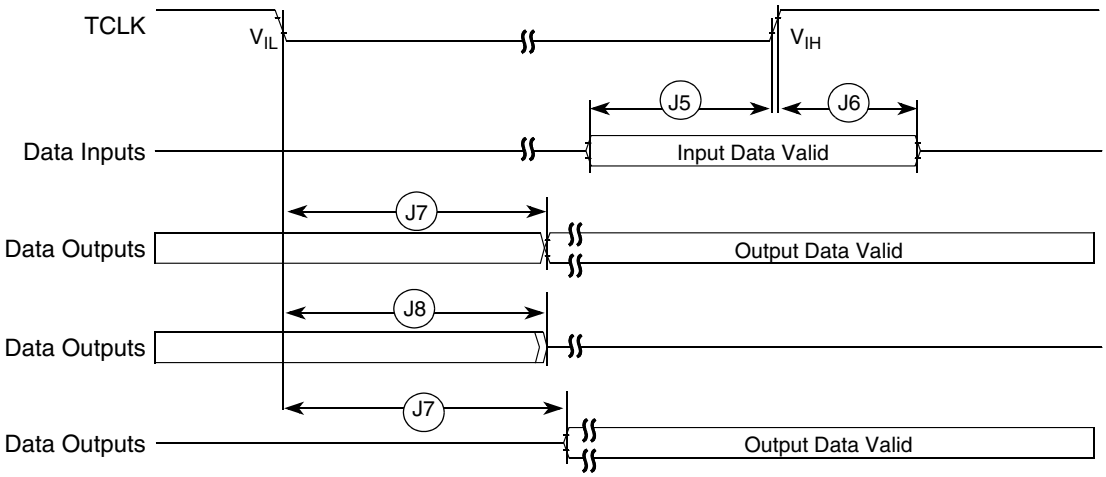

Figure 32. Boundary Scan (JTAG) Timing

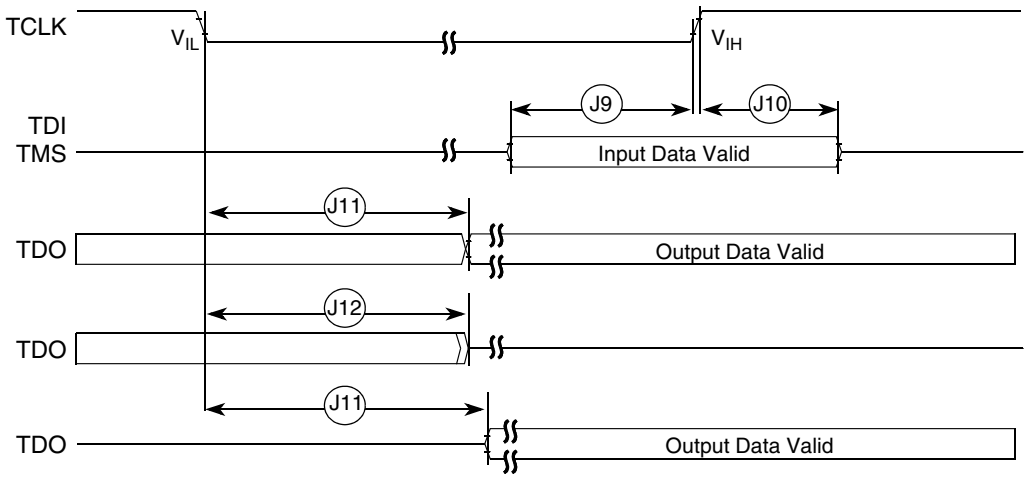

Figure 33. Test Access Port Timing

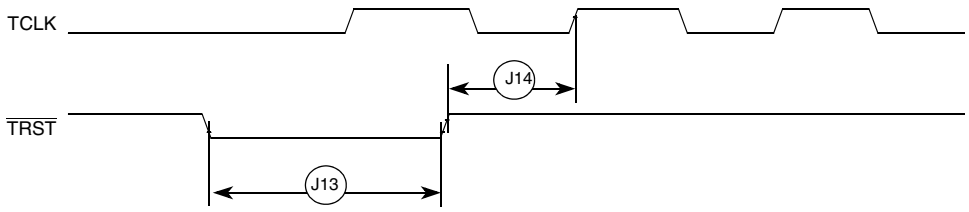

Figure 34. $\overline{\text{TRST}}$ Timing

5.20 Debug AC Timing Specifications

Table 30 lists specifications for the debug AC timing parameters shown in Figure 36.

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Table 30. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
DE0	PSTCLK cycle time	—	0.3	t_{cyc}
DE1	PST valid to PSTCLK high	4	—	ns
DE2	PSTCLK high to PST invalid	1.5	—	ns
DE3	DSCLK cycle time	5	—	t_{cyc}
DE4	DSI valid to DSCLK high	1	—	t_{cyc}
DE5[1]	DSCLK high to DSO invalid	4	—	t_{cyc}
DE6	$\overline{\text{BKPT}}$ input data setup time to FB_CLK high	4	—	ns
DE7	FB_CLK high to $\overline{\text{BKPT}}$ invalid	0	—	ns

NOTES:
1 DSCLK and DSI are synchronized internally. DE4 is measured from the synchronized DSCLK input relative to the rising edge of FB_CLK.

Figure 35 shows real-time trace timing for the values in Table 30.

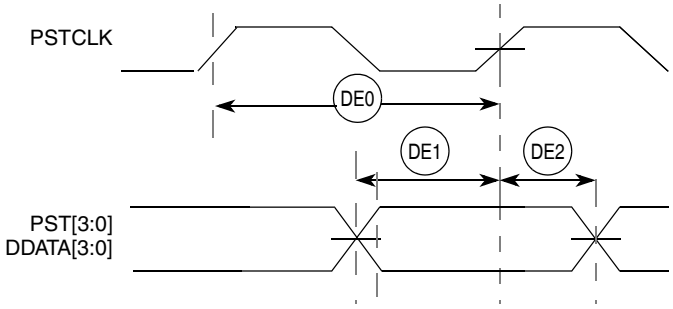

Figure 35. Real-Time Trace AC Timing

Figure 36 shows BDM serial port AC timing and $\overline{\text{BKPT}}$ pin timing for the values in Table 30.

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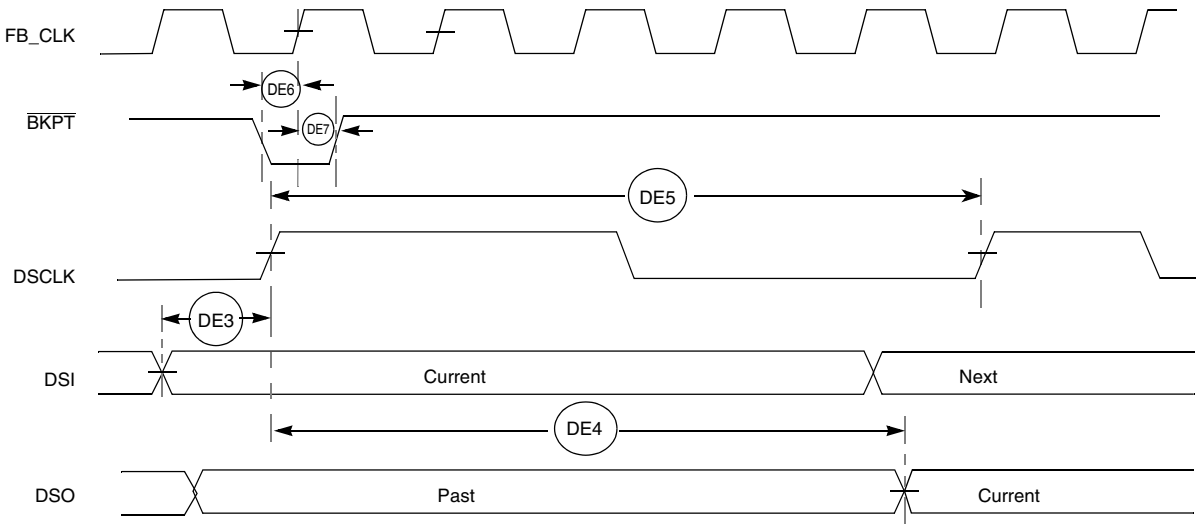

Figure 36. BDM Serial Port AC Timing

6 Revision History

Table 31. MCF5329DS Document Revision History

Rev. No.	Substantive Changes	Date of Release
0	• Initial release.	11/2005
0.1	• Added not to Section 4, “Mechanicals and Pinouts.” • Added “top view” and “bottom view” where appropriate in mechanical drawings and pinout figures. • Figure 9: Corrected “FB_CLK (75MHz)” label to “FB_CLK (80MHz)”	3/2006

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