## □ MN102H730F , MN102H73G , MN102H73K

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Туре	MN102H730F	MN102H73G (under development)	MN102H73K (under development)			
ROM (×8-bit)	External	128 K	256 K			
RAM (×8-bit)	10 K	10 K	12 K			
Package	TQFP128-P-1414B *Lead-free	TQFP128	B-P-1414A *Lead-free			
Minimum Instruction Execution Time	With main clock operated58 ns (at 3.0 V to 3.6 V, 34 MHz)					
Interrupts	<ul> <li>RST pin • Watchdog • NMI pin • Timer counter 0 to 9 underflow • Timer counter 10 to 14 underflow</li> <li>Timer counter 10 to 14 compare capture A • Timer counter 10 to 14 compare capture B</li> <li>ATC ch.0 to 1 transfer finish • ETC ch.0 to 1 transfer finish</li> <li>External 0 to 7 • Serial ch.0 to 4 transmission • Serial ch.0 to 4 reception • A/D conversion finish</li> </ul>					
Timer Counter	Timer counter 0 : 8-bit × 1 Clock source					
	Timer counter 1 : 8-bit × 1 Clock source					
	Timer counter 2 : 8-bit × 1 Clock source					
						Timer counter 4 : 8-bit × 1 Clock source
	Timer counter 5 : 8-bit × 1 Clock source		underflow of timer counter 9; TM5IO pin			
	Timer counter 6 : 8-bit × 1 Clock source					
	Timer counter 7 : 8-bit × 1 Clock source	1/2 of system clock (BOSC) frequency; t timer counter 6 output	underflow of timer counter 9; TM7IO pin			
		Timer counter 8 : 8-bit × 1 Clock source	underflow of timer counter 7 1/2 of system clock (BOSC) frequency; s 1/4 of system clock (XI) frequency; TM8			
		underflow of timer counter 8	-			

### MN102H730F , MN102H73G , MN102H73K $\Box$

Timer Counter (Continu	e) Timer counter 9 : 8-bit × 1				
	Clock source				
	Interrupt source underflow of timer counter 9				
	Timer counter 10 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM10IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM10IOA pin/TM10IOB pin (1 ×, 4 ×)				
	Interrupt source underflow of timer counter 10; timer counter 10 compare capture A; timer counter 10 compare capture B				
	Timer counter 11 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM11IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM11IOA pin/TM11IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 11; timer counter 11 compare capture A;				
	timer counter 11 compare capture B				
	Timer counter 12 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM12IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM12IOA pin/TM12IOB pin (1 ×, 4 ×)				
	Interrupt source underflow of timer counter 12; timer counter 12 compare capture A; timer counter 12 compare capture B				
	Timer counter 13 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM13IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM13IOA pin/TM13IOB pin (1 ×, 4 ×)				
	Interrupt source underflow of timer counter 13; timer counter 13 compare capture A; timer counter 13 compare capture B				
	Timer counter 14 : 16-bit × 1 (timer output, event count, input capture, PWM output, 2-phase encoder input) Clock source underflow of timer counter 8, 9; TM14IOB pin; 1/2 of system clock (BOSC) frequency; 2-phase encode of TM14IOA pin/TM14IOB pin (1 ×, 4 ×) Interrupt source underflow of timer counter 14; timer counter 14 compare capture A; timer counter 14 compare capture A;				
Serial Interface	timer counter 14 compare capture B Serial 0, 1 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source				
	Serial 2, 3 : 8-bit × 1 (transfer direction of MSB / LSB selectable, transmission / reception of 7, 8-bit length) Clock source				
	UART $\times$ 4 (common use with serial 0 to 3)				
	$I^2C \times 2$ (common use with serial 1,3; single master)				
Multiply-and-Accumulate	16-bit sign $\times$ 16-bit sign $+$ 40-bit sign				
I/O Pins I/O	104       • Common use : 59 (use of full address, address data separate 16-bit mode)         • Common use : 76 (use of address 16-bit, address data separate 8-bit mode)				
A/D Inputs	$10\text{-bit} \times 12\text{-ch.}$ (with S/H)				
D/A Outputs	8-bit × 4-ch.				
PWM	16-bit × 5-ch. (timer counter 10 to 14)				
ICR	16-bit $\times$ 5-ch. (timer counter 10 to 14)				
	16-bit × 5-ch. (timer counter 10 to 14)				
OCR	16-bit $\times$ 5-ch. (timer counter 10 to 14)				

See the next page for electrical characteristics, pin assignment and support tool.

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#### **Electrical Characteristics**

#### Supply current

Parameter	Symbol	Condition		Limit		
				typ	max	Unit
Operating supply current	IDDess	VI = VDD or VSS, output open	(0.10-*		mA	
	IDDopr	f = 34  MHz, VDD = 3.3  V		60+10α*		
Supply current at STOP	IDDS	Pin with pull-up resistor is open	70		70	
	IDDS	all other input pins and Hi-Z state input/output		/0	μΑ	
Supply current at HALT	IDDII	pins are simultaneously applied VDD or VSS level f = 34 MHz , VDD = 3.3 V, output open		20, 10 at	mA	
	IDDH			50+10α*		

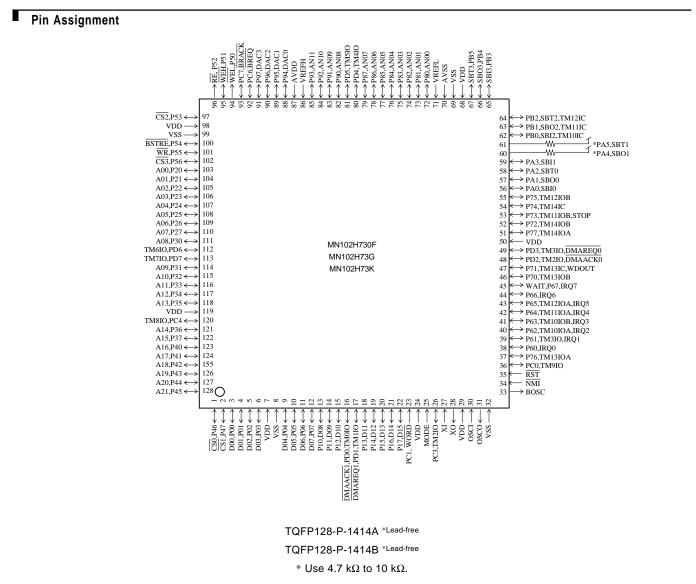
 $(Ta = -40^{\circ}C \text{ to } +85^{\circ}C \text{ , } VDD = AVDD = 3.3 \text{ V} \text{ , } VSS = AVSS = 0 \text{ V})$ 

 $\ast$  "  $\alpha$  " depends on products .

MN102H73G/73K/730F  $\alpha=0$ 

MN102HF73G  $\alpha = 1$ 

MN102HF73K  $\alpha = 2$ 



#### Support Tool

In-circuit Emulator	PX-ICE102H73-128P1414		
Flash Memory Built-in Type	Туре	MN102HF73G, MN102HF73K	
	ROM (× 8-bit)	128 K / 256 K	
	RAM (× 8-bit)	10 K / 12 K	
	Minimum instruction execution time	58 ns (at 3.0 V to 3.6 V, 34 MHz)	
	Package	TQFP128-P-1414B *Lead-free	

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