## $\square$ MN101E33G, MN101E33K

| Type | MN101E33G | MN101E33K | MN101EF33N |
| :---: | :---: | :---: | :---: |
| Internal ROM type | Mask ROM |  | FLASH |
| ROM (byte) | 128K | 256K | 512K |
| RAM (byte) | 6K | 12K | 30K |
| Package (Lead-free) | QFP100-P-1818B (Under planning) | QFP100-P-1818B (Under development) |  |
| Minimum Instruction Execution Time | $\begin{gathered} 0.05 \mu \mathrm{~s} \text { (at } 3.0 \mathrm{~V} \text { to } 3.6 \mathrm{~V}, 20 \mathrm{MHz} \text { at internal } 2,4,8 \text { times oscillation) } \\ 0.0588 \mu \mathrm{~s}(\text { at } 2.7 \mathrm{~V} \text { to } 3.6 \mathrm{~V}, 17 \mathrm{MHz}) \\ 30.6 \mu \mathrm{~s} \text { (at } 2.7 \mathrm{~V} \text { to } 3.6 \mathrm{~V}, 32.768 \mathrm{kHz} \text { ) } \\ \hline \end{gathered}$ |  | $0.05 \mu \mathrm{~s}$ (at 3.0 V to $3.6 \mathrm{~V}, 20 \mathrm{MHz}$ ) |

## Interrupts

RESET, Watchdog, External 0 to 5, Timer 0 to 3, Timer 6, Timer 7 (2 systems), Timer A to E, Time base, Serial 0 (2 systems), Serial
1 (2 systems), Serial 2, Serial 3 ( 2 systems), Serial 4 ( 2 systems), Automatic transfer finish ( 2 systems), A/D conversion finish, Key
interrupts, IEBus*

* IEBus is a trademark of NEC Electronics Corporation.


## Timer Counter

Timer counter 0 : 8-bit $\times 1$
(square-wave/8-bit PWM output, event count, simple pulse width measurement, real time output control)
Clock source............... $1 / 2,1 / 4$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 32,1 / 64$ of OSC oscillation clock frequency; $1 / 1$ of
XI oscillation clock frequency; external clock input
Interrupt source ........... coincidence with compare register 0

## Timer counter 1 : 8 -bit $\times 1$

(square-wave output, event count, synchronous output event, 16-bit timer with casscade connection (Timer 0 and connection), serial clocke output)
Clock source. $\qquad$ $1 / 2,1 / 8$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 64,1 / 128$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source $\qquad$ coincidence with compare register 1

Timer counter 0, 1 can be cascade-connected.
Timer counter 2 : 8-bit $\times 1$
(square-wave/8-bit PWM output, event count, synchronous output event, pulse width measurement, real time output control, serial baud rate timer)
Clock source. $\qquad$ $1 / 2,1 / 4$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 32,1 / 64$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source $\qquad$ coincidence with compare register 2

Timer counter 0, 1, 2 can be cascade-connected.
Timer counter 3 : 8 -bit $\times 1$ (square-wave output, event count, serial baud rate timer)
Clock source $\qquad$ $1 / 2,1 / 8$ of system clock frequency; $1 / 1,1 / 4,1 / 16,1 / 64,1 / 128$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency; external clock input
Interrupt source $\qquad$ coincidence with compare register 3

Timer counter 2, 3 can be cascade-connected.
Timer counter 0, 1, 2, 3 can be cascade-connected.
Timer counter 6 : 8-bit freerun timer, time base timer
Clock source. $\qquad$ 1/1 of system clock frequency; $1 / 1,1 / 4096,1 / 8192$ of OSC oscillation clock frequency; $1 / 1,1 / 4096$, 1/8192 of XI oscillation clock frequency
Interrupt generating cycle.... $1 / 128,1 / 256,1 / 512,1 / 1024,1 / 81921 / 32768$ of OSC oscillation clock frequency; $1 / 128,1 / 256,1 / 512$, $1 / 1024,1 / 8192,1 / 32768$ of XI oscillation clock frequency
Interrupt source $\qquad$ coincidence with compare register 6

## Timer counter 7 : 16-bit $\times 1$

(square-wave/16-bit PWM output, cycle / duty continuous variable, event count, synchronous output evevt, pulse width measurement, input capture)

Clock source.................
$1 / 1,1 / 2,1 / 4,1 / 16$ of system clock frequency; $1 / 1,1 / 2,1 / 4,1 / 16$ of OSC oscillation clock frequency; $1 / 1$, $1 / 2,1 / 4,1 / 16$ of external clock input frequency
Interrupt source ........... coincidence with compare register 7 (2 lines)
Timer counter A, B, C, D, E : 8-bit $\times 5$
Clock source............... 1/2, 1/4 of system clock frequency; $1 / 1,1 / 2,1 / 4,1 / 8,1 / 16.1 / 32$ of OSC oscillation clock frequency
Interrupt source $\qquad$ coincidence with compare register $\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D}, \mathrm{E}$

Time base timer (one-minute count setting)
Clock source $\qquad$ $1 / 1$ of OSC oscillation clock frequency; $1 / 1$ of XI oscillation clock frequency
Interrupt source $\qquad$ $1 / 128,1 / 256,1 / 512,1 / 1024,1 / 8192,1 / 32768$ of clock source frequency

Watchdog timer
Interrupt source $\qquad$ $1 / 65536,1 / 262144,1 / 1048576,1 / 4194304$ of system clock frequency

## Serial interface

Serial 0 : synchronous type/UART (full-duplex) $\times 1$
Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, A ; 1 / 2,1 / 4,1 / 16,1 / 64$ of OSC oscillation clock frequency

Serial 1 : synchronous type/UART (full-duplex) $\times 1$
Clock source $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $3, \mathrm{~B} ; 1 / 2,1 / 4,1 / 8,1 / 16,1 / 64$ of OSC oscillation clock frequency

Serial 2 : synchronous type/single-master $\mathrm{I}^{2} \mathrm{C} \times 1$
Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $3, C ; 1 / 2,1 / 4,1 / 16,1 / 32$ of OSC oscillation clock frequency

Serial 3 : synchronous type/ $I^{2} \mathrm{C} \times 1$
Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, D ; 1 / 2,1 / 4,1 / 16,1 / 32$ of OSC oscillation clock frequency

Serial 4 : synchronous type/UART (full-duplex) $\times 1$
Clock source $\qquad$ $1 / 2,1 / 4$ of system clock frequency; pulse output of timer counter $2, E ; 1 / 2,1 / 4,1 / 16,1 / 64$ of OSC oscillation clock frequency

## - IEBus Interface

Serial 0 : asynchronous
Clock source $\quad 1 / 2,1 / 3$ of system clock frequency
DMA controller
Nomber of channels : 2
Max. Transfer cycles : 255
Starting factor : external request, various types of interrupt, software
Transfer mode : 1-byte transfer, word transfer, burst transfer

- I/O Pins

| $\mathrm{I} / \mathrm{O}$ | 22 | (5 V IF port) Common use, Specified pull-up resistor available, Input/output selectable (bit unit) |
| :--- | :---: | :---: |
|  | 62 | (3 V IF port) Common use, Specified pull-up resistor available, Input/output selectable (bit unit) |
|  | 1 | (3 V IF port) Common use |

## A/D converter

10-bit $\times 8$-ch. (with S/H)

## Special Ports

Buzzer output, high-current drive port

## ROM Correction

Correcting address designation : up to 7 addresses possible

## Development tools

In-circuit Emulator (under development)

## Pin Assignment



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