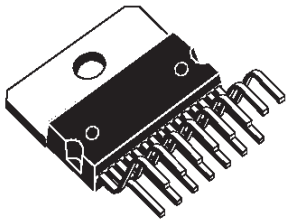
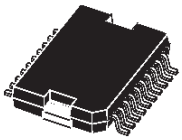
LNBP10 SERIES
LNBP20

LNB SUPPLY AND CONTROL VOLTAGE REGULATOR (PARALLEL INTERFACE)

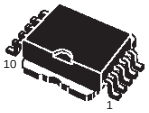
- COMPLETE INTERFACE FOR TWO LNBs REMOTE SUPPLY AND CONTROL
- LNB SELECTION AND STAND-BY FUNCTION
- BUILT-IN TONE OSCILLATOR FACTORY TRIMMED AT 22KHz
- FAST OSCILLATOR START-UP FACILITATES DiSEqC™ ENCODING
- TWO SUPPLY INPUTS FOR LOWEST DISSIPATION
- BYPASS FUNCTION FOR SLAVE OPERATION
- LNB SHORT CIRCUIT PROTECTION AND DIAGNOSTIC
- AUXILIARY MODULATION INPUT EXTENDS FLEXIBILITY
- CABLE LENGTH COMPENSATION
- INTERNAL OVER TEMPERATURE PROTECTION
- BACKWARD CURRENT PROTECTION



Multiwatt-15



PowerSo-20



PowerSO-10

DESCRIPTION

Intended for analog and digital satellite receivers, the LNBP is a monolithic linear voltage regulator, assembled in Multiwatt-15, PowerSO-20 and PowerSO-10, specifically designed to provide the powering voltages and the interfacing signals to the LNB downconverter situated in the antenna via the coaxial cable. Since most satellite receivers have two antenna ports, the output voltage of the regulator is available at one of two logic-selectable output pins (LNBA, LNBB). When the IC is powered and put in Stand-by (EN pin LOW), both regulator outputs are disabled to allow the antenna downconverters to be supplied/controlled by others satellite receivers sharing the same coaxial lines. In this occurrence the device will limit at 3 mA (max) the backward current that could flow from LNBA and LNBB output pins to GND.

For slave operation in single dish, dual receiver systems, the bypass function is implemented by an electronic switch between the Master Input pin (MI) and the LNBA pin, thus leaving all LNB powering and control functions to the Master Receiver. This electronic switch is closed when the device is powered and EN pin is LOW.

The regulator outputs can be logic controlled to be 13 or 18 V (typ.) by mean of the VSEL pin for remote controlling of LNBs. Additionally, it is possible to increment by 1V (typ.) the selected voltage value to compensate the excess voltage drop along the coaxial cable (LLC pin HIGH).

In order to reduce the power dissipation of the device when the lowest output voltage is selected, the regulator has two Supply Input pins V_{CC1} and V_{CC2}. They must be powered respectively at 16V (min) and 23V (min), and an internal switch automatically will select the suitable supply pin according to the selected output voltage. If adequate heatsink is provided and higher power losses are acceptable, both supply pins can be powered by the same 23V source without affecting any other circuit performance.

The ENT (Tone Enable) pin activates the internal oscillator so that the DC output is modulated by a ±0.3 V, 22KHz (typ.) square wave. This internal oscillator is factory trimmed within a tolerance of ±2KHz, thus no further adjustments neither external components are required.

A burst coding of the 22KHz tone can be

accomplished thanks to the fast response of the ENT input and the prompt oscillator start-up. This helps designers who want to implement the DiSEqC™ protocols (*).

In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is available (EXTM). An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. When external modulation is not used, the relevant pin can be left open.

Two pins are dedicated to the overcurrent protection/monitoring: CEXT and OLF. The overcurrent protection circuit works dynamically: as soon as an overload is detected in either LNB output, the output is shut-down for a time Toff determined by the capacitor connected between CEXT and GND. Simultaneously the OLF pin, that is an open collector diagnostic output flag, from HIGH IMPEDANCE state goes LOW. After the time has elapsed, the output is resumed for a time $t_{on}=1/15t_{off}$ (typ.) and OLF goes in HIGH IMPEDANCE. If the overload is still present, the protection circuit will cycle again through t_{off} and t_{on} until the overload is removed. Typical $t_{on}+t_{off}$ value is 1200ms when a 4.7µF external capacitor is used.

This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up even with highly capacitive loads on LNB outputs.

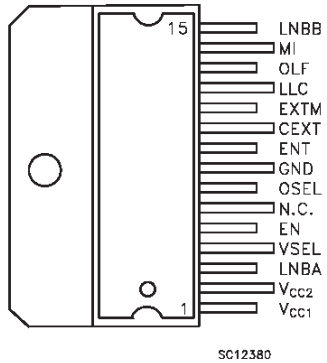
The device is packaged in Multiwatt15 for thru-holes mounting and in PowerSO-20 for surface mounting. When a limited functionality in a smaller package matches design needs, a range of cost-effective PowerSO-10 solutions is also offered. All versions have built-in thermal protection against overheating damage.

(*): External components are needed to comply to level 2.x and above (bidirectional) DiSEqC™ bus hardware requirements. DiSEqC™ is a trademark of EUTELSAT.

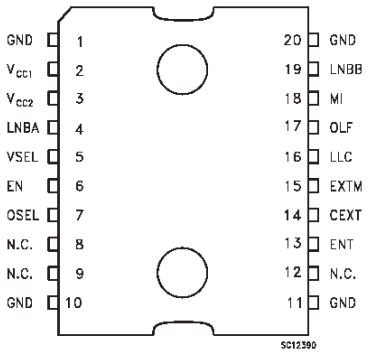
ORDERING NUMBERS

Type	Multiwatt-15	PowerSO-20	PowerSO-10
LNBP10			LNBP10SP
LNBP11			LNBP11SP
LNBP12			LNBP12SP
LNBP13			LNBP13SP
LNBP14			LNBP14SP
LNBP15			LNBP15SP
LNBP16			LNBP16SP
LNBP20	LNBP20CR	LNBP20PD	

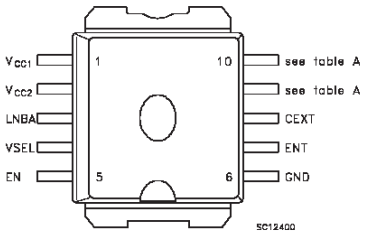
PIN CONFIGURATIONS



Multiwatt-15



PowerSO-20



PowerSO-10

TABLE A: PIN CONFIGURATIONS

SYMBOL	NAME	FUNCTION	PIN NUMBER vs SALES TYPE (LNBP)								
			20CR	20PD	10SP	11SP	12SP	13SP	14SP	15SP	16SP
V_{CC1}	Supply Input 1	15V to 25V supply. It is automatically selected when V_{OUT} = 13 or 14V	1	2	1	1	1	1	1	1	1
V_{CC2}	Supply Input 2	22V to 25V supply. It is automatically selected when V_{OUT} = 18 or 19V	2	3	2	2	2	2	2	2	2
LNBA	Output Port	See truth tables for voltage and port selection. In stand-by mode this port is powered by the MI pin via the internal Bypass Switch	3	4	3	3	3	3	3	3	3
VSEL	Output Voltage Selection: 13 or 18V (typ)	Logic control input: See truth table	4	5	4	4	4	4	4	4	4
EN	Port Enable	Logic control input: See truth table	5	6	5	5	5	5	5	5	5
OSEL	Port Selection	Logic control input: See truth table	7	7	9	NA	NA	NA	NA	NA	NA
GND	Ground	Circuit Ground. It is internally connected to the die frame	8	1 10 11 20	6	6	6	6	6	6	6
ENT	22 KHz Tone Enable	Logic control input: See truth table	9	13	7	7	7	7	7	7	7
CEXT	External Capacitor	Timing capacitor used by the Dynamic Overload Protection. Typical application is 4.7 µF for a 1200 ms cycle	10	14	8	8	8	8	8	8	8
EXTM	External Modulation	External Modulation Input. Needs DC decoupling to the AC source. If not used, can be left open.	11	15	NA	NA	NA	9	NA	9	9
LLC	Line Length Compens. (1V typ)	Logic control input: See truth table	12	16	NA	NA	9	NA	9	NA	10
OLF	Over Load Flag	Logic output (open Collector). Normally in HIGH IMPEDANCE, goes LOW when current or thermal overload occurs.	13	17	NA	9	NA	NA	10	10	NA
MI	Master Input	In stand-by mode, the voltage on MI is routed to LNBA pin. Can be left open if bypass function is not needed	14	18	NA	10	10	10	NA	NA	NA
LNBB	Output Port	See truth tables for voltage and port selection.	15	19	10	NA	NA	NA	NA	NA	NA

NOTE: The limited pin availability of the PowerSO-10 package leads to drop some functions.

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (VCC1, VCC2, MI)	28	V
I_o	Output Current (LNBA, LNBB)	Internally limited	
V_i	Logic Input Voltage (ENT, EN, OSEL, VSEL, LLC)	-0.5 to 7	V
I_{SW}	Bypass Switch Current	900	mA
P_{tot}	Power Dissipation at $T_{case} < 85^oC$	14	W
T_{stg}	Storage Temperature Range	- 40 to 150	^oC
T_{op}	Operating Junction Temperature Range	- 40 to 125	^oC

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	2	$^oC/W$

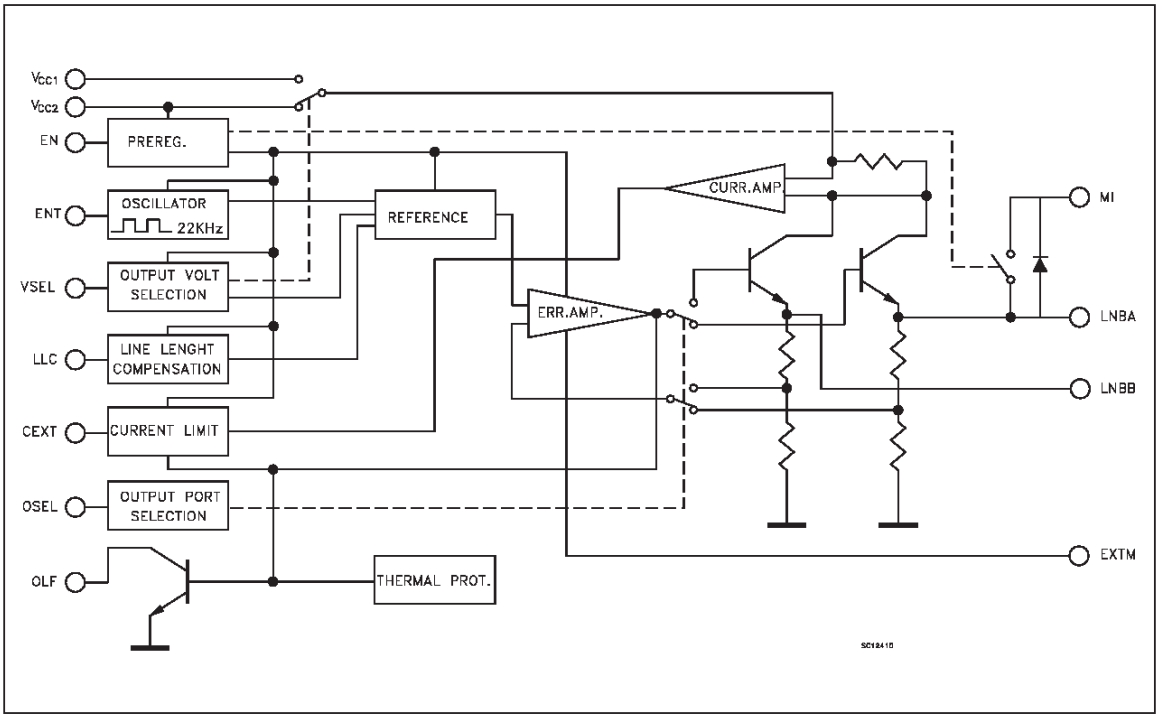
LOGIC CONTROLS TRUTH TABLES

Control I/O	Pin Name	L	H
OUT	OLF	$I_{OUT} > I_{OMAX}$ or $T_j > 150^oC$	$I_{OUT} < I_{OMAX}$
IN	ENT	22KHz tone OFF	22KHz tone ON
IN	EN	See table below	See table below
IN	OSEL	See table below	See table below
IN	VSEL	See table below	See table below
IN	LLC	See table below	See table below

EN	OSEL	VSEL	LLCP	V_{LNBA}	V_{LNBB}
L	X	X	X	V_{MI} -0.4V (typ.)	Disabled
H	L	L	L	13V (typ.)	Disabled
H	L	H	L	18V (typ.)	Disabled
H	L	L	H	14V (typ.)	Disabled
H	L	H	H	19V (typ.)	Disabled
H	H	L	L	Disabled	13V (typ.)
H	H	H	L	Disabled	18V (typ.)
H	H	L	H	Disabled	14V (typ.)
H	H	H	H	Disabled	19V (typ.)

NOTE: All logic input pins have internal pull-down resistor (typ. = 250KΩ)

BLOCK DIAGRAM

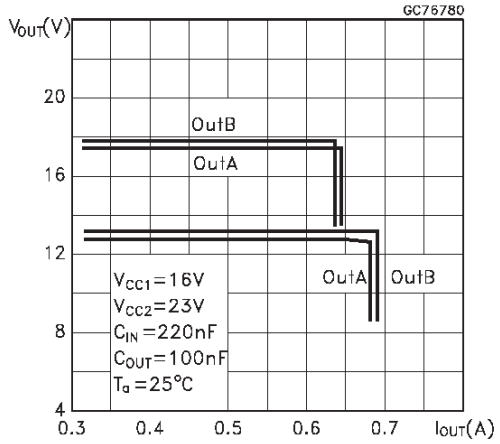


ELECTRICAL CHARACTERISTICS FOR LNBP SERIES (T_j = 0 to 85 °C, C_i = 0.22 µF, C_o = 0.1 µF, EN=H, ENT=L, LLC= L, V_{IN1} = 16V, V_{IN2} = 23V, I_{OUT} = 50mA, (unless otherwise specified)

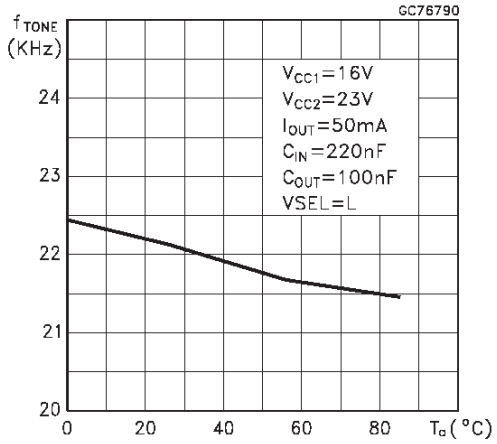
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN1}	V_{CC1} Supply Voltage	I_O = 500mA, ENT=H, VSEL=L, LLC=L I_O = 500mA, ENT=H, VSEL=L, LLC=H	15 16		25 25	V V
V_{IN2}	V_{CC2} Supply Voltage	I_O = 500mA, ENT=VSEL=H, LLC=L I_O = 500mA, ENT=VSEL=H, LLC=H	22 23		25 25	V V
V_{O1}	Output Voltage	I_O = 500 mA, VSEL=H, LLC=L I_O = 500 mA, VSEL=H, LLC=H	17.3	18 19	18.7	V V
V_{O2}	Output Voltage	I_O = 500 mA, VSEL=L, LLC=L I_O = 500 mA, VSEL=L, LLC=H	12.5	13 14	13.5	V V
ΔV_O	Line Regulation	V_{IN1} = 15 to 18 V, V_{OUT} = 13 V V_{IN2} = 22 to 25 V, V_{OUT} = 18 V		4 4	40 40	mV mV
ΔV_O	Load Regulation	V_{IN1} = V_{IN2} = 22 V, V_{OUT} = 13 or 18V, I_O = 50 to 500 mA		80	180	mV
SVR	Supply Voltage Rejection	V_{IN1} = V_{IN2} = 23 ± 0.5V_{ac}, f_{ac} = 50 KHz		45		dB
I_{MAX}	Output Current Limiting		500	650	800	mA
t_{OFF}	Dynamic Overload Protection OFF Time	Output shorted, C_{EXT} = 4.7µF		1100		ms
t_{ON}	Dynamic Overload Protection ON Time	Output shorted, C_{EXT} = 4.7µF		t_{OFF}/15		ms
F_{TONE}	Tone Frequency	ENT=H	20	22	24	KHz
A_{TONE}	Tone Amplitude	ENT=H	0.4	0.6	0.8	Vpp
D_{TONE}	Tone Duty Cucle	ENT=H	40	50	60	%
t_r, t_f	Tone Rise or Fall Time	ENT=H	5	10	15	µs
G_{EXTM}	External Modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 40KHz		5		
V_{EXTM}	External Modulation Input Voltage	AC Coupling			400	mV_{pp}
Z_{EXTM}	External Modulation Impedance	f = 10Hz to 40KHz		400		Ω
V_{SW}	Bypass Switch Voltage Drop (MI to LNBA)	EN=L, I_{SW}= 300mA, V_{CC2}-V_{MI} = 4V		0.35	0.6	V
V_{OL}	Overload Flag Pin Logic Low	I_{OL} = 8mA		0.28	0.5	V
I_{OZ}	Overload Flag Pin OFF State Leakage Current	V_{OH} = 6V			10	µA
V_{IL}	Control Input Pin Logic Low				0.8	V
V_{IH}	Control Input Pin Logic High		2.5			V
I_{IH}	Control Pins Input Current	V_{IH} = 5V		20		µA
I_{CC}	Supply Current	Outputs Disabled (EN=L)		0.3	1	mA
I_{CC}	Supply Current	ENT=H, I_{OUT} = 500 mA		3.1	6	mA
I_{OBK}	Output Backward Current	EN=L, V_{LNBA} = V_{LNBB} = 18V V_{IN1} = V_{IN2} = 22V or floating		0.2	3	mA
T_{SHDN}	Thermal Shutdown Threshold			150		°C

TYPICAL PERFORMANCE CHARACTERISTICS (unless otherwise specified T_j=25°C)

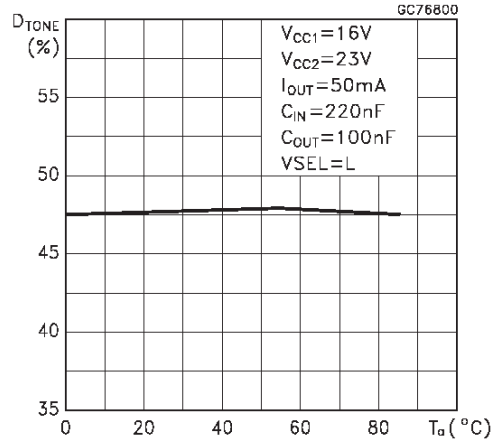
Output Voltage vs Output Current



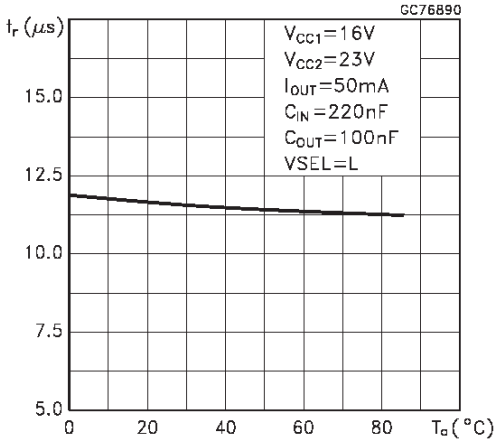
Tone Frequency vs Temperature



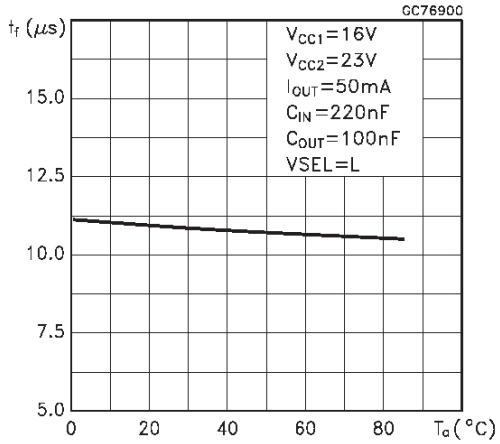
Tone Duty Cycle vs Temperature



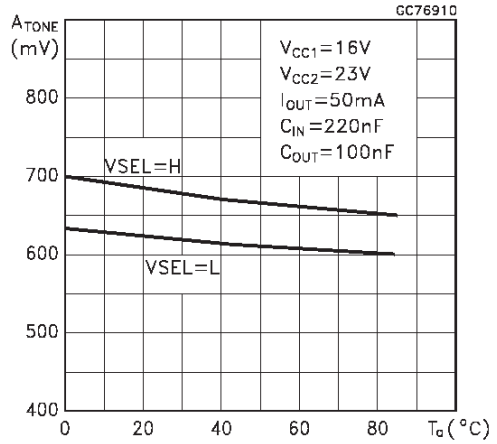
Tone Rise Time vs Temperature



Tone Fall Time vs Temperature

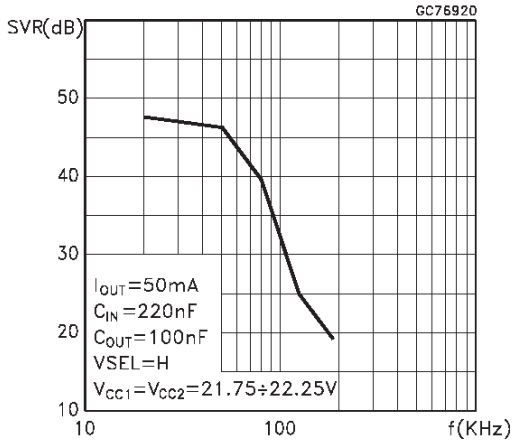


Tone Amplitude vs Temperature

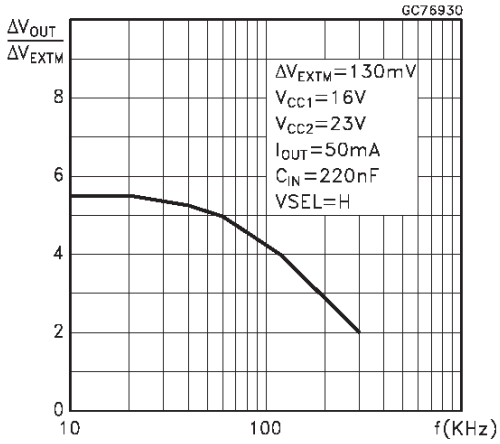


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

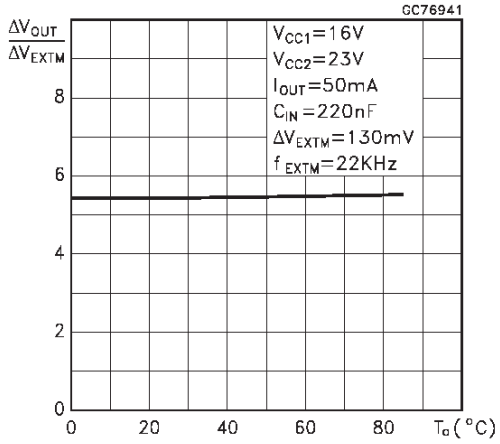
S.V.R. vs Frequency



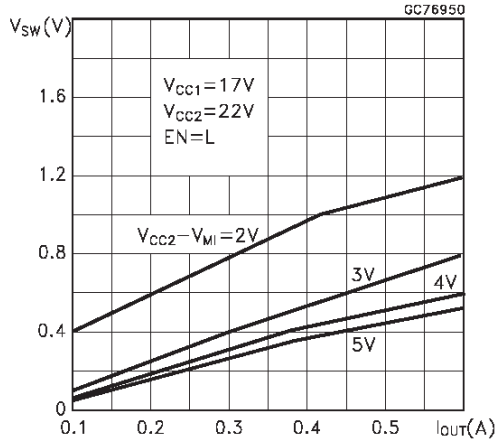
LNBA External Modulation Gain vs Frequency



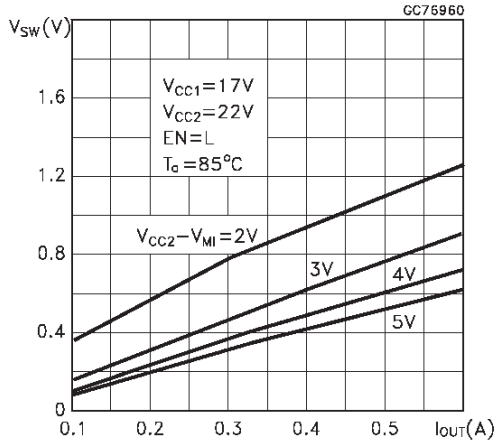
External Modulation vs Temperature



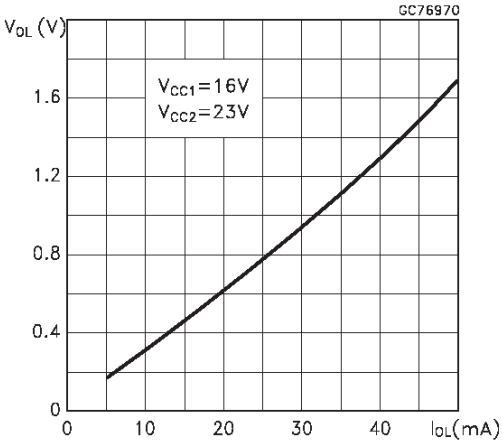
Bypass Switch Drop vs Output Current



Bypass Switch Drop vs Output Current

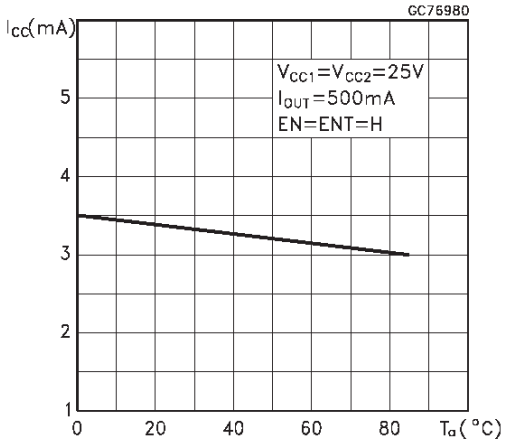


Overload Flag pin Logic Low vs Flag Current

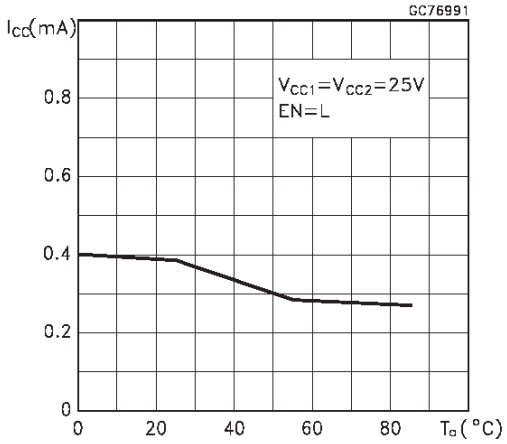


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

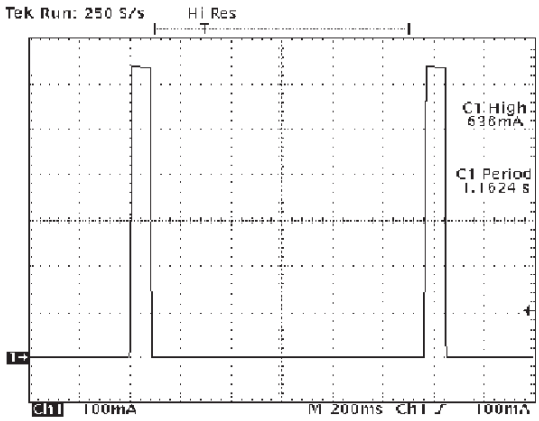
Supply Current vs Temperature



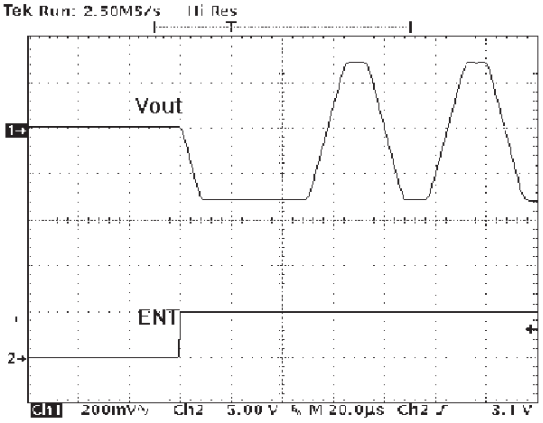
Supply Current vs Temperature



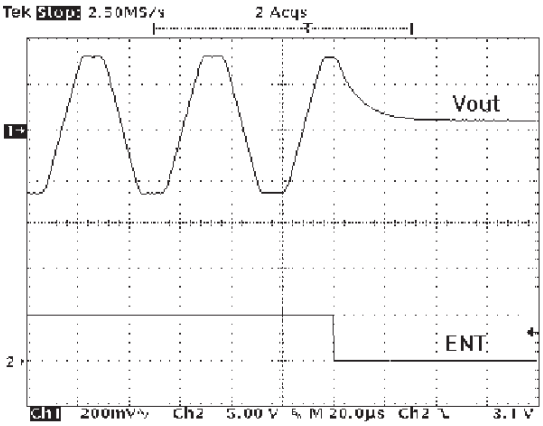
Dynamic Overload protection (I_{SC} vs Time)



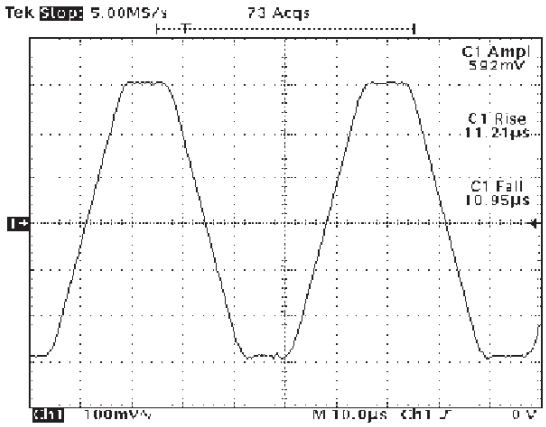
Tone Enable



Tone Disable

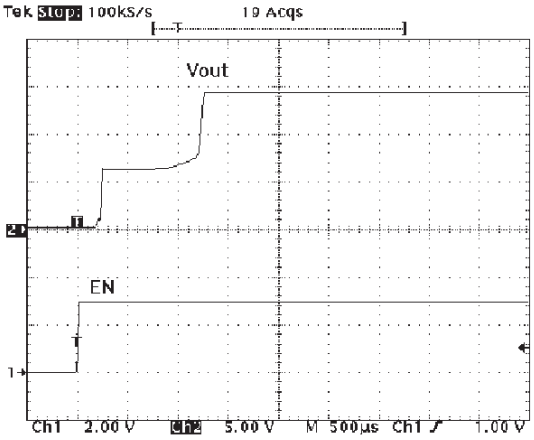


22 KHz Tone

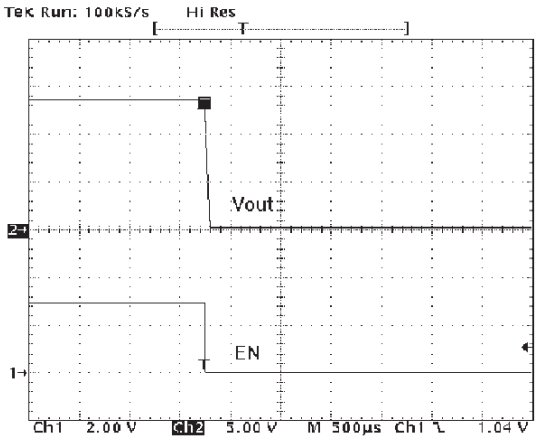


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

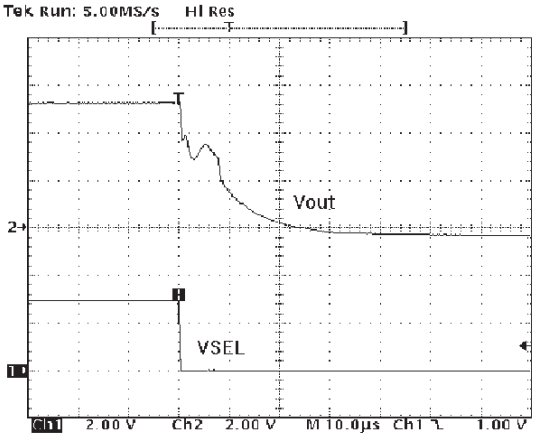
Enable Time



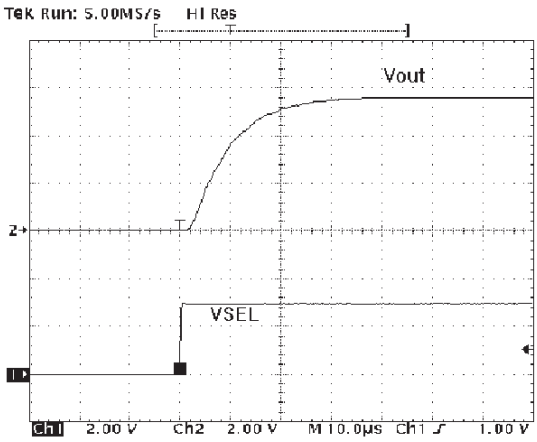
Disable Time



18V to 13V Change

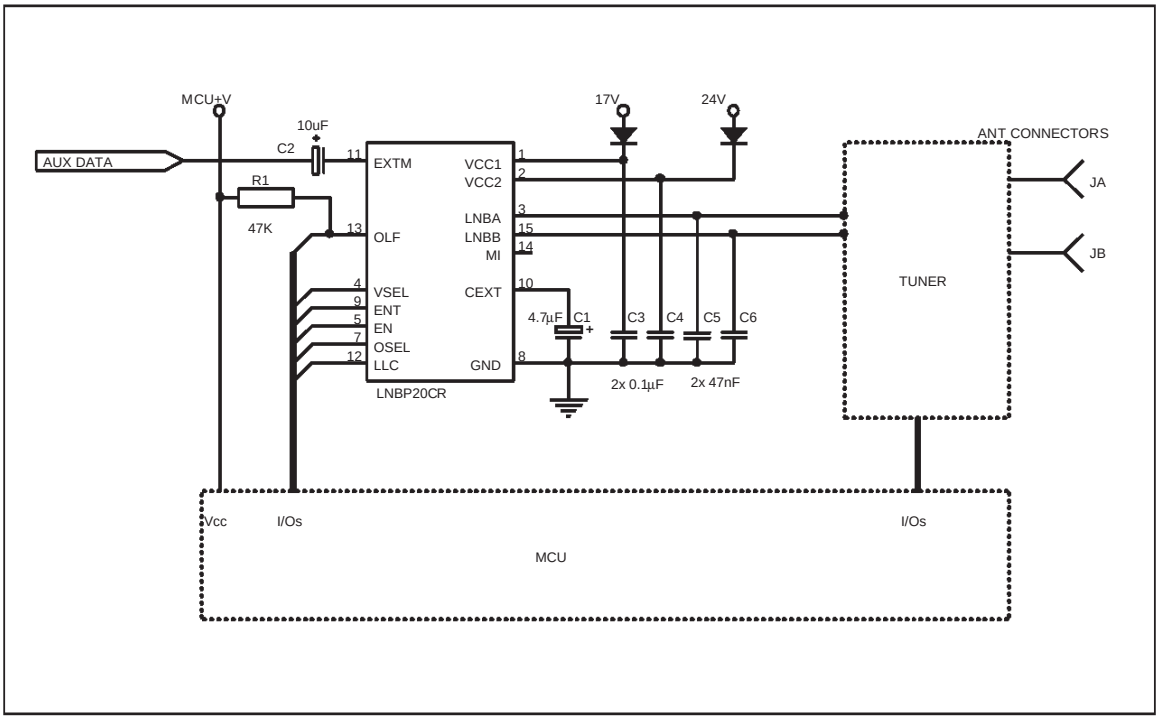


13V to 18V Change

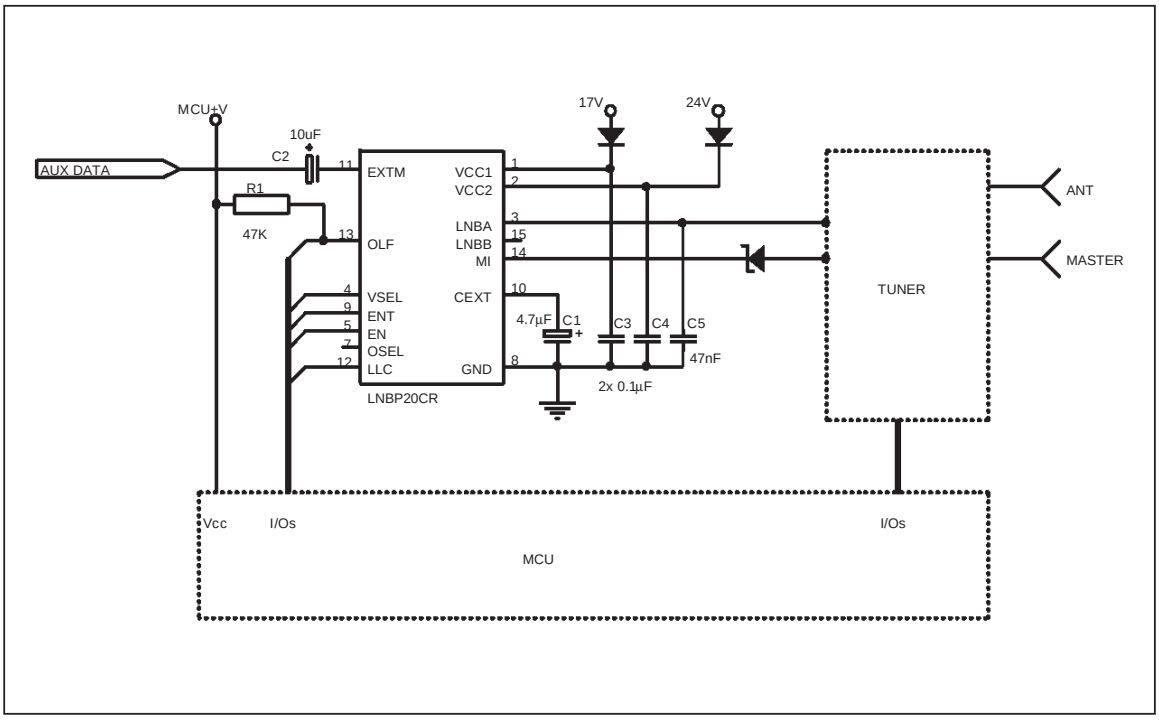


TYPICAL APPLICATION SCHEMATICS

TWO ANTENNA PORTS RECEIVER

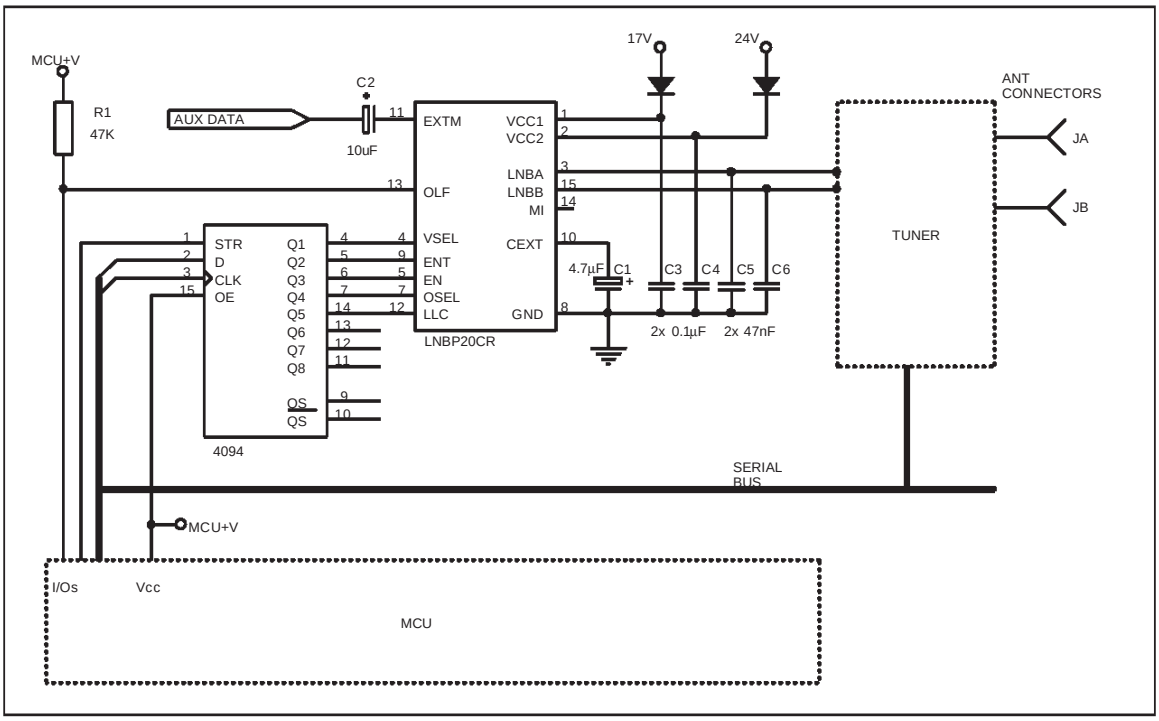


SINGLE ANTENNA RECEIVER WITH MASTER RECEIVER PORT

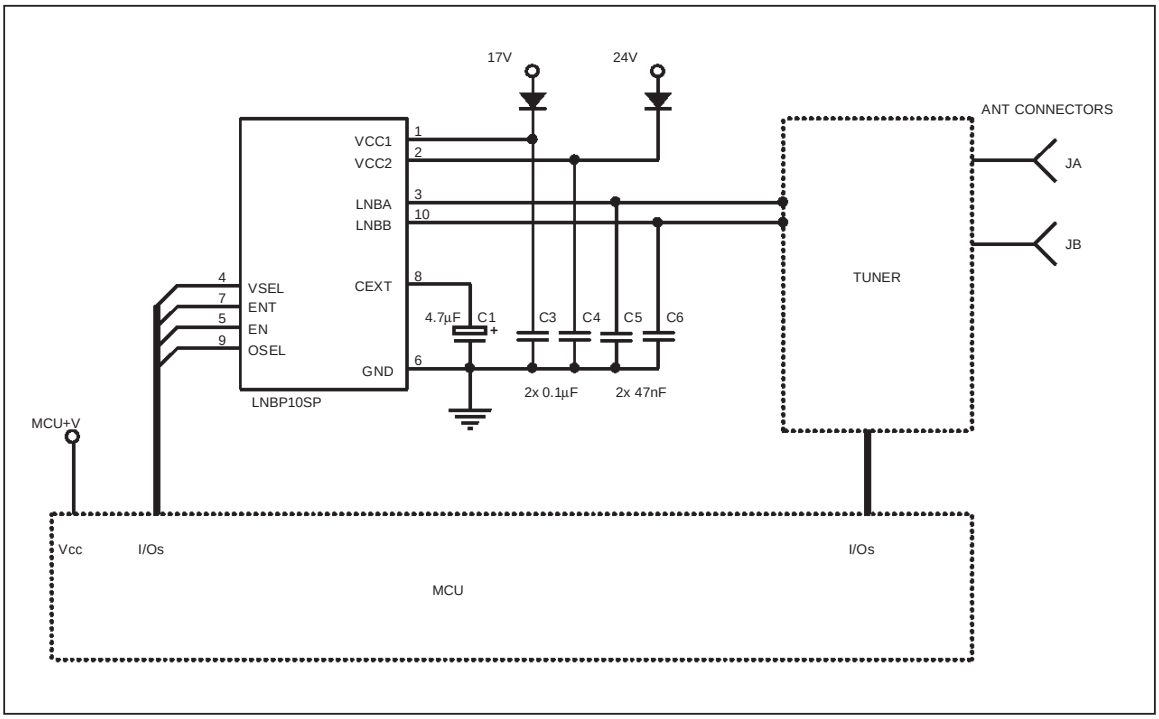


TYPICAL APPLICATION SCHEMATICS (continued)

USING SERIAL BUS TO SAVE MPU I/Os

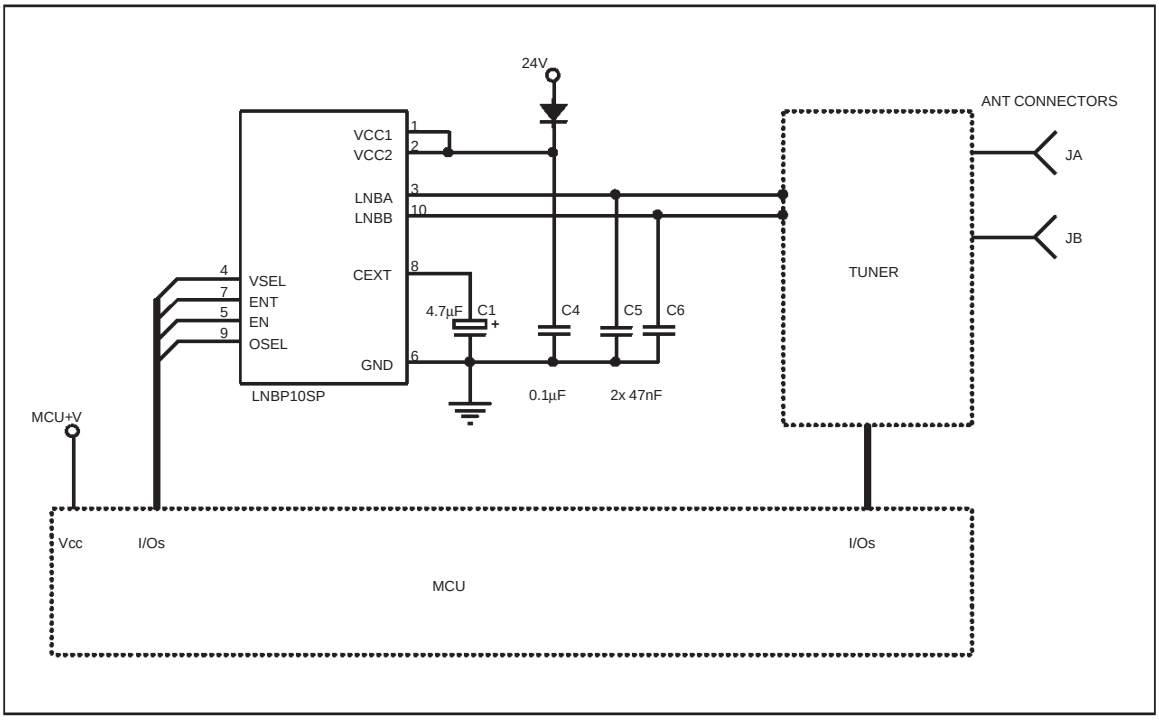


TWO ANTENNA PORTS RECEIVER: LOW COST SOLUTION

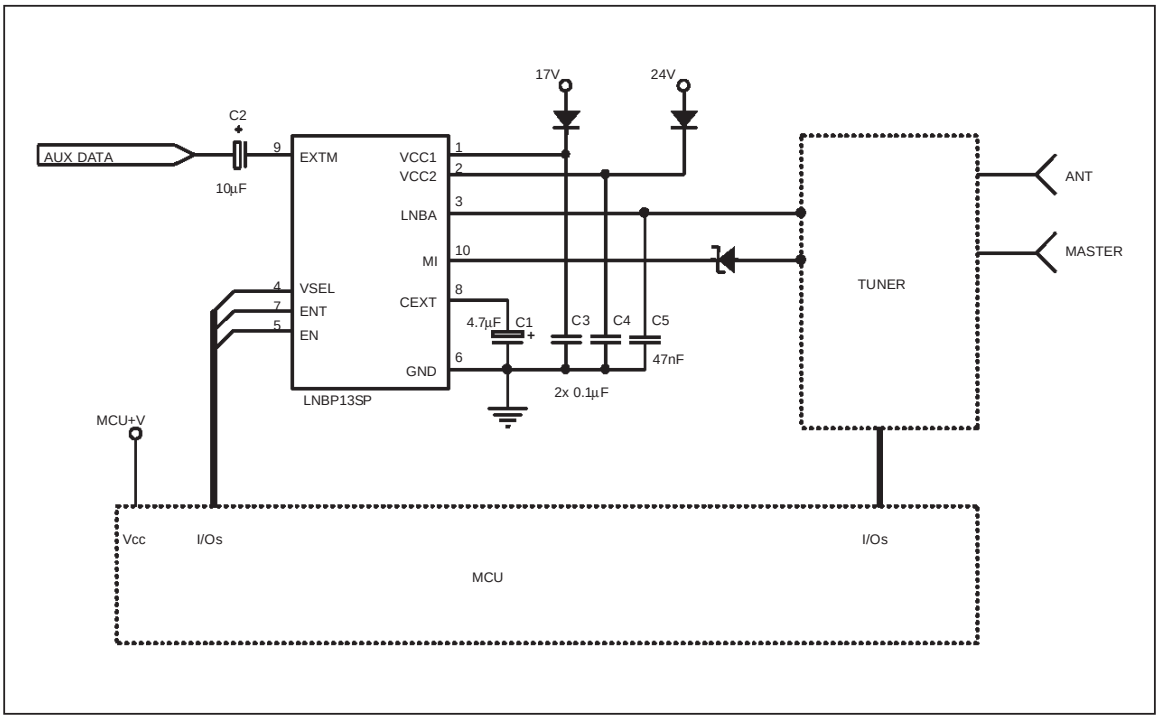


TYPICAL APPLICATION SCHEMATICS (continued)

CONNECTING TOGETHER V_{CC1} AND V_{CC2}

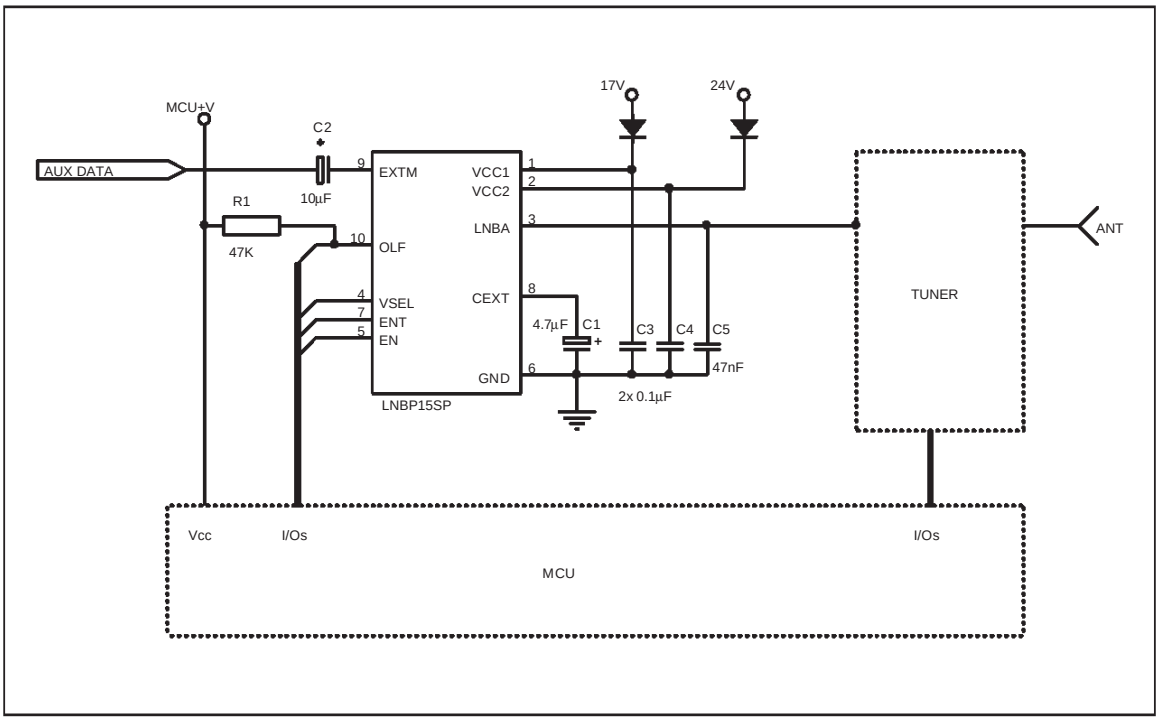


SINGLE ANTENNA RECEIVER WITH MASTER RECEIVER PORT: LOW COST SOLUTION



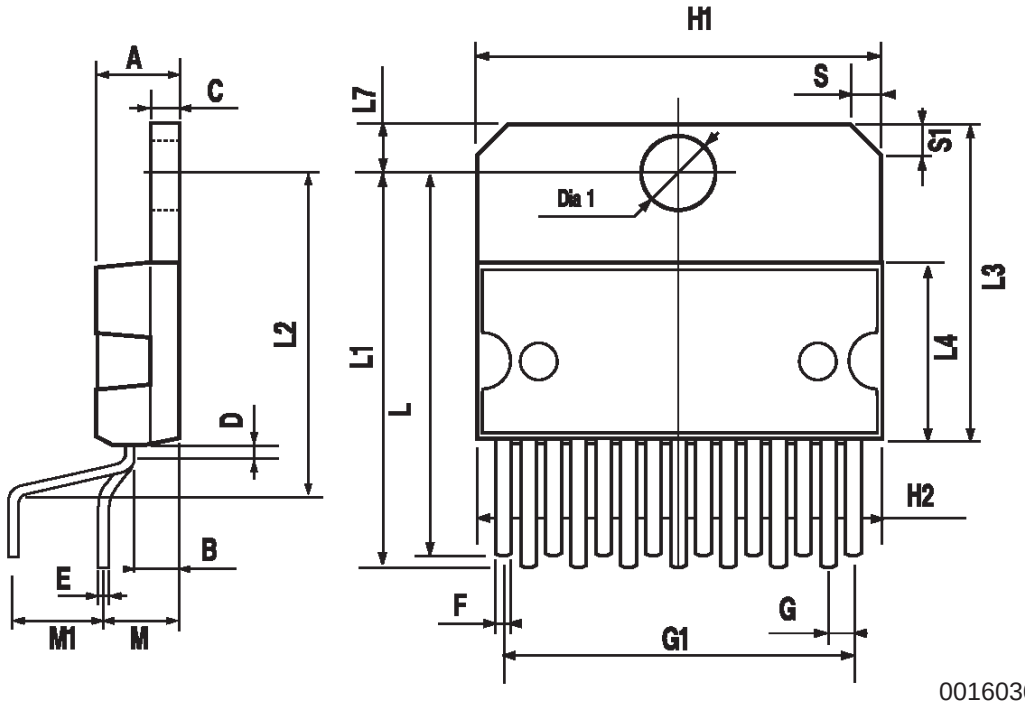
TYPICAL APPLICATION SCHEMATICS (continued)

SINGLE ANTENNA RECEIVER WITH OVERLOAD DIAGNOSTIC



MULTIWATT-15 MECHANICAL DATA

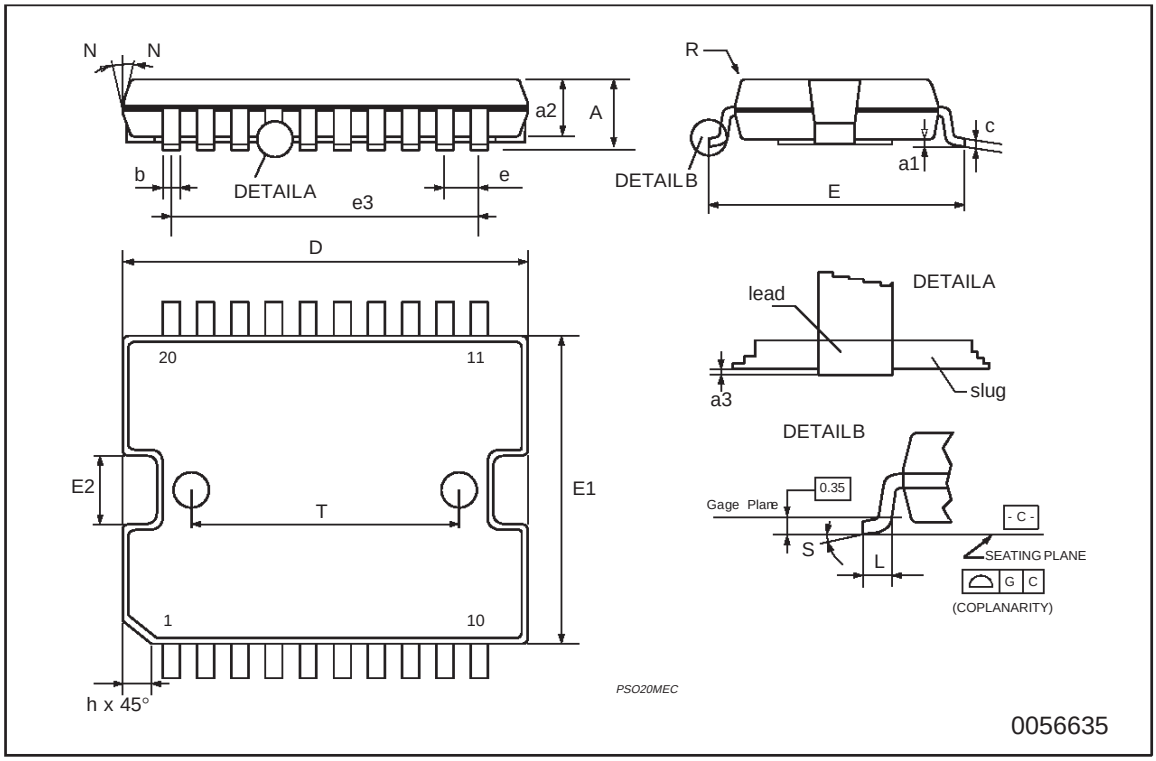
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152



PowerSO-20 MECHANICAL DATA

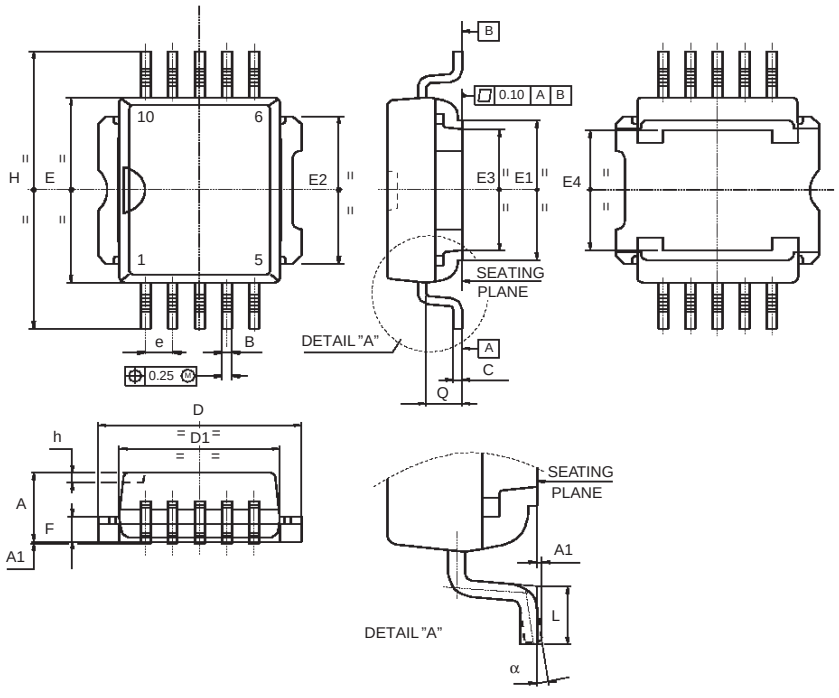
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.40		0.53	0.0157		0.0209
c	0.23		0.32	0.009		0.0126
D (1)	15.80		16.00	0.6220		0.6299
E	13.90		14.50	0.5472		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.90		11.10	0.4291		0.437
E2			2.90			0.1141
G	0		0.10	0		0.0039
h			1.10			0.0433
L	0.80		1.10	0.0314		0.0433
N	10^o (max.)					
S	8^o (max.)					
T		10.0			0.3937	

(1) "D and E1" do not include mold flash or protusions
- Mold flash or protusions shall not exceed 0.15mm (0.006")



PowerSO-10 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0^o		8^o			



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