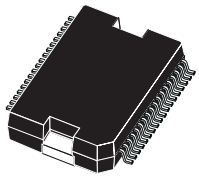
LNBH221

Dual LNB supply and control IC with Step-Up converter and I²C interface

Feature summary

- All the features are the same for both section
- Complete and independent interface between LNBS and relevant I^2C^{TM} BUS
- BUILT-IN DC/DC controller for single 12V supply operation and high efficiency (Typ. 93% @ 500mA)
- LNB output current guaranteed up to 500mA
- Both compliant with eutelsat and directv output voltage specification accurate BUILT-IN 22KHz tone oscillator suits widely accepted standards
- Fast oscillator start-up facilitates DiSEqC^{TM} encoding
- BUILT-IN 22KHz tone detector supports bi-directional DiSEqC^{TM} 2.0
- Semi-lowdrop post regulator and high efficiency step-up pwm for low power loss: Typ. 0.56W @ 125mA
- Two output pins suitable to bypass the output r-l filter and avoid any tone distorsion (R-L filter as per DiSEqC 2.0 SPECs, see application circuit on pag. 7, 8)
- Overload and over-temperature internal protections
- Overload and over-temperature I^2C diagnostic BITs
- LNB short circuit soa protection with I^2C diagnostic bit
- +/- 4KV ESD tolerant on input/output power pins



POWER SO-36

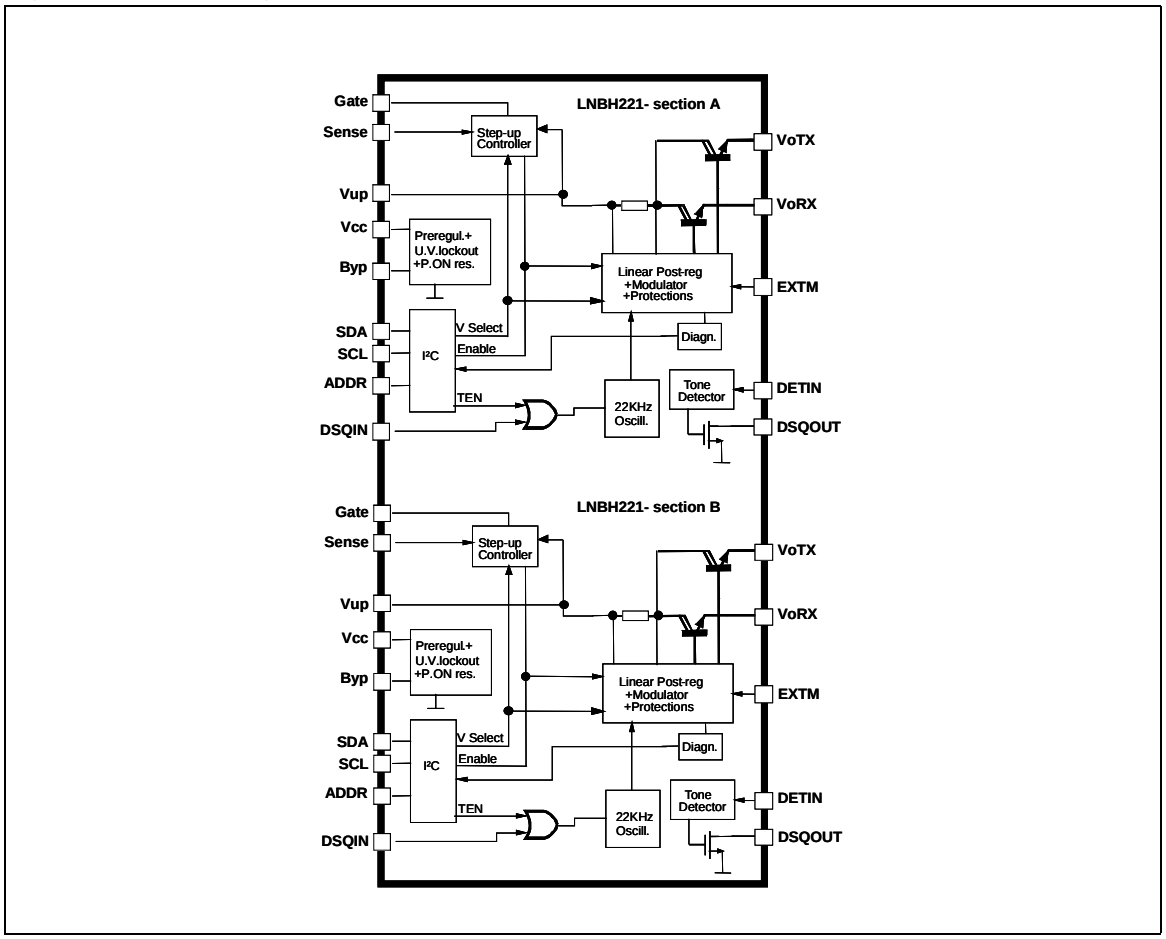
Description

Intended for analog and digital DUAL Satellite STB receivers/SatTV, sets/PC cards, the LNBH221 is a voltage regulator and interface IC, assembled in POWER SO-36, specifically designed to provide the power 13/18V, and the 22KHz tone signalling for two independent LNB down converters or to a multiswitch box that could be independently powered and set. In this application field, it offers a complete solution with extremely low component count, low power dissipation together with simple design and I^2C^{TM} standard interfacing.

Contents

1 Diagram

Figure 1. Block diagram



2 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Input Voltage	-0.3 to 16	V
V_{UP}	DC Input Voltage	-0.3 to 25	V
V_OTX/RX	DC Output Pin Voltage	-0.3 to 25	V
I_O	Output Current	Internally Limited	mA
V_I	Logic Input Voltage (SDA, SCL, DSQIN)	-0.3 to 7	V
V_{DETIN}	Detector Input Signal Amplitude	-0.3 to 2	V_{PP}
V_{OH}	Logic High Output Voltage (DSQOUT)	-0.3 to 7	V
I_{GATE}	Gate Current	±400	mA
V_{SENSE}	Current Sense Voltage	-0.3 to 1	V
$V_{ADDRESS}$	Address Pin Voltage	-0.3 to 7	V
T_{stg}	Storage Temperature Range	-40 to 150	°C
T_J	Operating Junction Temperature Range	-40 to 125	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 2. Thermal Data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal Resistance Junction-Case	2	°C/W

3 Pin configuration

Figure 2. Pin configurations (top view)

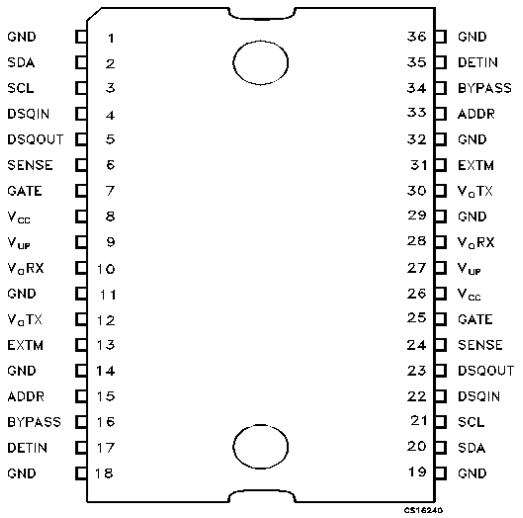


Table 3. Pin description

Symbol	Name	Function	PIN Number Sect:	
			A	B
V_{CC}	Supply Input	8V to 15V supply. A 220µF bypass capacitor to GND with a 470nF (ceramic) in parallel is recommended.	8	26
GATE	External Switch Gate	External MOS switch Gate connection of the step-up converter.	7	25
SENSE	Current Sense (Input)	Current Sense comparator input. Connected to current sensing resistor.	6	24
V_{UP}	Step-up Voltage	Input of the linear post-regulator. The voltage on this pin is monitored by the internal step-up controller to keep a minimum dropout across the linear pass transistor.	9	27
V_ORX	Output Port during 22KHz Tone RX	RX Output to the LNB in DiSEqC 2.0 application. See truth table for voltage selections and description on page 4.	28	10
SDA	Serial Data	Bidirectional data from/to I^2C bus.	2	20
SCL	Serial Clock	Clock from I^2C bus.	3	21
DSQIN	DiSEqC Input	When the TEN bit of the System Register is LOW, this pin will accept the DiSEqC code from the main µcontroller. Each section of the LNBH221 will use this code to modulate the internally generated 22kHz carrier. Set to GND this pin if not used.	4	22
DETIN	Detector In	22kHz Tone Detector Input. Must be AC coupled to the DiSEqC bus.	35	17

Table 3. Pin description

Symbol	Name	Function	PIN Number Sect:	
			A	B
DSQOUT	DiSEqC Output	Open drain output of the Tone Detector to the main µcontroller for DiSEqC data decoding. It is LOW when tone is detected on the DETIN.	5	23
EXTM	External Modulation	External Modulation Input. Needs DC decoupling to the AC source. If not used, can be left open.	31	13
GND	Ground	Circuit Ground. It is internally connected to the die frame for heat dissipation.	1, 14, 18, 19, 32, 36	1, 14, 18, 19, 32, 36
BYP	Bypass Capacitor pin	Needed for internal pre regulator filtering.	34	16
V_OTX	Output Port during 22KHz Tone TX	Output of the linear post regulator/modulator to the LNB. See truth table for voltage selections.	30	12
GND	Ground	To be connected to ground.	29	11
ADDR	Address Setting	Four I^2C bus addresses available by setting the Address Pin level voltage.	33	15

4 Typical application circuits for each section: A and B

Figure 3. Application Circuit For Diseqc 1.x And Output Current Up To 500mA

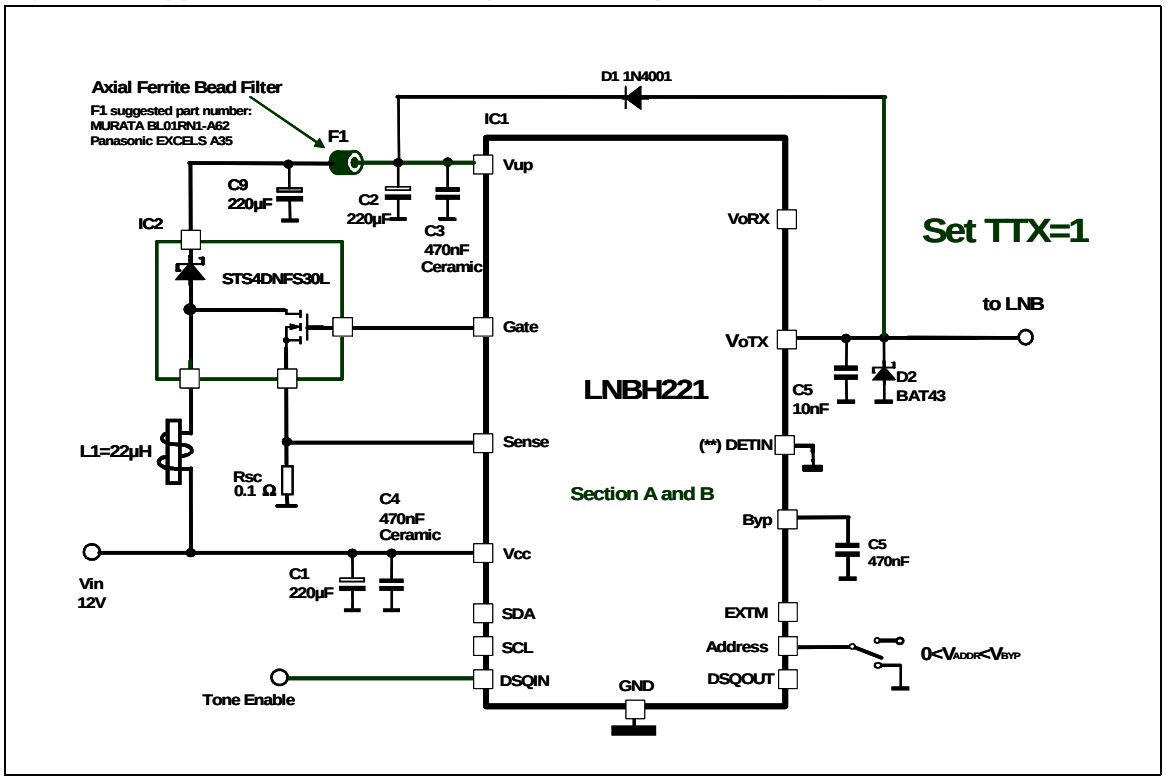
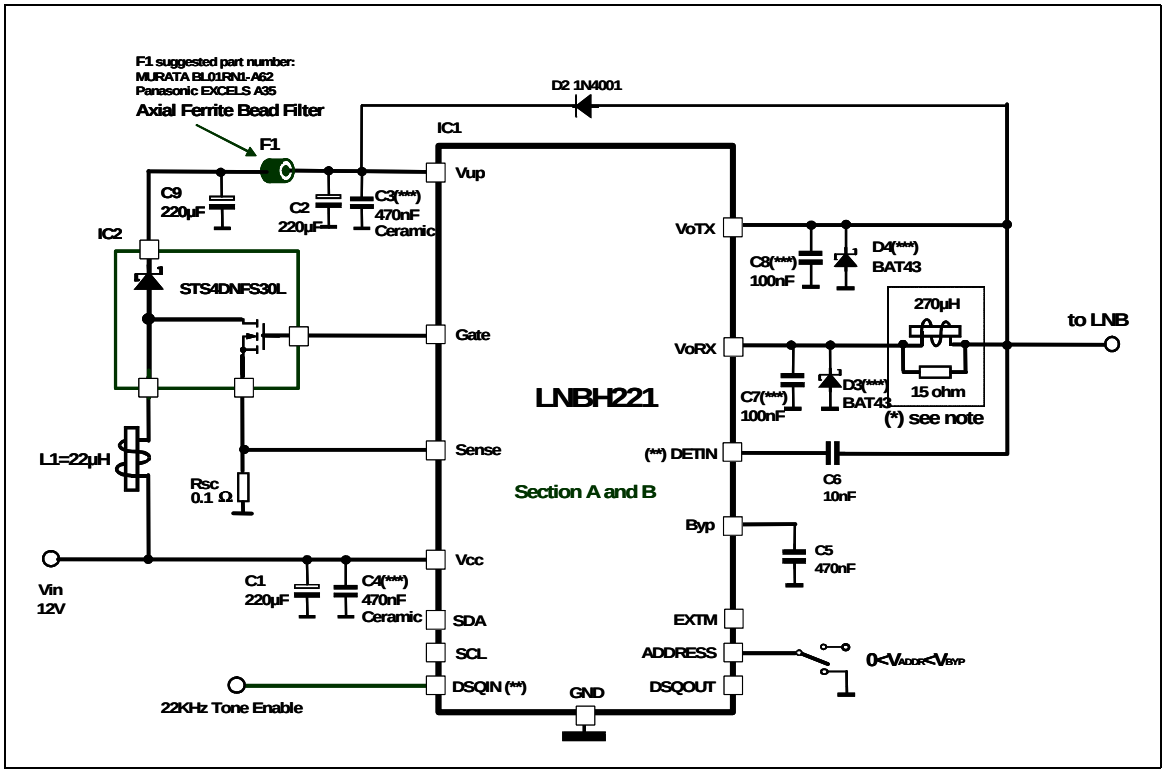


Figure 4. Application Circuit For Bi-directional Diseqc 2.0 And Output Current Up To 500mA



1. C8, D3 and D4 are needed to protect the output pins from any negative voltage spikes during high speed voltage transitions.
2. (*): R-L filter to be used according to EUTELSAT recommendation to implement the DiSEqC™ 2.0, (see DiSEqC™ implementation on page 8). If bidirectional DiSEqC™ 2.0 is not implemented it can be removed both with C8 and D4.
3. (**) Do not leave these pins floating if not used.
4. (***) To be soldered as close as possible to relative pins

5 Application information

Basically, the LNBH221 includes two circuits that are completely independent. Each circuit can be separately controlled and must have its independent external components. All the below specification must be considered equal for each section.

This IC has a built in DC/DC step-up controller that, from a single supply source ranging from 8 to 15V, generates the voltages (V_{UP}) that let the linear post-regulator to work at a minimum dissipated power of 1W typ. @ 500mA load (the linear regulator drop voltage is internally kept at: V_{UP}-V_{OUT}=2V typ.). An UnderVoltage Lockout circuit will disable the whole circuit when the supplied V_{CC} drops below a fixed threshold (6.7V typically). The internal 22KHz tone generator is factory trimmed in accordance to the standards, and can be controlled either by the I^2C^{TM} interface or by a dedicated pin (DSQIN) that allows immediate DiSEqC^{TM} data encoding (*). When the TEN (Tone ENable) I^2C bit it is set to HIGH, a continuous 22KHz tone is generated on the output regardless of the DSQIN pin logic status.

The TEN bit must be set LOW when the DSQIN pin is used for DiSEqC^{TM} encoding. The fully bi-directional DiSEqC^{TM} 2.0 interfacing is completed by the built-in 22KHz tone detector. Its input pin (DETIN) must be AC coupled to the DiSEqC^{TM} bus, and the extracted PWK data are available on the DSQOUT pin (*). To comply to the bi-directional DiSEqC^{TM} 2.0 bus hardware requirements an output R-L filter is needed. The LNBH221 is provided with two output pins: the V_OTX to be used during the tone transmission and the V_ORX to be used when the tone is received. This allows the 22KHz Tone to pass without any losses due to the R-L filter impedance (see DiSeqC 2.0 application circuit on page 4). In DiSeqC 2.0 applications during the 22KHz transmission activated by DSQIN pin (or TEN I^2C bit), the V_OTX pin must be preventively set ON by the TTX I^2C bit and, both the 13/18V power supply and the 22KHz tone, are provided by mean of V_OTX output. As soon as the tone transmission is expired, the V_OTX must be set to OFF by setting the TTX I^2C bit to zero and the 13/18V power supply is provided to the LNB by the V_ORX pin through the R-L filter. When the LNBH221 is used in DiSeqC 1.x applications the R-L filter is not required (see DiSeqC 1.x application circuit on pag. 4), the TTX I^2C bit must be kept always to HIGH so that, the V_OTX output pin can provide both the 13/18V power supply and the 22KHz tone, enabled by DSQIN pin or by TEN I^2C bit. All the functions of this IC are controlled via I^2C^{TM} bus by writing 6 bits on the System Register (SR, 8 bits). The same register can be read back, and two bits will report the diagnostic status. When the IC is put in Stand-by (EN bit LOW), the power blocks are disabled.

When the regulator blocks are active (EN bit HIGH), the output can be logic controlled to be 13 or 18V by mean of the VSEL bit (Voltage SELect) for remote controlling of non-DiSEqC LNBs. Additionally, the LNBH221 is provided with the LLC I^2C bit that increase the selected voltage value (+1V when VSEL=0 and +1.5V when VSEL=1) to compensate for the excess voltage drop along the coaxial cable (LLC bit HIGH). By mean of the LLC bit, the LNBH221 is also compliant to the American LNB power supply standards that require the higher output voltage level to 19.5V (typ.) (instead of 18V), by simply setting the LLC=1 when VSEL=1. In order to improve design flexibility and to allow implementation of newcoming LNB remote control standards, an analogic modulation input pin is available (EXTM).

An appropriate DC blocking capacitor must be used to couple the modulating signal source to the EXTM pin. Also in this case, the V_OTX output must be set ON during the tone transmission by setting the TTX bit high. When external modulation is not used, the relevant pin can be left open. The current limitation block is SOA type: if the output port is shorted to ground, the SOA current limitation block limits the short circuit current (I_{SC}) at typically 300mA or 200mA respectively for V_{OUT} 13V or 18V, to reduce the power dissipation.

Moreover, it is possible to set the Short Circuit Current protection either statically (simple current clamp) or dynamically by the PCL bit of the I^2C SR; when the PCL (Pulsed Current Limiting) bit is set to LOW, the overcurrent protection circuit works dynamically, as soon as an overload is detected, the output is shut-down for a time T_{OFF}, typically 900ms. Simultaneously the OLF bit of the System Register is set to HIGH. After this time has elapsed, the output is resumed for a time T_{ON}=1/10T_{OFF} (typ.). At the end of T_{ON}, if the overload is still detected, the protection circuit will cycle again through T_{OFF} and T_{ON}. At the end of a full T_{ON} in which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical T_{ON}+T_{OFF} time is 990ms and it is determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in short circuit condition, still ensuring excellent power-on start up in most conditions. However, there could be some cases in which an highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (PCL=HIGH) and then switching to the dynamic mode (PCL=LOW) after a chosen amount of time. When in static mode, the OLF bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared. This IC is also protected against overheating: when the junction temperature exceeds 150°C (typ.), the step-up converter and the linear regulator are shut off, and the OTF SR bit is set to HIGH. Normal operation is resumed and the OTF bit is reset to LOW when the junction is cooled down to 140°C (typ.).

Note: (*): External components are needed to comply to bi-directional DiSEqC™ bus hardware requirements. Full compliance of the whole application to DiSEqC™ specifications is not implied by the use of this IC.

Note: NOTICE: DiSEqC is a trademark of EUTELSAT. I^2C is a trademark of Philips Semiconductors.

5.1 I^2C Bus Interface (one for each section)

Data transmission from main µP to the LNBH221 and viceversa takes place through the 2 wires I^2C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

5.2 Data validity

As shown in *Figure 5.*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

5.3 Start and stop conditions

As shown in *Figure 6.* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

5.4 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

5.5 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 7.*). The peripheral (LNBH221) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer. The LNBH221 won't generate the acknowledge if the V_{CC} supply is below the Undervoltage Lockout threshold (6.7V typ.).

5.6 Transmission without acknowledgement

Avoiding to detect the acknowledge of the LNBH221, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity..

Figure 5. Data Validity On The I^2C Bus

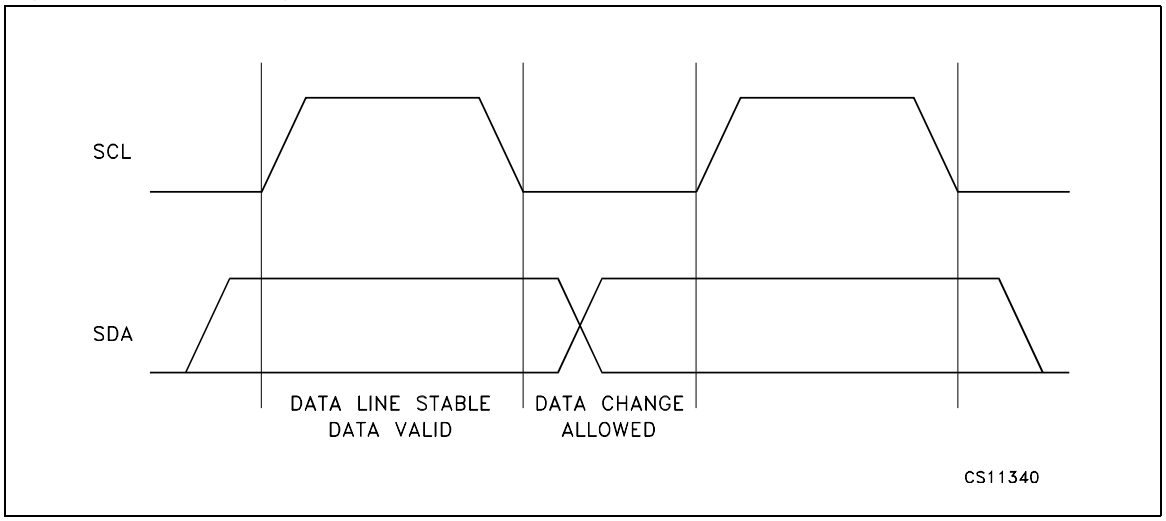


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Figure 6. Timing Diagram On I²C Bus

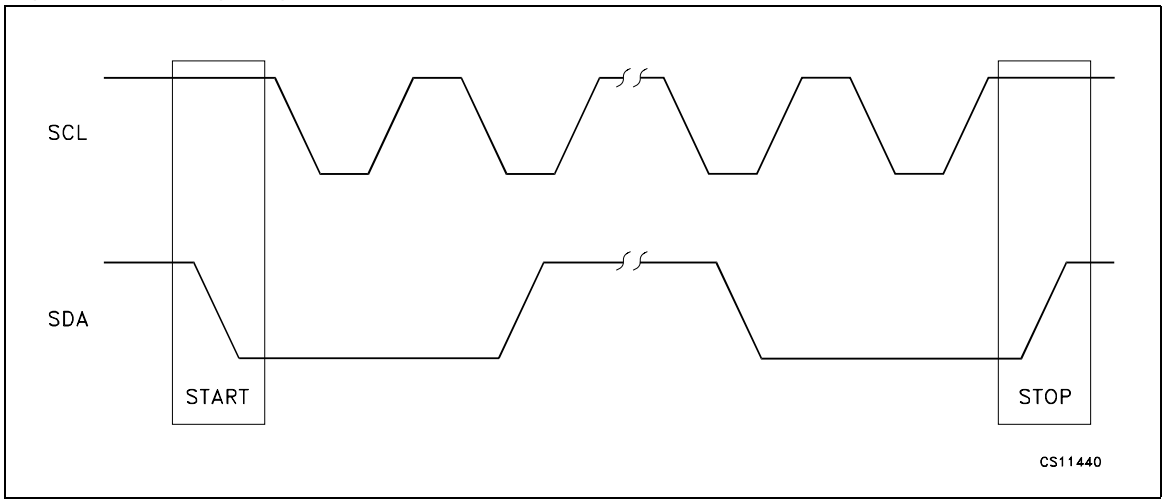
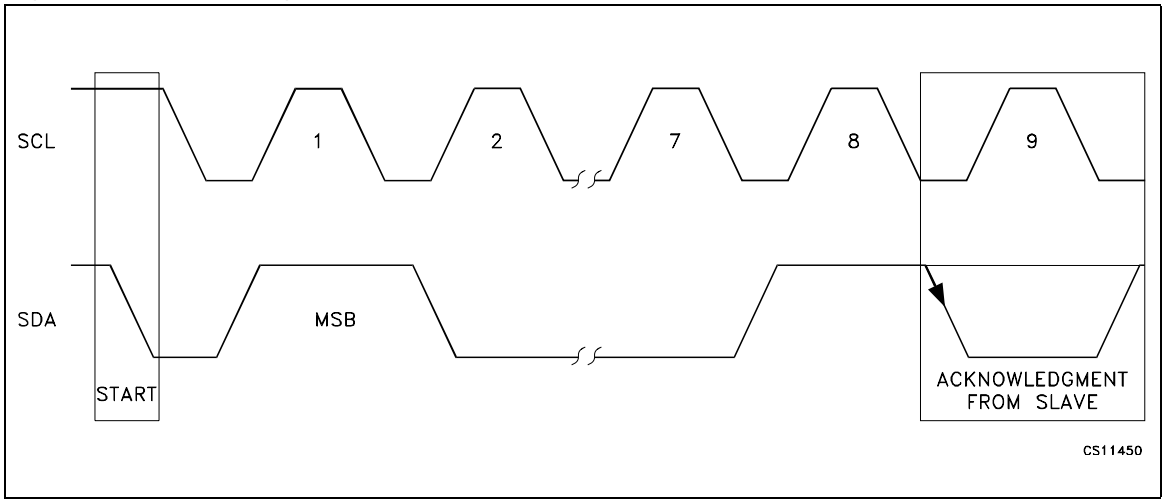


Figure 7. Acknowledge On I²C Bus



6 LNBH221 software description (same for both section)

6.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte = hex 10 / 11 (the LSB bit determines read(=1)/write(=0) transmission)
- A sequence of data (1 byte + acknowledge)
- A stop condition (P)

	CHIP ADDRESS										DATA									
	MSB							LSB			MSB							LSB		
S	0	0	0	1	0	0	0	R/W	ACK										ACK	P

ACK= Acknowledge

S= Start

P= Stop

R/W= Read/Write

6.2 System register (SR, 1 Byte)

MSB							LSB
R, W	R, W	R, W	R, W	R, W	R, W	R	R
PCL	TTX	TEN	LLC	VSEL	EN	OTF	OLF

R,W= read and write bit

R= Read-only bit

All bits reset to 0 at Power-On

6.3 Transmitted data (I^2C BUS write mode)

When the R/W bit in the chip address is set to 0, the main µP can write on the System Register (SR) of the LNBH221 via I^2C bus. Only 6 bits out of the 8 available can be written by the µP, since the remaining 2 are left to the diagnostic flags, and are read-only.

PCL	TTX	TEN	LLC	VSEL	EN	OTF	OLF	Function
			0	0	1	X	X	V_{OUT}=13.25V, V_{UP}=15.25V
			0	1	1	X	X	V_{OUT}=18V, V_{UP}=20V
			1	0	1	X	X	V_{OUT}=14.25V, V_{UP}=16.25V
			1	1	1	X	X	V_{OUT}=19.5V, V_{UP}=21.5V
		0			1	X	X	22KHz tone is controlled by DSQIN pin
		1			1	X	X	22KHz tone is ON, DSQIN pin disabled
	0				1	X	X	V_ORX output is ON, output voltage controlled by VSEL and LLC
	1	X			1	X	X	V_OTX output is ON, 22KHz controlled by DSQIN or TEN, output voltage level controlled by VSEL and LLC
0					1	X	X	Pulsed (dynamic) current limiting is selected
1					1	X	X	Static current limiting is selected
X	X	X	X	X	0	X	X	Power blocks disabled

X= don't care.

Values are typical unless otherwise specified.

6.4 Received data (I^2C bus READ MODE)

The LNBH221 can provide to the Master a copy of the SYSTEM REGISTER information via I^2C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1.

At the following master generated clocks bits, the LNBH221 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- acknowledge the reception, starting in this way the transmission of another byte from the LNBH221;

- no acknowledge, stopping the read mode communication.

While the whole register is read back by the µP, only the two read-only bits OLF and OTF convey diagnostic informations about the LNBH221.

PCL	ISEL	TEN	LLC	VSEL	EN	OTF	OLF	Function
These bits are read exactly the same as they were left after last write operation						0		T_J<140°C, normal operation
						1		T_J>150°C, power block disabled
							0	I_{OUT}<I_{OMAX}, normal operation
							1	I_{OUT}>I_{OMAX}, overload protection triggered

Values are typical unless otherwise specified.

6.5 Power-On I^2C interface reset

The I^2C interface built in the LNBH221 is automatically reset at power-on. As long as the V_{CC} stays below the UnderVoltage Lockout threshold (6.7V typ.), the interface will not respond to any I^2C command and the System Register (SR) is initialized to all zeroes, thus keeping the power blocks disabled. Once the V_{CC} rises above 7.3V typ, the I^2C interface becomes operative and the SR can be configured by the main µP. This is due to 500mV of hysteresis provided in the UVL threshold to avoid false retriggering of the Power-On reset circuit.

6.6 Address Pin

Connecting this pin to GND the Chip I^2C interface address is 0001000, but, it is possible to choice among 4 different addresses simply setting this pin at 4 fixed voltage levels (see *Table 7.* on page 17).

6.7 DiSEqC™ Implementation

The LNBH221 helps the system designer to implement the bi-directional DiSEqC 2.0 protocol by allowing an easy PWK modulation/demodulation of the 22KHz carrier. The PWK data are exchanged between the LNBH221 and the main µP using logic levels that are compatible with both 3.3 and 5V microcontrollers. This data exchange is made through two dedicated pins, DSQIN and DSQOUT, in order to maintain the timing relationships between the PWK data and the PWK modulation as accurate as possible. These two pins should be directly connected to two I/O pins of the µP, thus leaving to the resident firmware the task of encoding and decoding the PWK data in accordance to the DiSEqC protocol. Full compliance of the system to the specification is thus not implied by the bare use of the LNBH221. The system designer should also take in consideration the bus hardware requirements; that can be simply accomplished by the R-L termination connected on the V_{OUT} pins of the LNBH221, as shown in the Typical Application Circuit on page 7, 8. To avoid any losses due to the R-L impedance during the tone transmission, the LNBH221 has dedicated output (V_OTX) that, in a DiSEqC 2.0 application, is connected after the filter and must be enabled by setting the TTX SR bit HIGH only during the tone transmission (see DiSEqC 2.O operation description on page 9).

Unidirectional (1.x) DiSEqC and non-DiSEqC systems normally don't need this termination, and the V_OTX pin can be directly connected to the LNB supply port of the Tuner (see DiSeqC 1.x application circuit on pag. 7, 8). There is also no need of Tone Decoding, thus DETIN and DSQOUT pins can be left unconnected and the Tone is provided by the V_OTX.

7 Electrical characteristics

Table 4. Electrical characteristics of each section (A and B)
(T_J = 0 to 85°C, EN=1, TTX=0/1, LLC=VSEL=TEN=PCL=0, DSQIN=LOW, V_{IN}=12V, I_{OUT}=50mA, unless otherwise specified. See software description section for I^2C access to the system register)

Symbol	Parameter	Parameter		Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage	I_{OUT} = 500 mA TEN=VSEL=LLC=1		8		15	V
I_{IN}	Supply Current	EN=TEN=VSEL=LLC=1, No Load			20	40	mA
		EN=0			3.5	7	
V_{OUT}	Output Voltage	I_{OUT} = 500 mA VSEL=1	LLC=0	17.3	18	18.7	V
			LLC=1	18.7	19.5	20.3	
V_{OUT}	Output Voltage	I_O = 500 mA VSEL=0	LLC=0	12.75	13.25	13.75	V
			LLC=1	13.75	14.25	14.75	
ΔV_{OUT}	Line Regulation	V_{IN} =8 to 15V	VSEL=0		5	40	mV
			VSEL=1		5	60	
ΔV_{OUT}	Load Regulation	VSEL = 0 or 1 I_{OUT} = 50 to 500mA				200	mV
I_{MAX}	Output Current Limiting			500		750	mA
I_{SC}	Output Short Circuit Current	VSEL = 0			300		mA
		VSEL = 1			200		
t_{OFF}	Dynamic Overload protection OFF Time	PCL=0Output Shorted			900		ms
t_{ON}	Dynamic Overload protection ON Time	PCL=0Output Shorted			t_{OFF}/10		ms
f_{TONE}	Tone Frequency	TEN=1		20	22	24	KHz
A_{TONE}	Tone Amplitude	TEN=1		0.55	0.72	0.9	V_{PP}
D_{TONE}	Tone Duty Cycle	TEN=1		40	50	60	%
t_r, t_f	Tone Rise and Fall Time	TEN=1		5	8	15	µs
G_{EXTM}	External Modulation Gain	$\Delta V_{OUT}/\Delta V_{EXTM}$, f = 10Hz to 50KHz, TTX=1			6		
V_{EXTM}	External Modulation Input Voltage	AC Coupling, TTX=1				400	mV_{PP}
Z_{EXTM}	External Modulation Impedance	f = 10Hz to 50KHz			260		W
f_{SW}	DC/DC Converter Switch Frequency				220		kHz
f_{DETIN}	Tone Detector Frequency Capture Range	0.4Vpp sinewave		18		24	kHz

Table 4. Electrical characteristics of each section (A and B)
(T_J = 0 to 85°C, EN=1, TTX=0/1, LLC=VSEL=TEN=PCL=0, DSQIN=LOW, V_{IN}=12V, I_{OUT}=50mA, unless otherwise specified. See software description section for I^2C access to the system register)

Symbol	Parameter	Parameter	Min.	Typ.	Max.	Unit
V_{DETIN}	Tone Detector Input Amplitude	f_{IN}=22kHz sinewave	0.2		1.5	V_{PP}
Z_{DETIN}	Tone Detector Input Impedance			150		kΩ
V_{OL}	DSQOUT Pin Logic LOW	Tone presentI_{OL}=2mA		0.3	0.5	V
I_{OZ}	DSQOUT Pin Leakage Current	Tone absentV_{OH} = 6V			10	µA
V_{IL}	DSQIN Input Pin Logic LOW				0.8	V
V_{IH}	DSQIN Input Pin Logic HIGH		2			V
I_{IH}	DSQIN Pin Input Current	V_{IH} = 5V		15		µA
I_{OBK}	Output Backward Current	EN=0 V_{OBK} = 18V		-6	-15	mA
T_{SHDN}	Thermal Shutdown Threshold			150		°C
ΔT_{SHDN}	Thermal Shutdown Hysteresis			15		°C

Table 5. Gate And Sense Electrical Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Parameter	Min.	Typ.	Max.	Unit
R_{DSON-L}	Gate LOW R_{DSON}	I_{GATE}=-100mA		4.5		Ω
R_{DSON-H}	Gate LOW R_{DSON}	I_{GATE}=100mA		4.5		Ω
V_{SENSE}	Current Limit Sense Voltage			200		mV

Table 6. I^2C Electrical Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	LOW Level Input Voltage	SDA, SCL			0.8	V
V_{IH}	HIGH Level Input Voltage	SDA, SCL	2			V
I_{IN}	Input Current	SDA, SCL, V_{IN}= 0.4 to 4.5V	-10		10	µA
V_{OL}	Low Level Output Voltage	SDA (open drain), I_{OL} = 6mA			0.6	V
f_{MAX}	Maximum Clock Frequency	SCL	500			KHz

Table 7. Address Pin Characteristics (T_J = 0 to 85°C, V_{IN}=12V)

Symbol	Parameter	Parameter	Min.	Typ.	Max.	Unit
V_{ADDR-1}	"0001000" Addr Pin Voltage		0		0.7	V
V_{ADDR-2}	"0001001" Addr Pin Voltage		1.3		1.7	V
V_{ADDR-3}	"0001010" Addr Pin Voltage		2.3		2.7	V
V_{ADDR-4}	"0001011" Addr Pin Voltage		3.3		5	V
V_{ADDR-1}	"0001000" Addr Pin Voltage		0		0.7	V

8 Thermal design notes

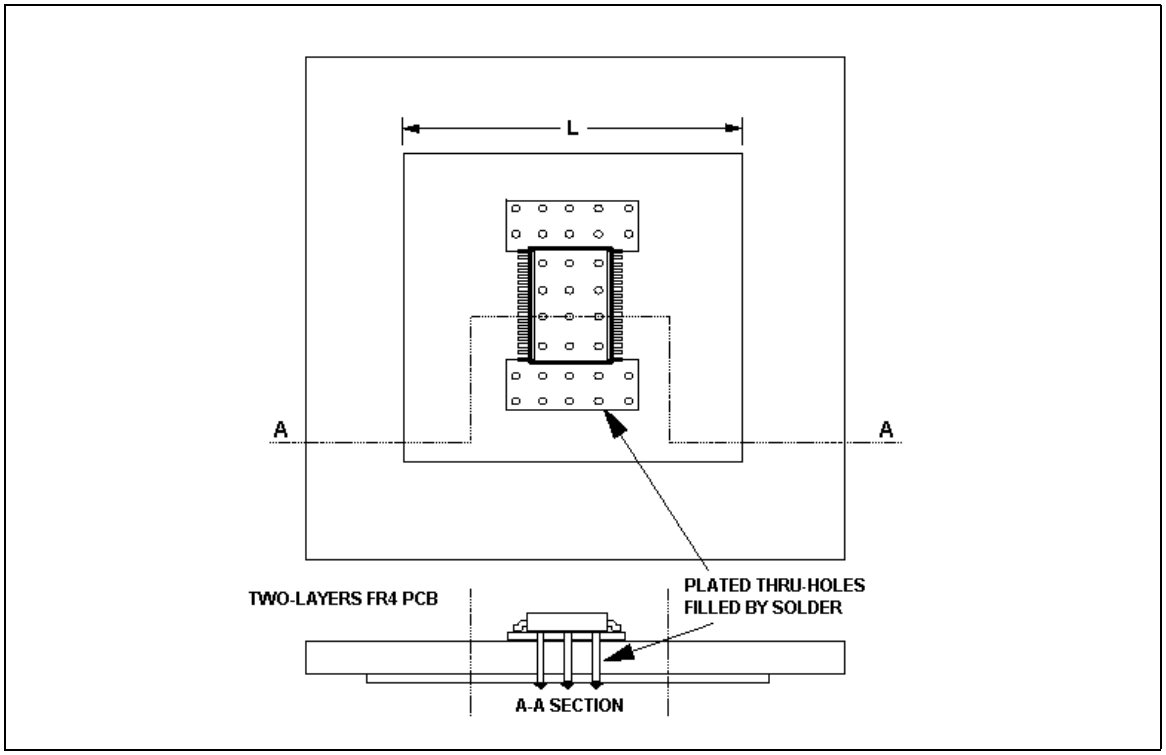
During normal operation, the LNBH221 device dissipates some power. At rated output current of 500mA on each section output, the voltage drop on both linear regulators lead to a total dissipated power that is typically 2W. The heat generated requires a suitable heatsink to keep the junction temperature below the over-temperature protection threshold. Assuming a 45°C temperature inside the Set-Top-Box case, the total R_{thJC} has to be less than 40°C/W.

While this can be easily achieved using a through-hole power package that can be attached to a small heatsink or to the metallic frame of the receiver, a surface mount power package must rely on PCB solutions whose thermal efficiency is often limited. The simplest solution is to use a large, continuous copper area of the GND layer to dissipate the heat coming from the IC body.

Given for the PSO-36 package an R_{thJC} equal to 2°C/W, a maximum of 38°C/W are left to the PCB heatsink. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, an unbroken GND area even on the opposite side where the IC is placed. In *Figure 8.*, it is shown a suggested layout for the PSO-36 package with a dual layer PCB, where the IC exposed pad connected to GND and the square dissipating area are thermally connected through 32 vias holes, filled by solder. This arrangement, when L=40mm, achieves an R_{thJA} of about 28°C/W.

Different layouts are possible, too. Basic principles, however, suggest to keep the IC and its ground exposed pad approximately in the middle of the dissipating area; to provide as many vias as possible; to design a dissipating area having a shape as square as possible and not interrupted by other copper traces.

Figure 8. PowerSO-36 Suggested Pcb Heatsink Layout



9 Typical performance characteristics (of each section)

(T_J = 25°C, unless otherwise specification)

Figure 9. Output Voltage vs Temperature

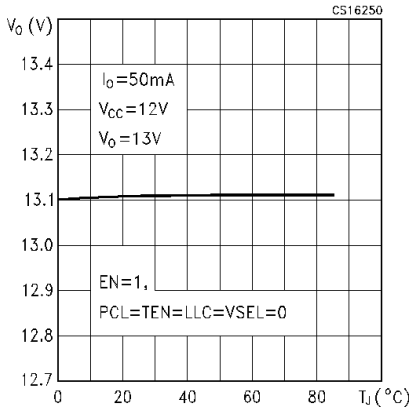


Figure 10. Output Voltage vs Temperature

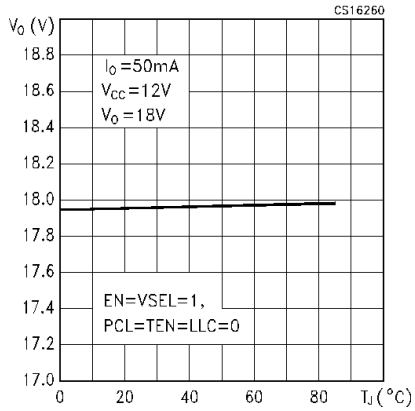


Figure 11. Output Voltage vs Temperature

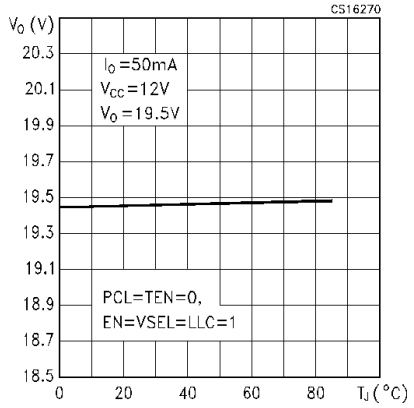


Figure 12. Load Regulation vs Temperature

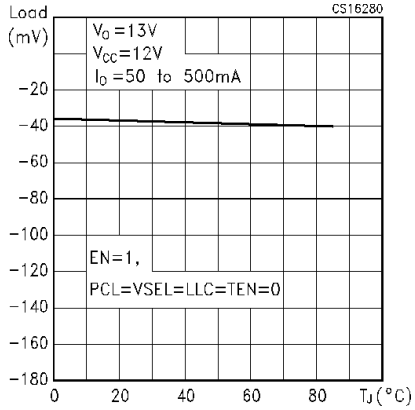


Figure 13. Load Regulation vs Temperature

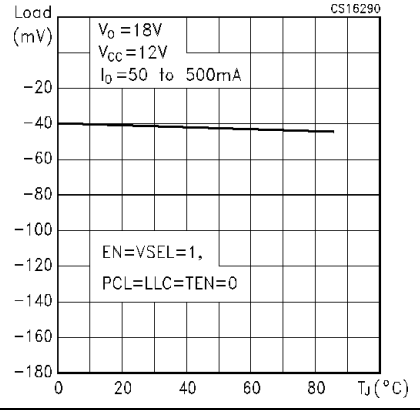


Figure 14. Supply Current vs Temperature

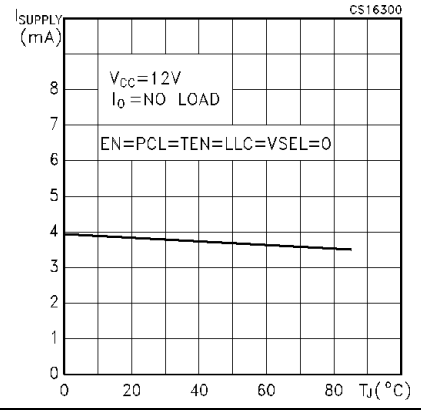


Figure 15. Supply Current vs Temperature

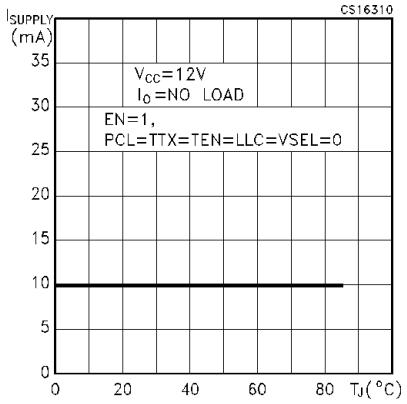


Figure 16. Supply Current vs Temperature

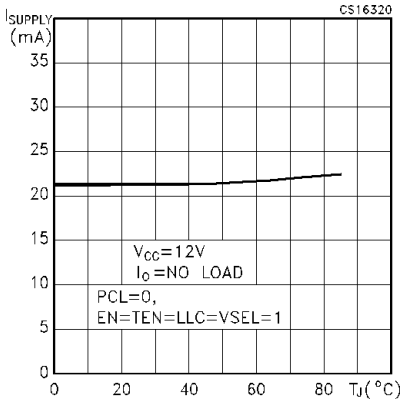


Figure 17. Dynamic Overload Protection ON Time vs Temperature

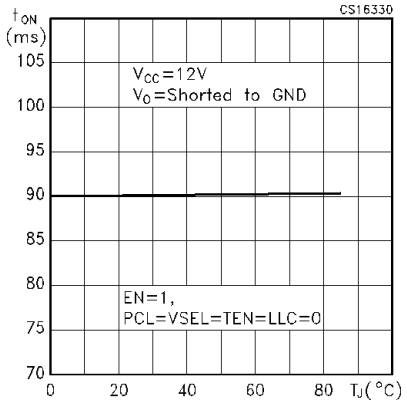


Figure 18. Dynamic Overload Protection OFF Time vs Temperature

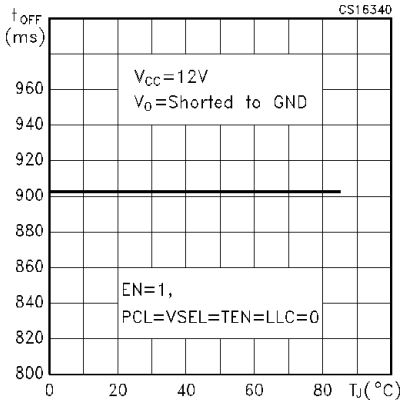


Figure 19. Output Current Limiting vs Temperature

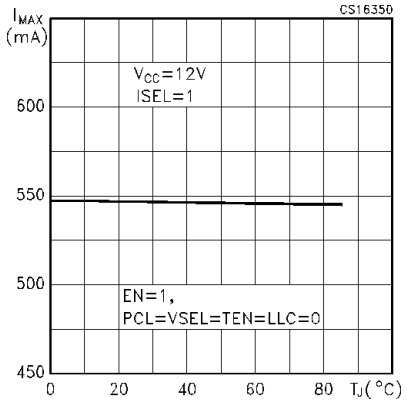


Figure 20. Tone Frequency vs Temperature

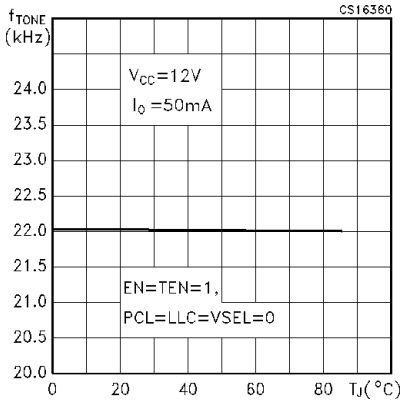


Figure 21. Tone Amplitude vs Temperature

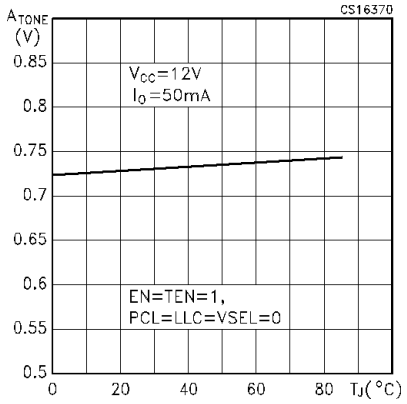


Figure 22. Tone Duty Cycle vs Temperature

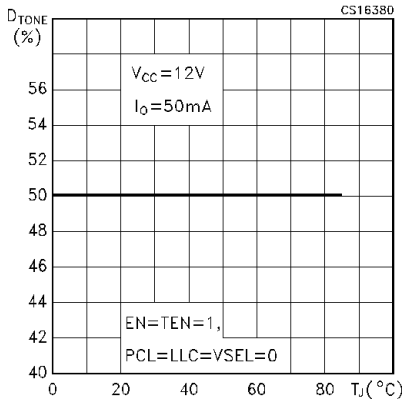


Figure 23. Tone Rise Time vs Temperature

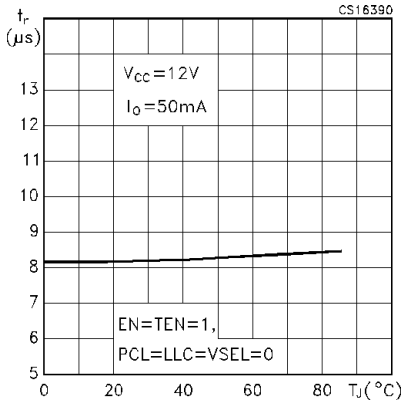


Figure 24. Tone Fall Time vs Temperature

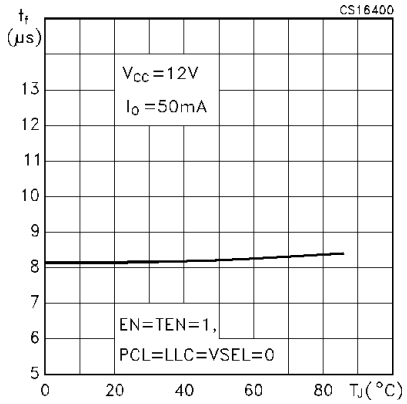


Figure 25. Undervoltage Lockout Threshold vs Temperature

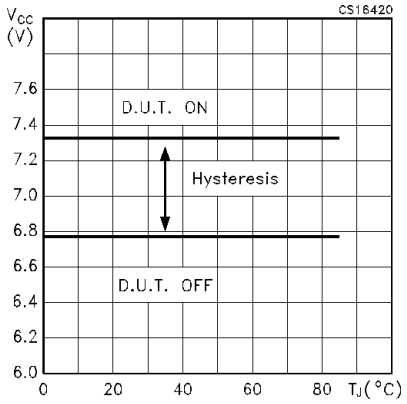


Figure 26. Output Backward Current vs Temperature

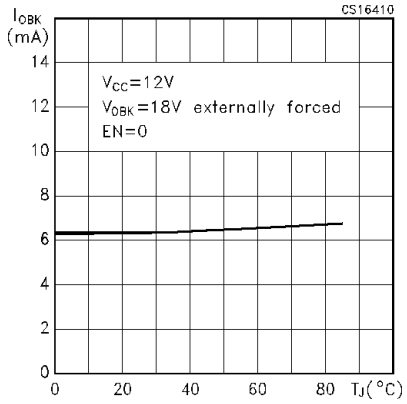


Figure 27. DC/DC Converter Efficiency vs Temperature

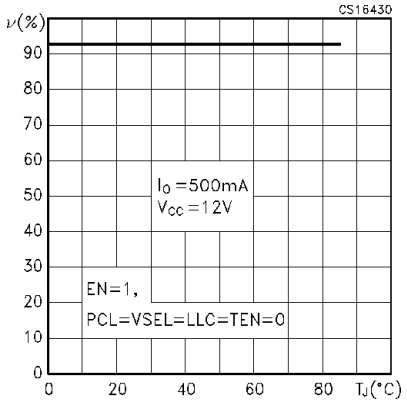


Figure 28. Current Limit Sense Voltage vs Temperature

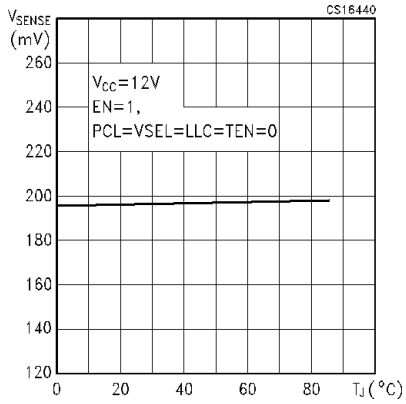
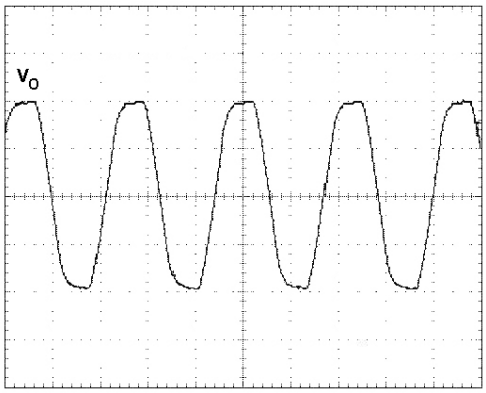
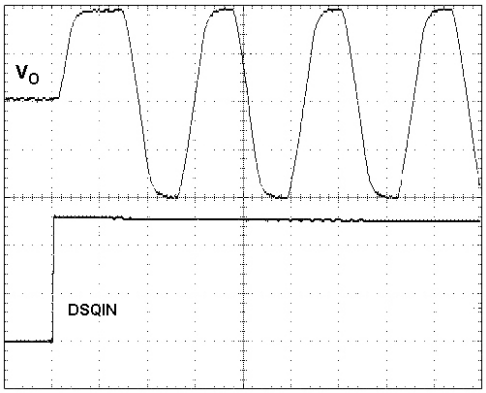


Figure 29. 22kHz Tone Waveform



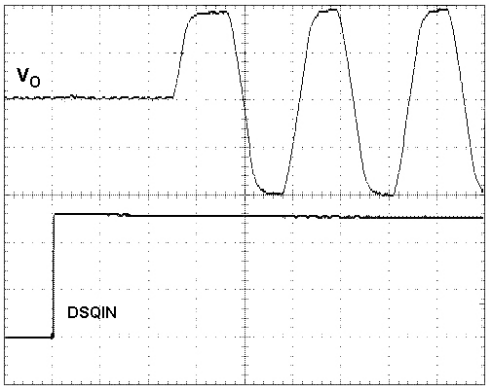
V_{CC}=12V, I_O=50mA, EN=TEN=1

Figure 30. DSQIN Tone Enable Transient Response



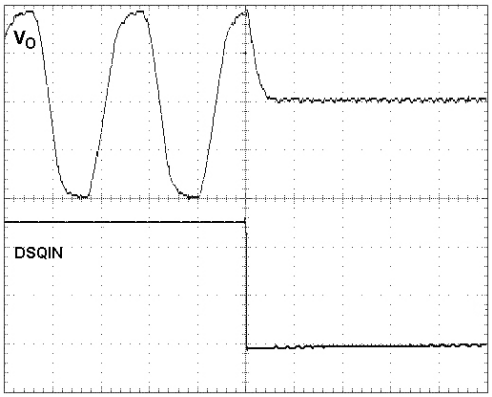
V_{CC}=12V, I_O=50mA, EN=1, Tone enabled by DSQIN Pin

Figure 31. DSQIN Tone Enable Transient Response



V_{CC}=12V, I_O=50mA, EN=1, Tone enabled by DSQIN Pin

Figure 32. DSQIN Tone Disable Transient Response



V_{CC}=12V, I_O=50mA, EN=1, Tone enabled by DSQIN Pin

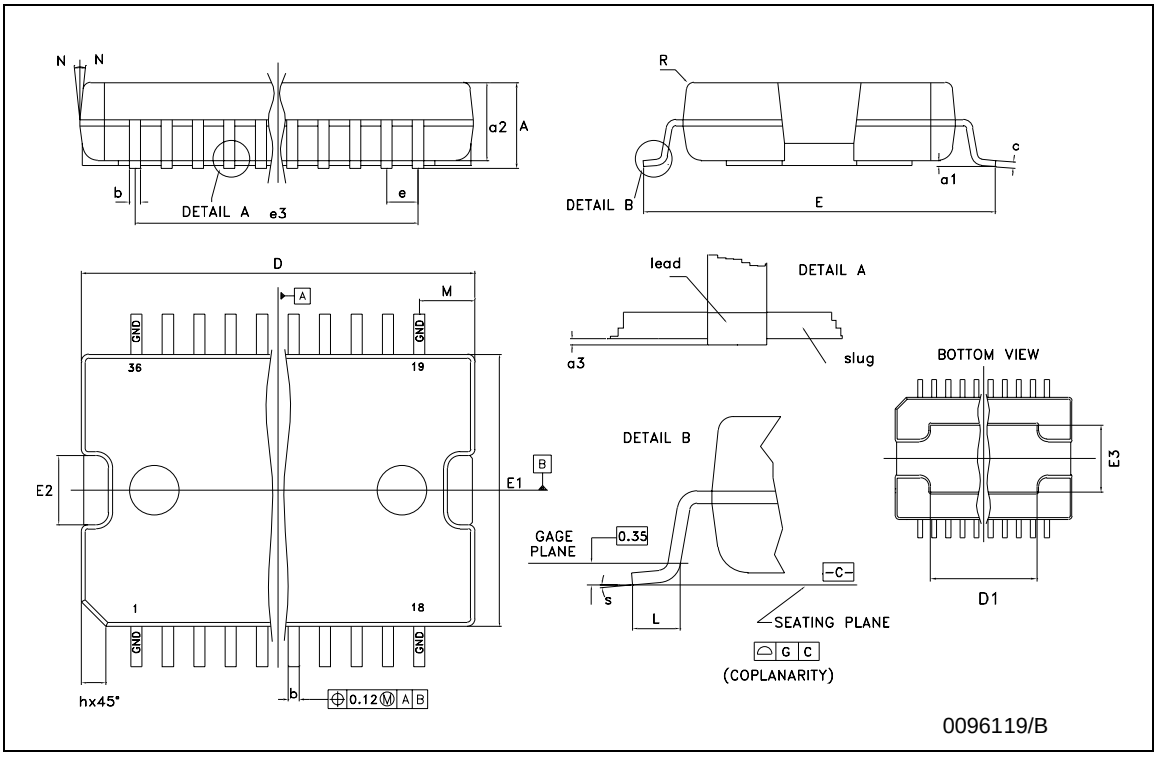
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

PowerSO-36 MECHANICAL DATA

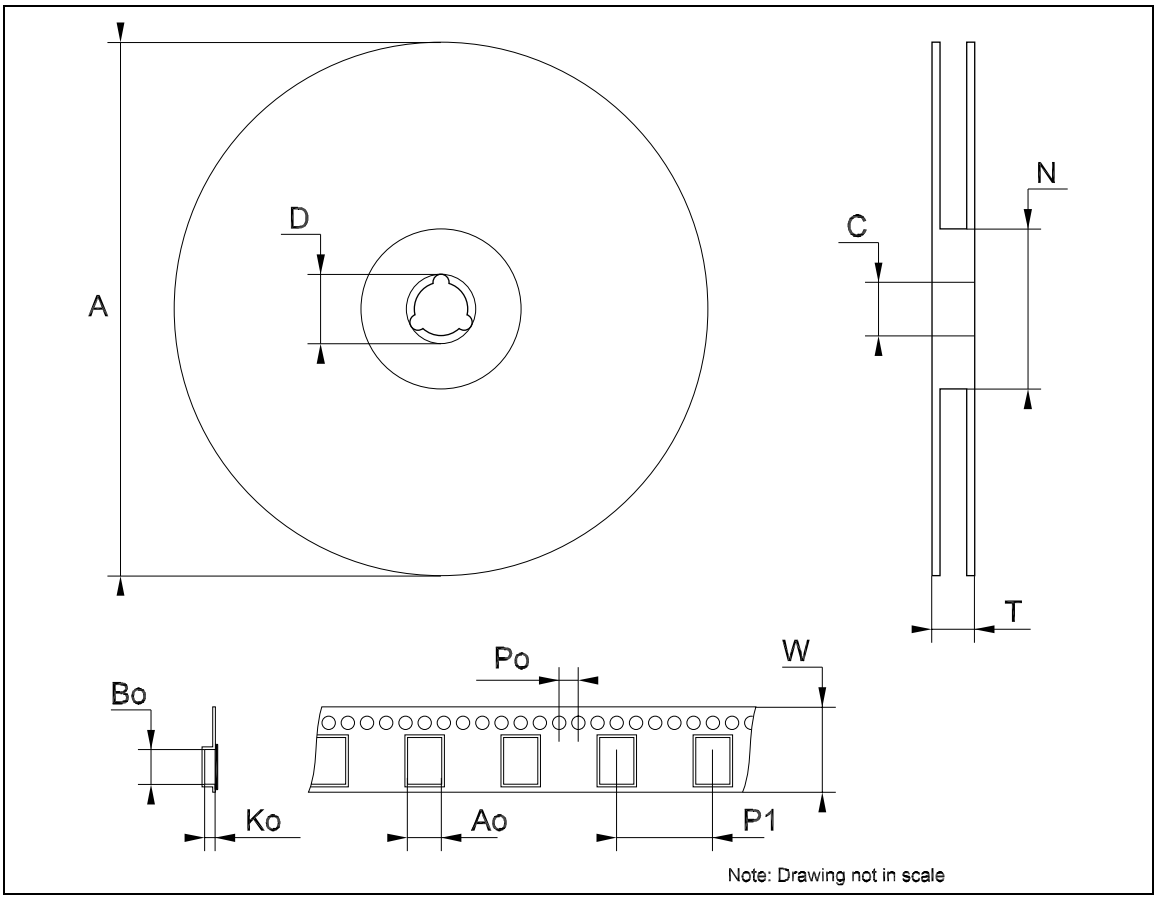
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			3.60			0.1417
a1	0.10		0.30	0.0039		0.0118
a2			3.30			0.1299
a3	0		0.10	0		0.0039
b	0.22		0.38	0.0087		0.0150
c	0.23		0.32	0.0091		0.0126
D (1)	15.80		16.00	0.6220		0.6299
D1	9.40		9.80	0.3701		0.3858
E	13.90		14.50	0.5472		0.5709
E1 (1)	10.90		11.10	0.4291		0.4370
E2			2.90			0.1142
E3	5.8		6.2	0.2283		0.2441
e		0.65			0.0256	
e3		11.05			0.4350	
G	0		0.10	0.0000		0.0039
H	15.50		15.90	0.6102		0.6260
h			1.10			0.0433
L	0.80		1.10	0.0315		0.0433
N			10°			10°
S	0°		8°	0°		8°

(1) “D and E1” do not include mold flash or protusions - Mold flash or protusions shall not exceed 0.15mm (0.00 ”)



Tape & Reel PowerSO-36 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	15.1		15.3	0.594		0.602
Bo	16.5		16.7	0.650		0.658
Ko	3.8		4.0	0.149		0.157
Po	3.9		4.1	0.153		0.161
P	23.9		24.1	0.941		0.949
W	23.7		24.3	0.933		0.957



11 Revision history

Table 8. Document revision history

Date	Revision	Changes
08-Apr-2005	4	Maturity Changed.
23-Feb-2006	5	The *Figure 3.* and *Figure 4.* has been updated.

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