National Semiconductor

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LMV422
Dual Rail-to-Rail Output Operational Amplifier with Power Select

General Description

The LMV422 dual rail-to-rail output amplifier offers a power select pin (PS) that allows the user to select one of two power modes depending on the level of performance desired. This is ideal for AC coupled circuits where the circuit needs to be kept active to maintain a quiescent charge on the coupling capacitors with minimum power consumption.

For portable applications, the LMV422 operates in low power mode consuming only 2 µA of supply current per channel at a bandwidth of 27 kHz. This allows the user to reduce the power consumption of an amplifier while maintaining an active circuit. For additional bandwidth and output current drive the amplifier can be switched to full power mode with 8 MHz bandwidth while consuming only 400 µA per channel.

The LMV422 features a rail-to-rail output voltage swing in addition to an input common mode range that includes ground. The LMV422 is designed for closed loop gains of plus two (or minus one) or greater. The LMV422 is offered in 10-Pin MSOP miniature package to ease the adoption in applications where board area is at a premium.

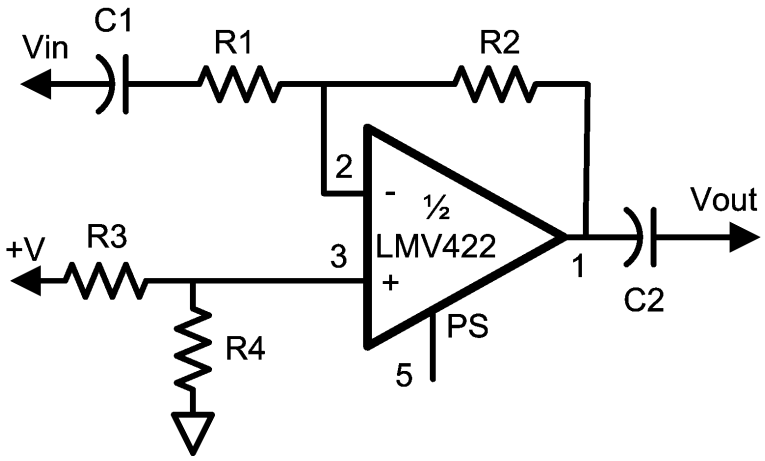
Features

- Supply voltage 2.7V to 5.5V
- Supply current per channel
  - — Low power mode 2 µA
  - — Full power mode 400 µA
- Input common mode voltage range –0.3V to 3.8V
- CMRR 85 dB
- Output voltage swing Rail-to-Rail
- Input offset voltage 1 mV
- Bandwidth
  - — Low power mode 27 kHz
  - — Full power mode 8 MHz
- Stable for $A_V \geq +2$ or $A_V \leq -1$

Applications

- AC coupled circuits
- Portable instrumentation
- Smoke detectors

Typical Application



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AC Coupled Application

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance(Note 2)	
Human Body	2000V
Machine Model	200V
V_{IN} Differential	±2V
Supply Voltage (V^+ - V^-)	2.5V to 5.5V
Storage Temperature Range	−65˚C to +150˚C
Junction Temperature (Note 4)	+150˚C
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering Lead Temp. (10 sec)	260˚C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	2.7V to 5.5V
Temperature Range	−40˚C to +85˚C
Package Thermal Resistance (θ_{JA})	
10-Pin MSOP	210˚C/W

5V Full Power Mode Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, PS = V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1	4 **5.5**	mV
ΔV_{OS}	Input Offset Voltage Difference	V_{OS} in Full Power Mode − V_{OS} in Low Power Mode		0.1	1	mV
TC V_{OS}	Input Offset Average Drift	(Note 9)		2		µV/C
I_B	Input Bias Current			5		pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	68 **60**	85		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	66 **60**	90		dB
CMVR	Input Common Mode Voltage Range	CMRR ≥ 50 dB	−0.3		3.8	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.75V to 4.25V R_L = 1 MΩ	72 **70**	100		dB
		V_O = 0.75V to 4.25V R_L = 10 kΩ	75 **70**	102		
V_O	Output Swing High	R_L = 10 kΩ to V^+/2	4.93 **4.88**	4.97		V
		R_L = 1 MΩ to V^+/2	4.94 **4.89**	4.98		
	Output Swing Low	R_L = 10 kΩ to V^+/2		33	180 **230**	mV
		R_L = 1 MΩ to V^+/2		25	120 **170**	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V V_{ID} = 100 mV	3	5		mA
		Sinking, V_O = 5V V_{ID} = −100 mV	9	16		
I_S	Supply Current Per Channel	PS ≤ 0.5V		400	650 **900**	µA
SR	Slew Rate	V_O = 3V, A_V = +2	1.8	3.8		V/µs
GBW	Gain Bandwidth Product			8		MHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		20		nV/ $\sqrt{Hz}$
		f = 1 kHz		25		

5V Full Power Mode Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, PS = V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
i_n	Input-Referred Current Noise	f = 1 kHz		0.006		pA/$\sqrt{Hz}$
t_{LF}	Time from Low Power Mode to Full Power Mode			210		ns
TH_{PS}	Full Power Mode Voltage Threshold				0.5	V
I_{PS}	Input Current PS pin(Note 7)			–2		µA

5V Low Power Mode Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25˚C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = V^+/2, PS = V^+ or Open. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1	4 **5.5**	mV
ΔV_{OS}	Input Offset Voltage Difference	V_{OS} in Full Power Mode – V_{OS} in Low Power Mode		0.1	1	mV
TC V_{OS}	Input Offset Average Drift	(Note 9)		2		µV/C
I_B	Input Bias Current			5		pA
CMRR	Common Mode Rejection Ratio	V_{CM} Stepped from 0V to 3.5V	60 **55**	82		dB
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	62 **60**	90		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	0		3.5	V
A_{VOL}	Large Signal Voltage Gain	R_L = 1 MΩ V_O = 0.75 to 4V	62 **54**	72		dB
V_O	Output Swing High	R_L = 1 MΩ	4.94 **4.89**	4.98		V
	Output Swing Low	R_L = 1 MΩ		150	200 **250**	mV
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V V_{ID} = 200 mV	40	140		µA
		Sinking, V_O = 5V V_{ID} = –200 mV	25	130		
I_S	Supply Current per channel	PS ≥ 4. 5V		2	3.5 **4.5**	µA
SR	Slew Rate	V_O = 3V, A_V = +2	8	14		V/ms
GBW	Gain Bandwidth Product			27		kHz
e_n	Input-Referred Voltage Noise	f = 100 kHz		40		nV/$\sqrt{Hz}$
		f = 1 kHz		60		
i_n	Input-Referred Current Noise	f = 1 kHz		0.06		pA/$\sqrt{Hz}$
t_{FL}	Time from Full Power Mode to Low Power Mode			500		ns
TH_{PS}	Low Power Mode Voltage Threshold		4.5			V
I_{PS}	Input Current PS pin (Note 7)			8		nA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF, Machine Model, 0Ω in series with 200 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

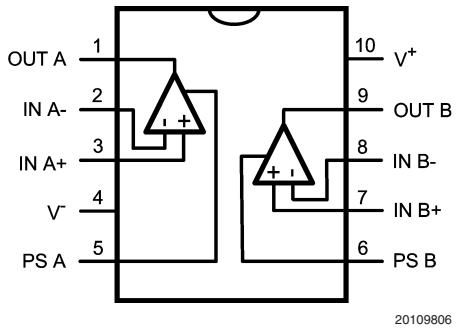
Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the average of the rising and falling slew rates.

Note 9: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

Connection Diagram

10-Pin MSOP

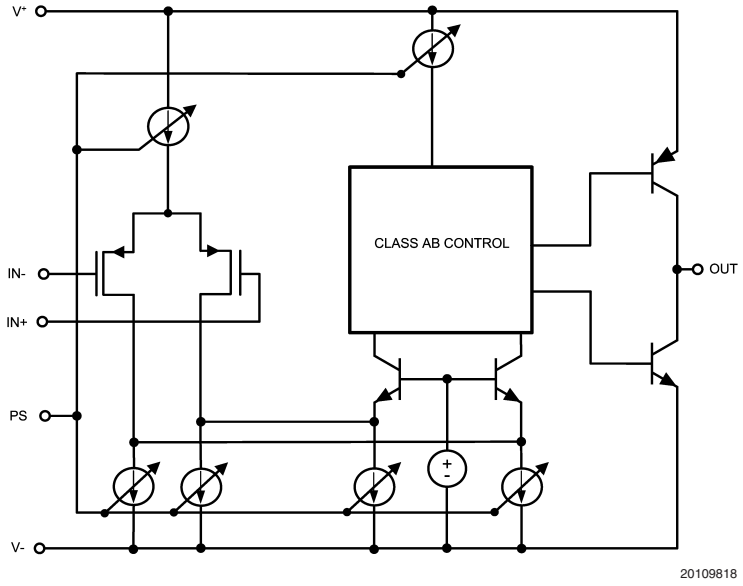


Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
10-Pin MSOP 3 x 5 mm	LMV422MM	AJ1A	1k Units Tape and Reel	MUB10A
	LMV422MMX		3.5k Units Tape and Reel	

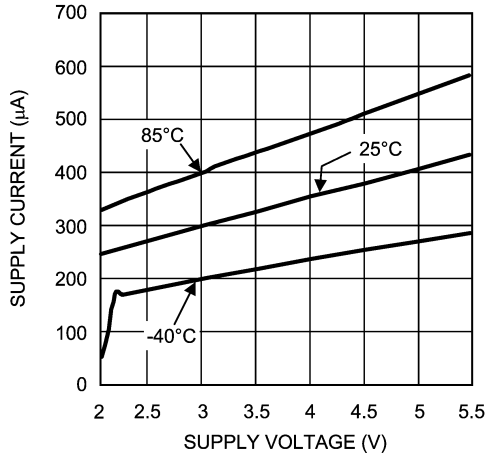
Simplified Schematic



Typical Performance Characteristics

Unless otherwise specified, V^+ = 5V, T_A = 25˚C, PS = V^+ for Full Power Mode, PS = V^- for Low Power Mode.

Supply Current vs. Supply Voltage per Channel (Full Power Mode)



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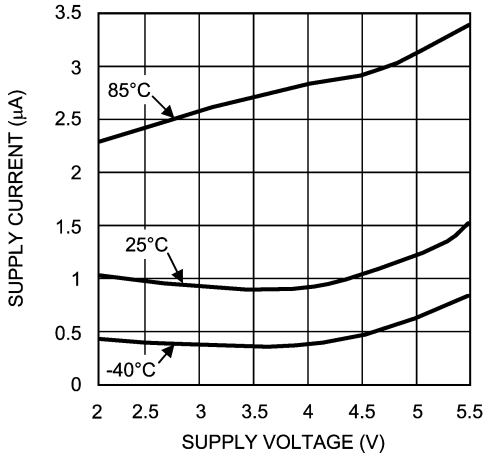
Supply Current vs. Supply Voltage per Channel (Low Power Mode)



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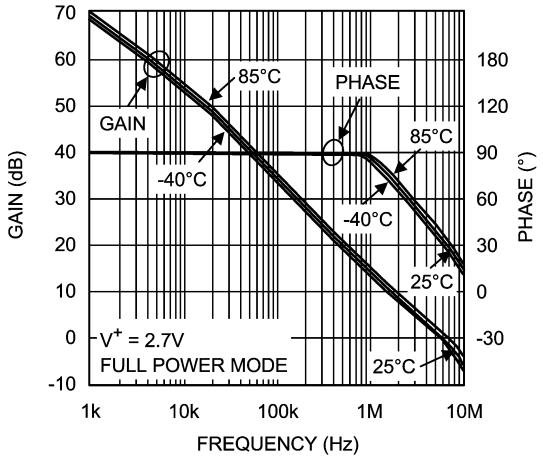
Gain and Phase vs. Frequency



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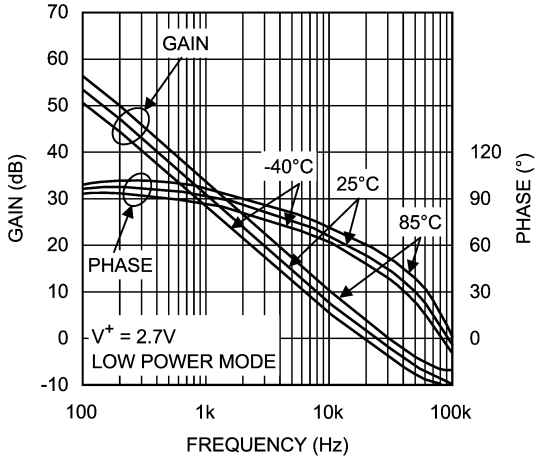
Gain and Phase vs. Frequency



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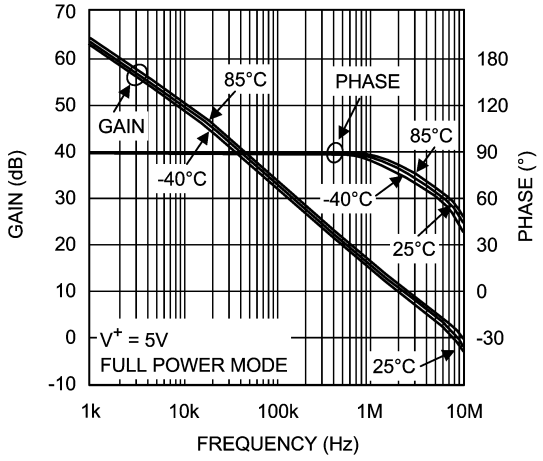
Gain and Phase vs. Frequency



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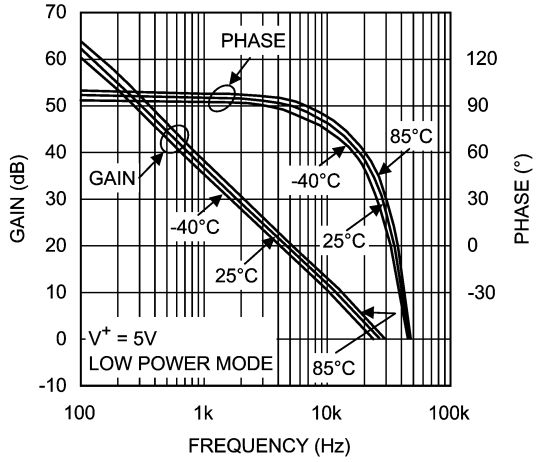
Gain and Phase vs. Frequency



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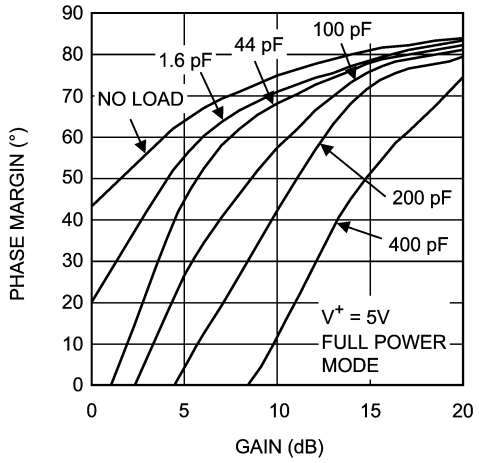
Typical Performance Characteristics Unless otherwise specified, V^+ = 5V, T_A = 25˚C, PS = V^+ for Full Power Mode, PS = V^- for Low Power Mode. (Continued)

Phase Margin vs. Gain for Various Capacitive Load



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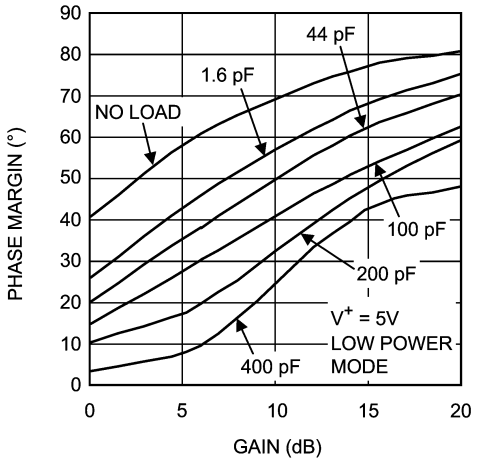
Phase Margin vs. Gain for Various Capacitive Load



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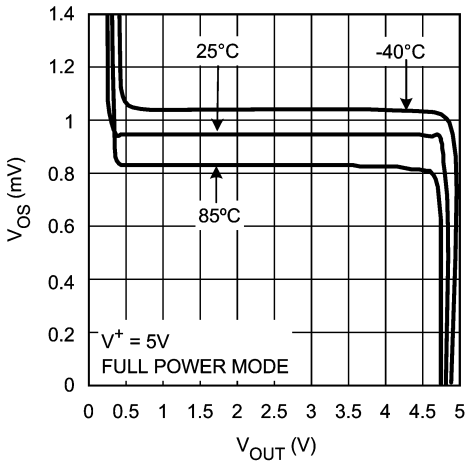
Input Offset Voltage vs. Output Voltage



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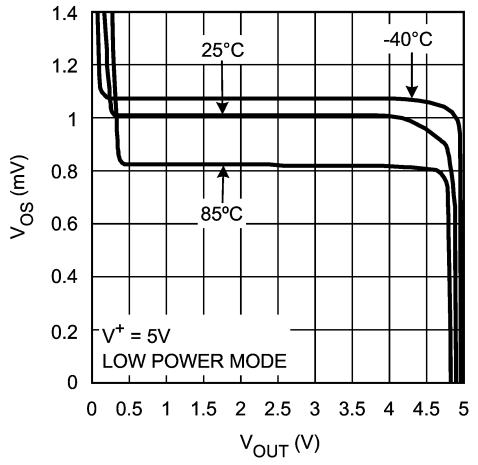
Input Offset Voltage vs. Output Voltage



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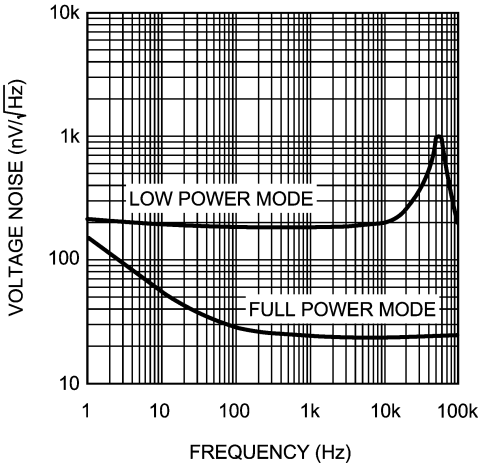
Noise vs. Frequency



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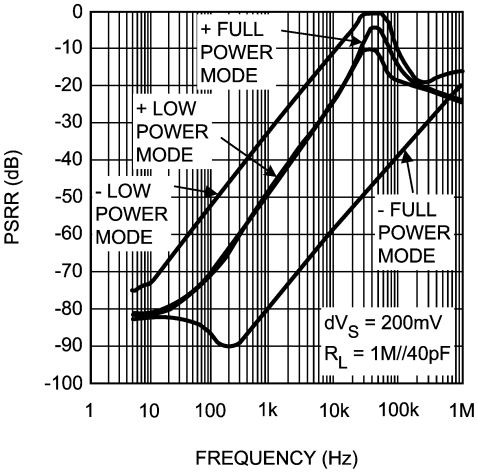
PSRR vs. Frequency



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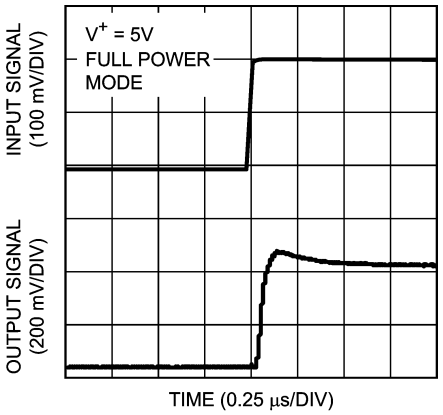
Typical Performance Characteristics Unless otherwise specified, V^+ = 5V, T_A = 25˚C, PS = V^+ for Full Power Mode, PS = V^- for Low Power Mode. (Continued)

Small Signal Non-Inverting Response



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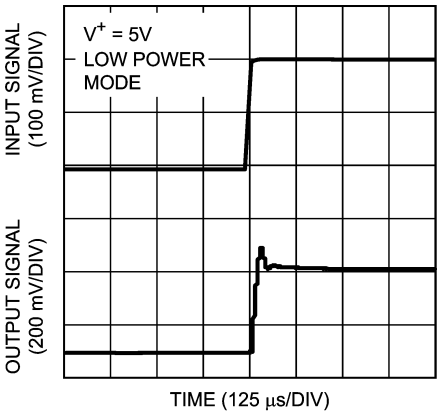
Small Signal Non-Inverting Response



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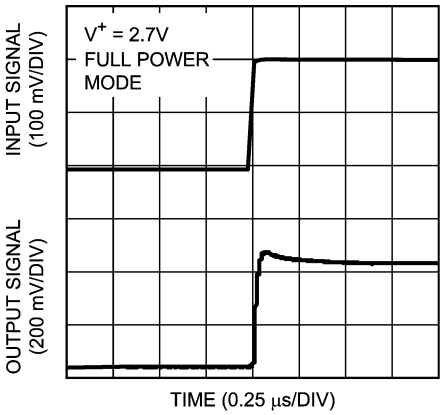
Small Signal Non-Inverting Response



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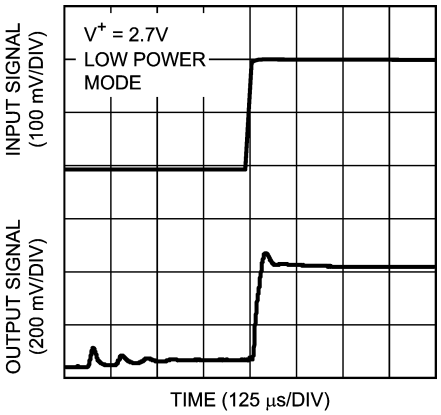
Small Signal Non-Inverting Response



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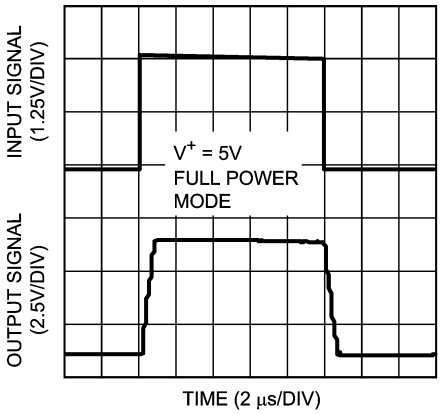
Large Signal Non-Inverting Response



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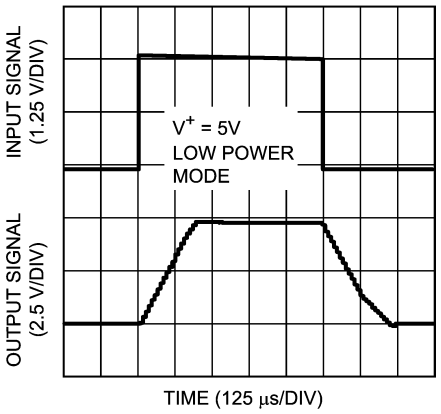
Large Signal Non-Inverting Response



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Application Information

The LMV422 is a dual rail-to-rail output amplifier that can be switched between two active power modes. The power select pin (PS) provides a method to optimize the power consumption, bandwidth and short circuit current. When the PS pin is set to greater than 4.5V (*Figure 1a*) or left open, the LMV422 is in Low Power Mode operating at a bandwidth of 27 kHz and consuming only 2 µA of supply current per channel. Setting the PS pin to less than 0.5V, switches the LMV422 to Full Power Mode with a bandwidth of 8 MHz and supply current of 400 uA per channel (*Figure 2b*).. The PS pin should not exceed the supply voltage. The active power modes of the two amplifiers can be set independently.

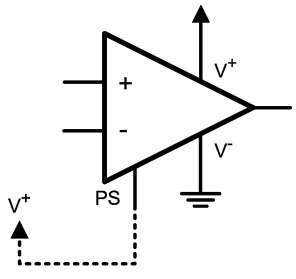


Figure 1a Low Power Mode

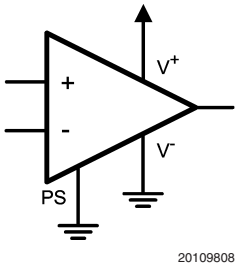


Figure 1b Full Power Mode

FIGURE 1.

The LMV422 PS pin has an internal pull up and a logic level control gate that makes it easy for the PS pin to be controlled by the output of a logic gate or the output pin of a microcontroller. The following figures show the three typical output configurations for logic gates and microcontrollers.

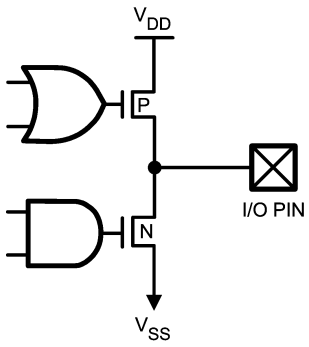


Figure 2a

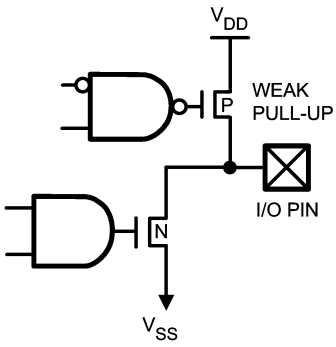


Figure 2b

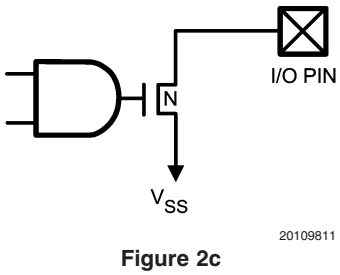


Figure 2c

FIGURE 2.

CAPACITIVE LOAD TOLERANCE

The LMV422 is optimized for maximum bandwidth when operating at a minimum closed loop gain of +2 or –1, therefore, it is not recommended to be configured as a buffer. Like many other op amps, the LMV422 may oscillate when the applied load appears capacitive. The threshold of the oscillation varies both with load and circuit gain (see Phase Margin vs. Gain for various capacitive loads curves). The load capacitance interacts with the amplifier's output resistance to create an additional pole. If this pole frequency is too low, it will degrade the amplifier's phase margin so that the amplifier is no longer stable.

Figure 3a and 3b show the addition of a small value resistor R_{ISO} or R_X (50Ω to 100Ω) in series with the op amps output. *Figure 3b* shows the addition of a capacitor C_F (5 pF to 10 pF) between the inverting input and the output pin. This addition capacitor returns the phase margin to a safe value without interfering with lower frequency circuit operation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

Application Information (Continued)

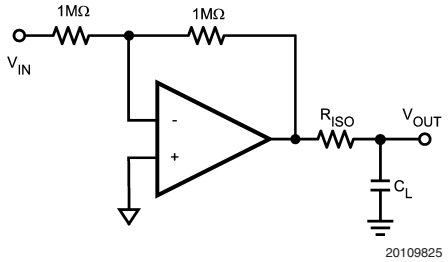


Figure 3a

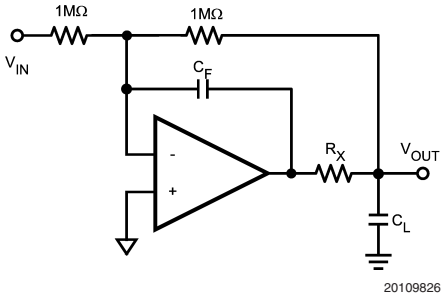


Figure 3b

FIGURE 3.

AC COUPLED CIRCUITS

The two power modes makes the LMV422 ideal for AC coupled circuit where the circuit needs to be kept active to maintain a quiescent charge on the coupling capacitors with minimum power consumption.

Figure 4 shows a schematic of an inverting and non-inverting AC coupled amplifiers using the LMV422 with the PS pins controlled by I/O ports of a microcontroller.

The advantage of the low power active mode for AC coupled amplifiers is the elimination of the time needed to re-establish a quiescent operating point when the amplifier is switched to a full power mode. When amplifiers without a low power active mode are used in low power applications, there are two ways to minimize power consumption. The first is turning off the amplifiers by switching off power to the op amps using a transistor switch. The second is using an amplifier with a shut down pin. Both of these methods have the problem of allowing the coupling capacitors, C1, C2, C3, C4, and C5, to discharge the quiescent DC voltage stored on them when placed in the shut down state. When the amplifiers are turned on again, the quiescent DC voltages must reestablish themselves. During this time, the amplifier's output is not usable because the output signal is a mixture of the amplified input signal and the charging voltage on the coupling capacitors. The settling time can range from a several milliseconds to several seconds depending on the resistor and capacitor values.

When the LMV422 is placed into the low power mode the power consumption is minimal but the amplifier is active to maintain the quiescent DC voltage on the coupling capacitors and the transition back to the operational high power mode is fast, within few hundred nanoseconds. The active low power mode of the LMV422 separates the two critical aspects of a low power AC amplifier design. The values of the gain resistors, bias resistors, and coupling capacitors can be chosen independently of the turn on and stabilization time.

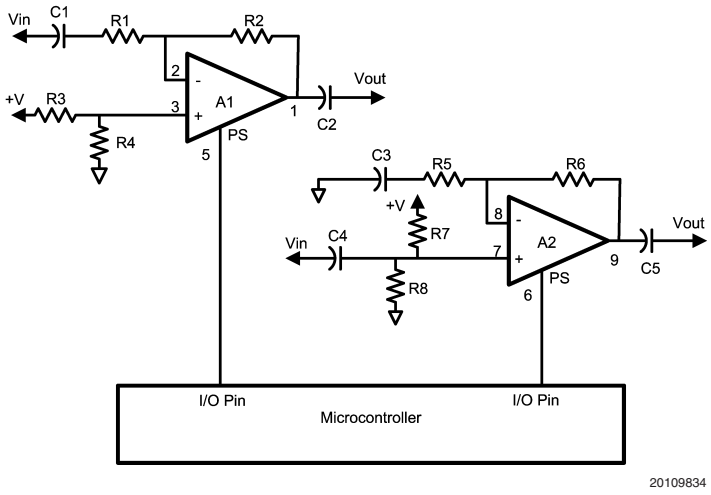
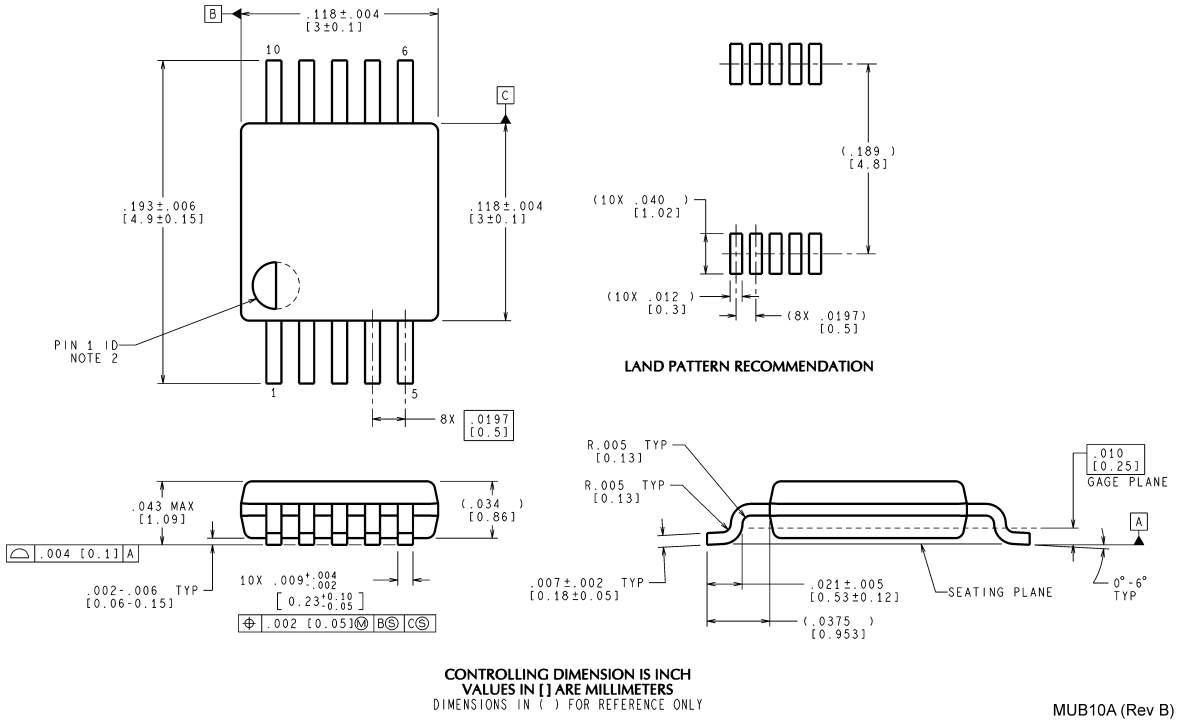


FIGURE 4.

RESISTIVE LOAD

The LMV422 has a minimum current drive of 3 mA in full power mode. The minimum resistive load should be 10 kΩ The current drive in the low power mode is 140 uA, the minimum resistive load should be 100 kΩ.

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MUB10A (Rev B)

10-Pin MSOP
NS Package Number MUB10A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

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