CMOS 4-BIT MICROCONTROLLER

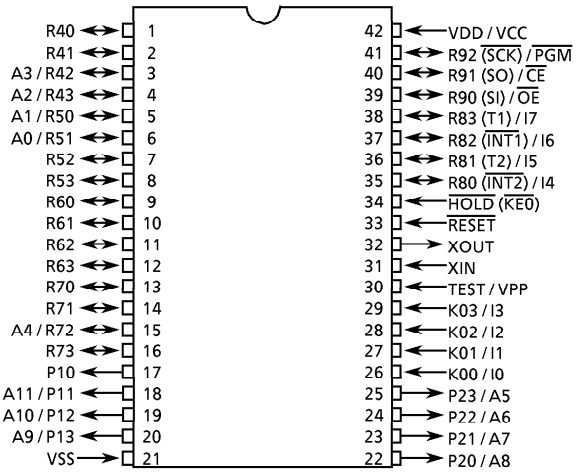
TMP47P400VN
TMP47P400VF

The 47P400V is the system evaluation LSI of 47C200B/400B with 32K bits one-time PROM. The 47P400V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764AD.
In addition, the 47P400V and the 47C200B/400B are pin compatible. The 47P400V operates as the same as the 47C200B/400B by programming to the internal PROM.

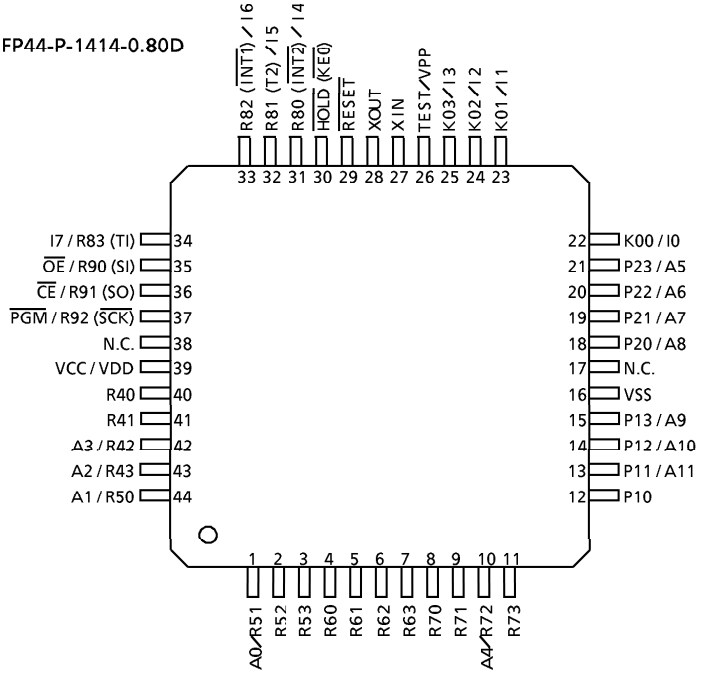
PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P400VN	OTP 4096 × 8-bit	256 × 4-bit	SDIP42-P-600-1.78	BM1118
TMP47P400VF			QFP44-P-1414-0.80D	BM1125

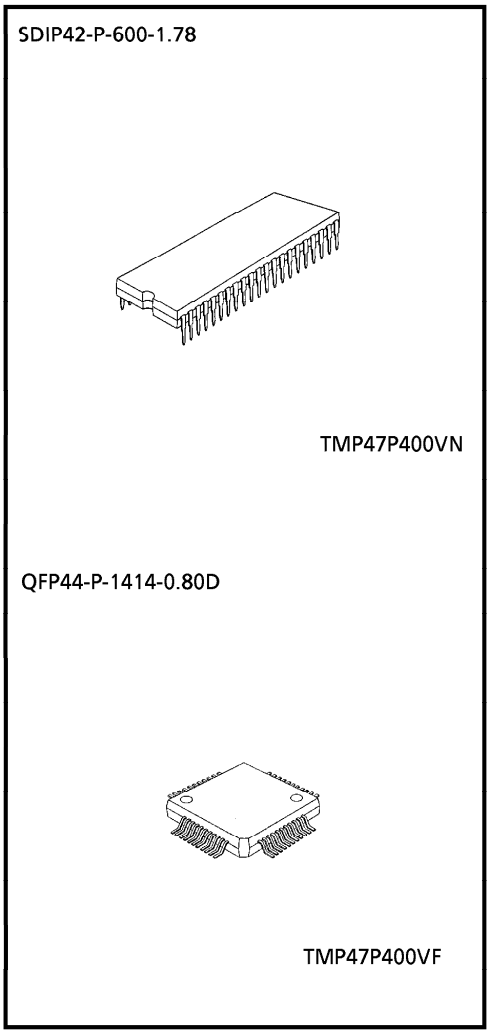
PIN ASSIGNMENT (TOP VIEW)

SDIP42-P-600-1.78



QFP44-P-1414-0.80D





PIN FUNCTION

The 47P400V has MCU mode and PROM mode.

(1) MCU mode

The 47C200B/400B and the 47P400V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	Input/Output	FUNCTIONS	PIN NAME (MCU MODE)
A11 to A9	Input	Address inputs	P11 to P13
A8 to A5			P20 to P23
A4			R72
A3 , A2			R42 , R43
A1 , A0			R50 , R51
I7 to I4	I/O	Data inputs / outputs	R83 to R80
I3 to I0			K03 to K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
VSS		0 V	VSS
P10	Output	Open or Be fixed to low level.	
R41 , R40	I/O	Be fixed to low level	
R53 , R52			
R63 to R60			
R70, R71, R73			
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins.	
XOUT	Output		

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P400V.
The 47P400V is the same as the 47C200B/400B except that an OTP is used instead of a Mask ROM.

1. OPERATION MODE

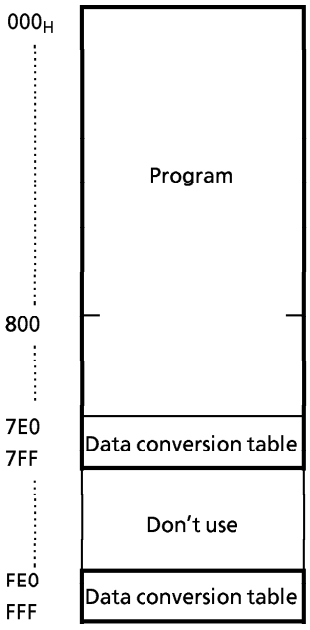
The 47P400V has an MCU mode and a PROM mode.

1.1 MCU Mode

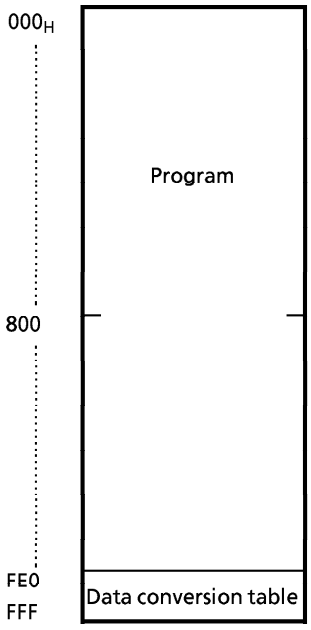
The MCU mode is set by fixing the TEST / VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C200B/400B, except that the TEST / VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C200B/400B. Data conversion tables must be set in two locations when using the 47P400V to check 47C200B operation.

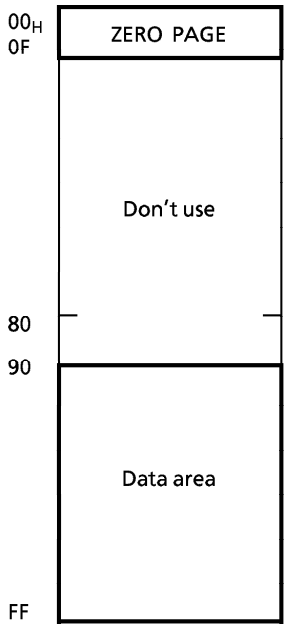


(a) 47C200B



(b) 47C400B

Figure 1-1. Program area (RAM)



(In case of 47C200B)

Figure 1-2. Shared RAM address (RAM)

1.1.2 Data Memory

The 47P400V has 256 × 4-bit data memory. When using the 47P400V as a 47C200B evaluator, programing should be performed assuming that the RAM is assigned to addresses 00 to $0F_H$ and 90 to FF_H as show in figure 1-2 by considering the application software evaluation.

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C200B/400B except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P400V is the same as I/O code FA of the 47C200B/400B.
External resistance, for example, is required when using as evaluator of other I/O codes (FB to FF) (Refer to Figure 1-3).

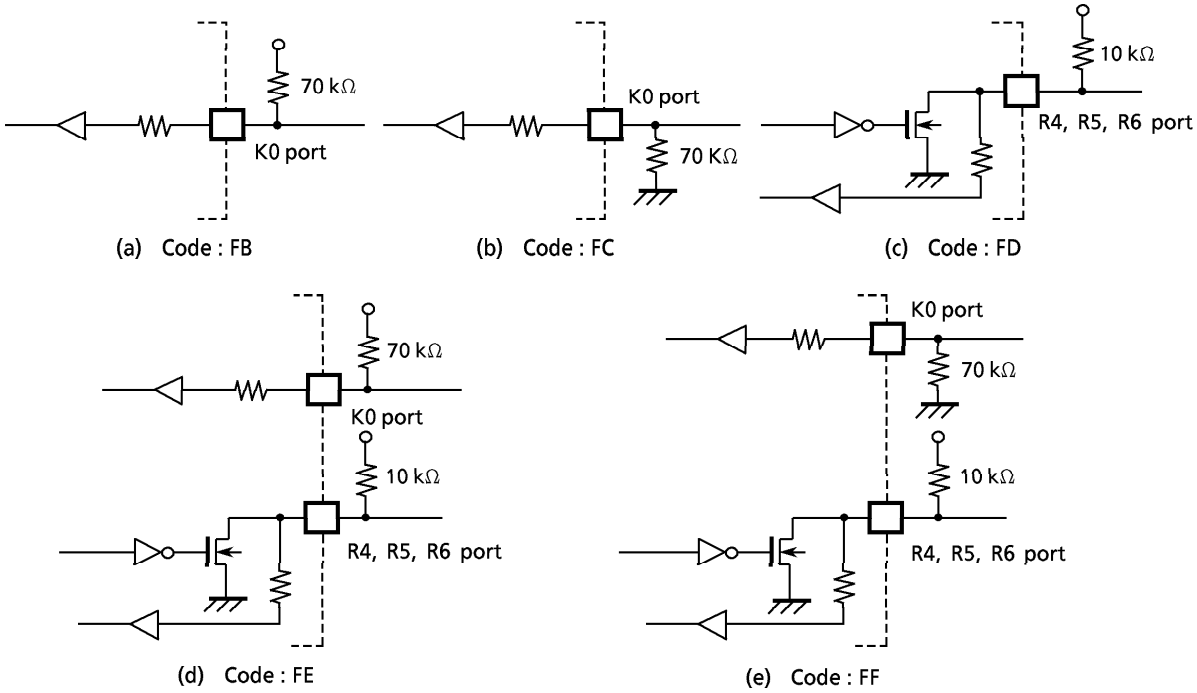
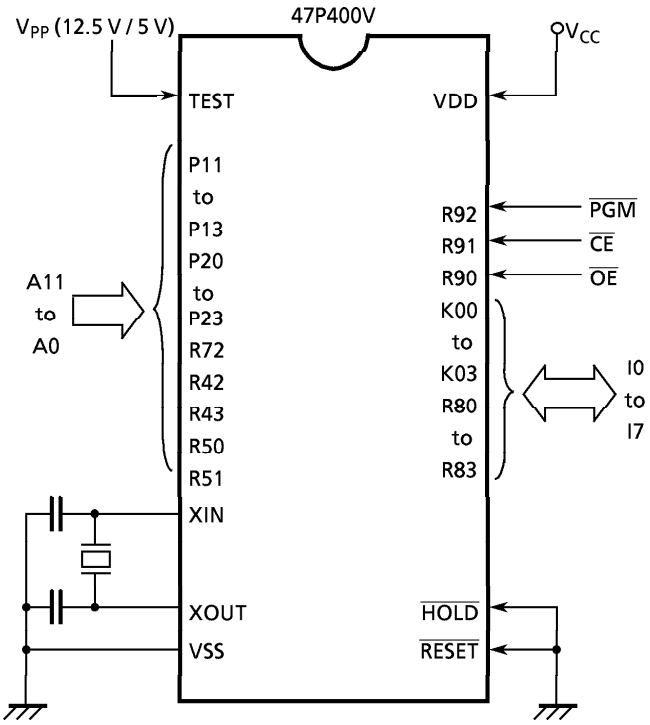


Figure 1-3. I/O code and external circuitry

1.2 PROM Mode

The PROM mode is set by setting the $\overline{RESET}$, $\overline{HOLD}$, pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM2764AD).



For more information on pins refer to the section on pin function.

Note. When writing a program, set a ROM type to 2764AD (programming voltage : 12.5V).
Since the 47P400B has 4096×8 bit internal PROM (000 to FFFH), set a stop address of a PROM writer to "FFFH", or store the same data to the latter half addresses 1000 to 1FFFH.

Figure 1-4. Setting for PROM mode

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5 V) is applied to the Vpp terminal with Vcc = 6 V and $\overline{PGM} = V_{IH4}$. The programming is achieved by applying a Single TTL low level 1 msec, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using program Verify Mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5 V.

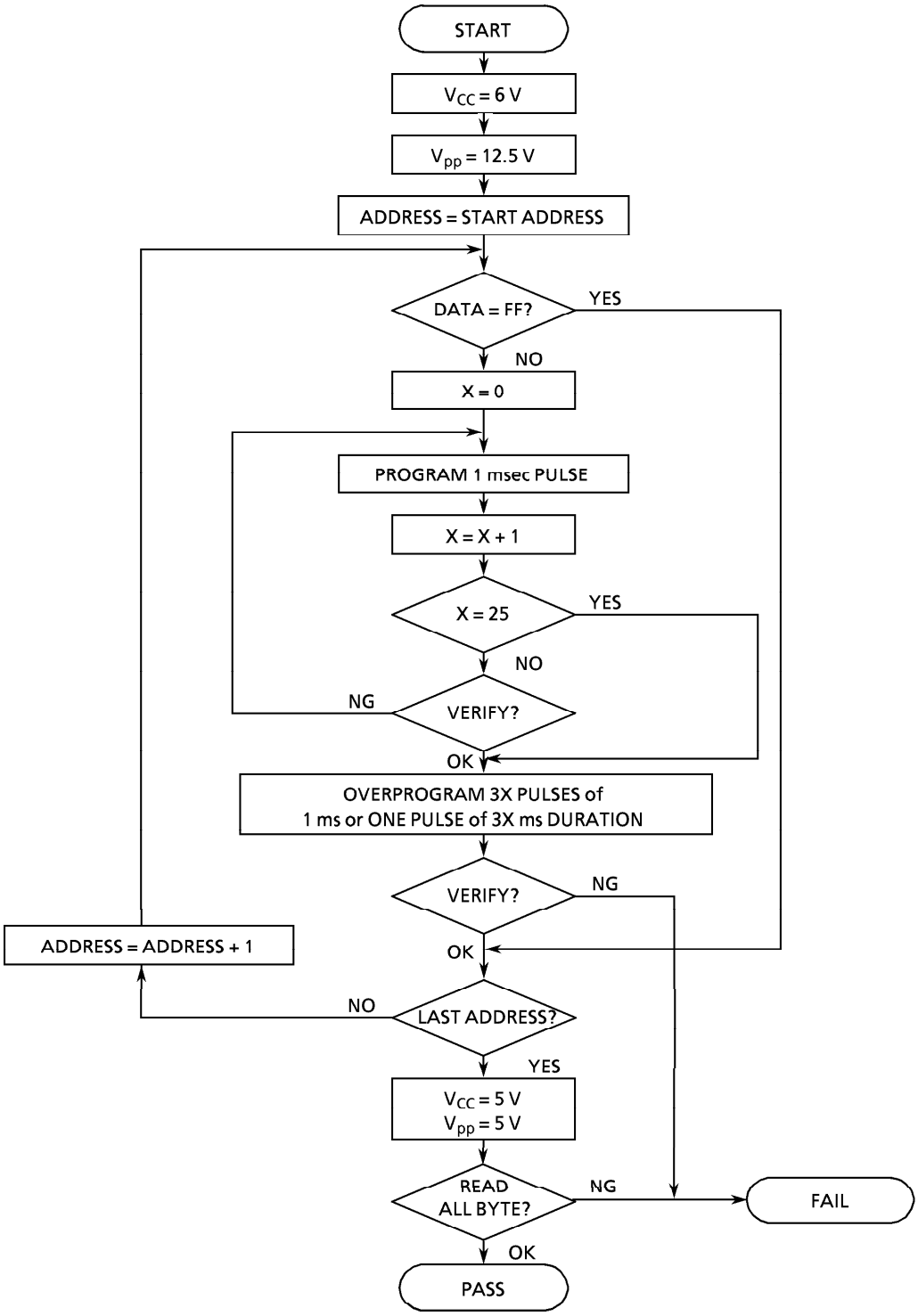


Figure1-5. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST/VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R8	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R8	– 0.3 to 10	
Output Current (per 1 pin)	I_{OUT1}	P1, P2	30	mA
	I_{OUT2}	R4 to R9	3.2	
Output Current (total all pin)	ΣI_{OUT1}	P1, P2	120	mA
Power Dissipation [Topr = 70°C]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	2.7	6.0	V
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc		V_{DD} = 2.7 to 6.0 V	0.4	4.2	MHz

D.C. CHARACTERISTICS

(V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Port R (open drain)					
Input Low Current	I_{IL}	Port R (push-pull)	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	– 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Ports P, R (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output High Voltage	V_{OH}	Port R (push-pull)	V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT, Port P	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL1}	Port P	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	30	—	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V fc = 4 MHz	—	2	4	mA
			V_{DD} = 3.0 V fc = 4 MHz	—	1	2	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ.values show those at T_{opr} = 25 °C, V_{DD} = 5 V.

Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up / pull-down resistor is contained.

Note 3. Supply Current : V_{IN} = 5.3 V / 0.2 V (V_{DD} = 5.5 V), 2.8 / 0.2 v (V_{DD} = 3.0 V)

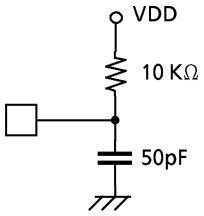
A.C. CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 70 °C)

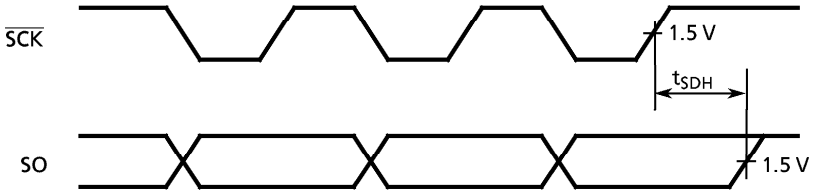
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	tcy		1.9	–	20	μs
High Level Clock Pulse Width	t_{WCH}	External clock mode	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		0.5tcy – 300	–	–	ns

Note. Shift Data Hold Time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmisson)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, T_{opr} = – 30 to 70 °C)

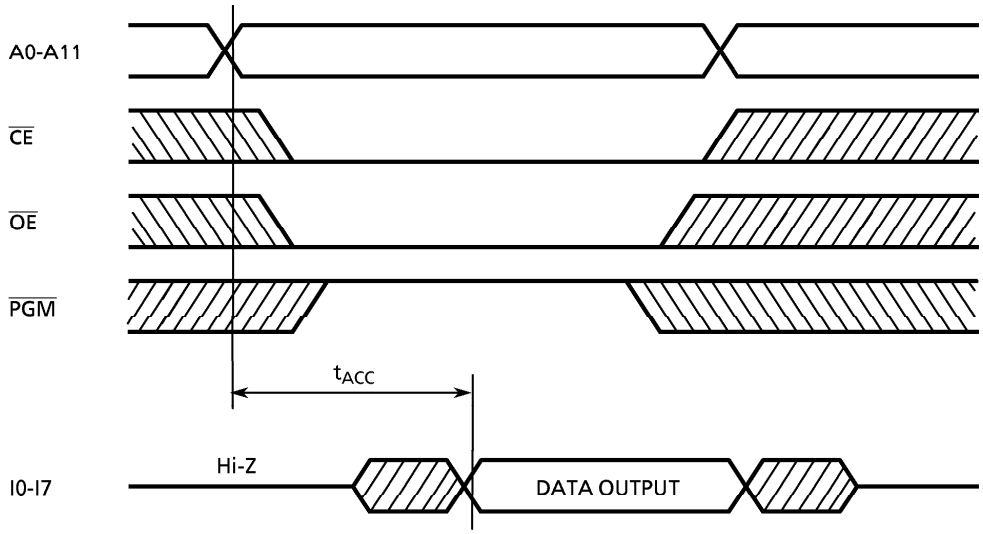
Recommended oscillating conditions of the 47P400V are equal to the 47C200B/400B's.

D.C./A.C. CHARACTERISTICS (PROM mode)

(V_{SS} = 0 V)

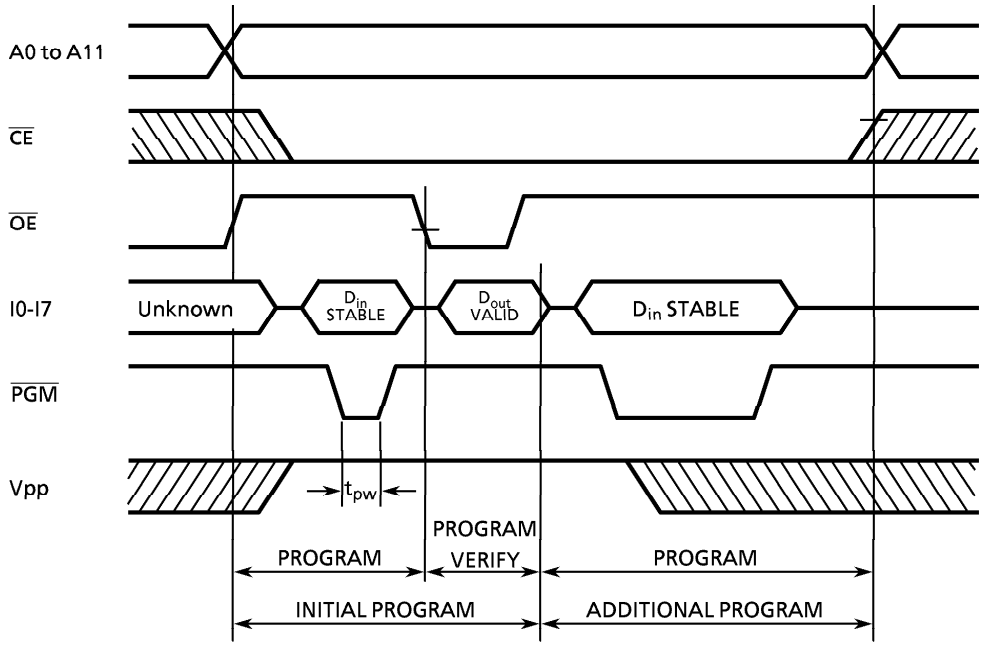
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.3	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	V_{CC} = 6.0 ± 0.25 V	0.95	1.0	1.05	ms



TYPICAL CHARACTERISTICS