TOSHIBA

TOSHIBA Original CMOS 4-Bit Microcontroller

TLCS-47 Series

TMP47C241NG
TMP47C241MG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP47C241N	P-SDIP28-400-1.78	TMP47C241NG	SDIP28-P-400-1.78	TMP47P241VNG
TMP47C241M	P-SOP28-450-1.27	TMP47C241MG	SOP28-P-450-1.27B	TMP47P241VMG

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
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  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

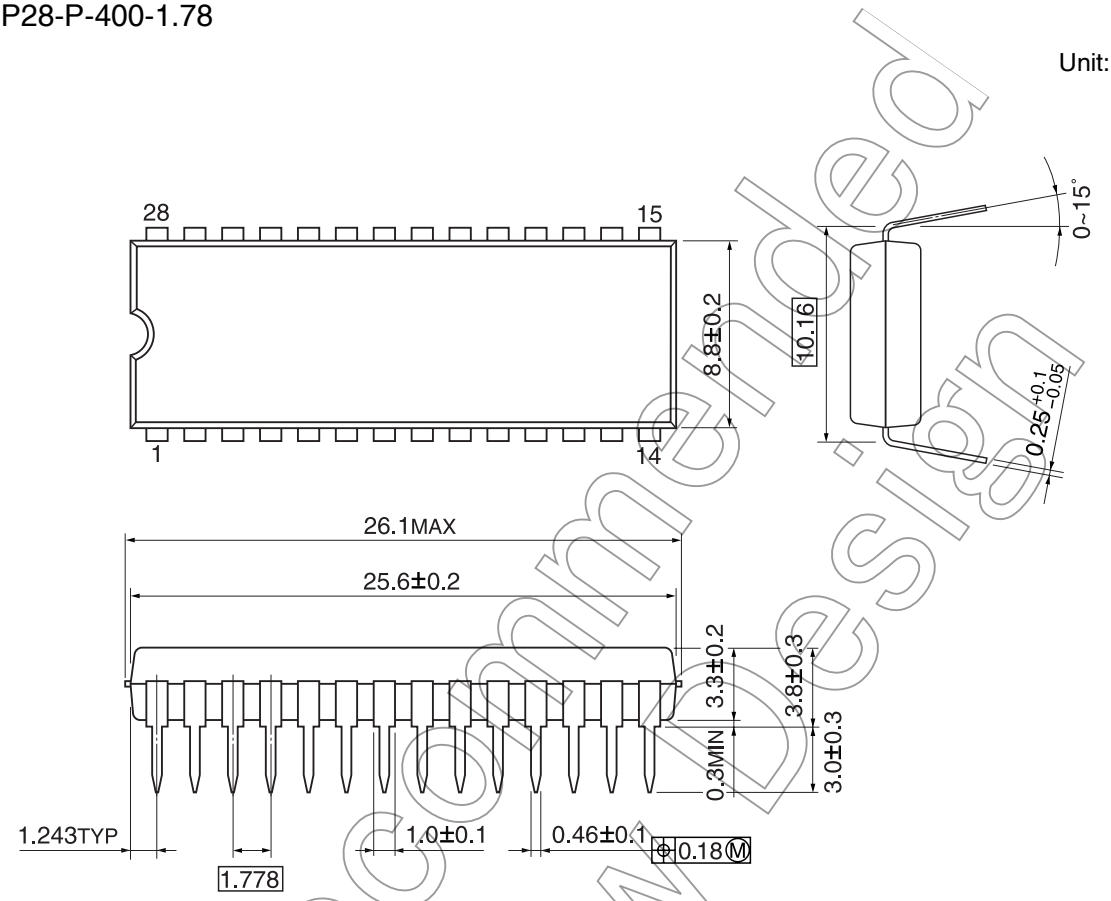
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

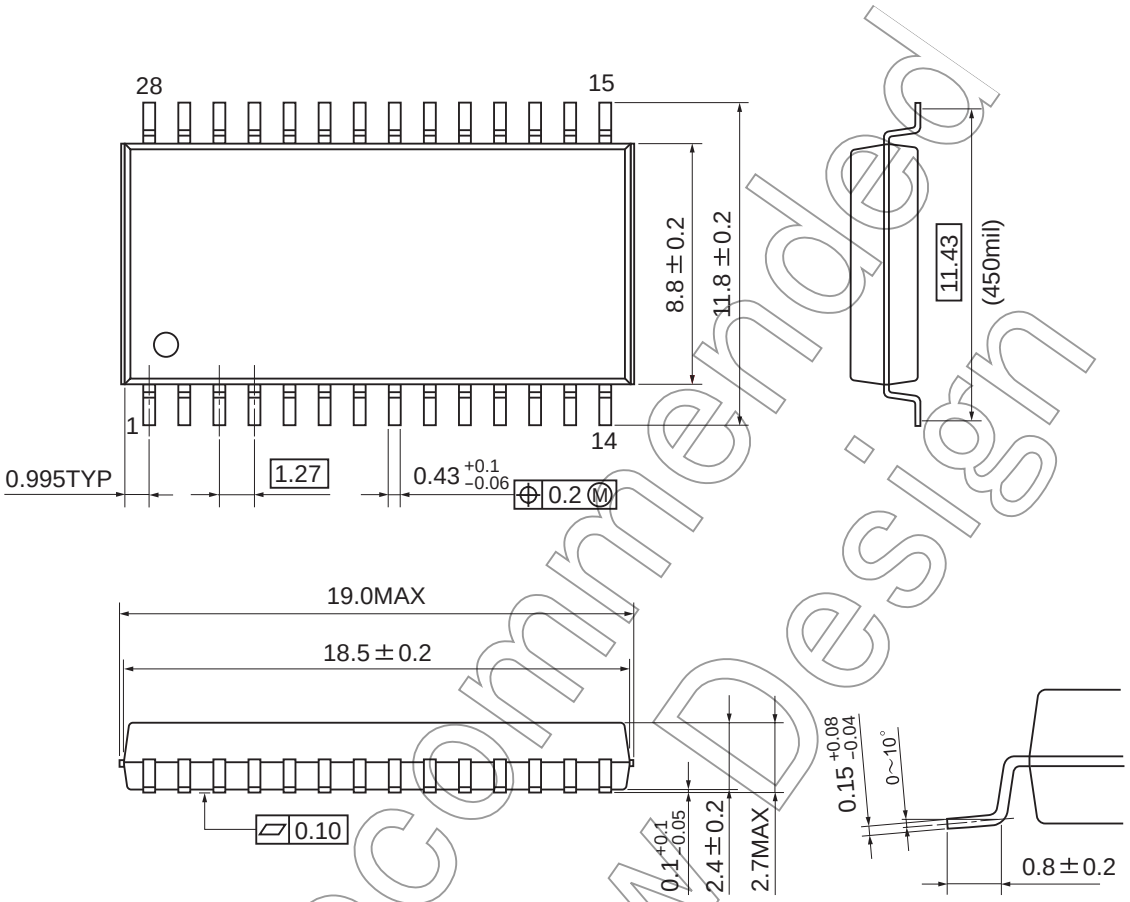
SDIP28-P-400-1.78

Unit: mm



SOP28-P-450-1.27B

Unit: mm



Note: Palladium plated

CMOS 4-Bit Microcontroller

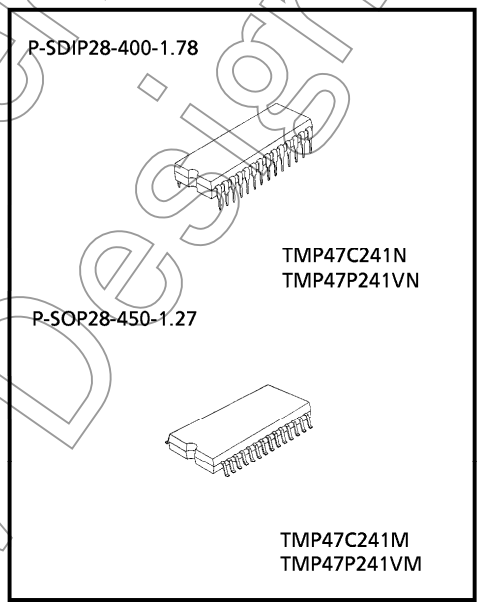
TMP47C241N
TMP47C241M

The TMP47C241 are high speed and high performance 4-bit single chip micro computers, integrating 8-bit AD converter, watchdog timer and serial Interface based on the TLCS-47 series.

Part No.	ROM	RAM	Rackage	OTP
TMP47C241N	2048 × 8-bit	128 × 4-bit	P-SDIP28-400-1.78	TMP47P241VN
TMP47C241M			P-SOP28-450-1.27	TMP47P241VM

Features

◆4-bit single chip microcomputer
◆Instruction execution time: 1.3 μs (at 6 MHz)
◆Low voltage operation: 2.7 V (at 4.2 MHz)
◆90 basic instructions
  ●Table look-up instructions
◆Subroutine nesting: 15 levels max
◆6 interrupt sources (External: 2, Internal: 4)
  All sources have independent latches each, and multiple interrupt control is available
◆I/O port (21 pins)
  - Input 2 ports 5 pins
  - Output 2 ports 5 pins
  - I/O 4 ports 11 pins
◆Two 12-bit Timer / Counters
  Timer, event counter, and pulse width measurement mode
◆Interval timer
◆Watchdog Timer
◆Serial Interface with 4-bit buffer
  External / internal clock, and leading / trailing edge shift mode



000707EBA1

◆8-bit successive approximate type AD converter
(With sample and hold)
- 4 analog inputs
- Converting time: 48 μs (4 MHz)

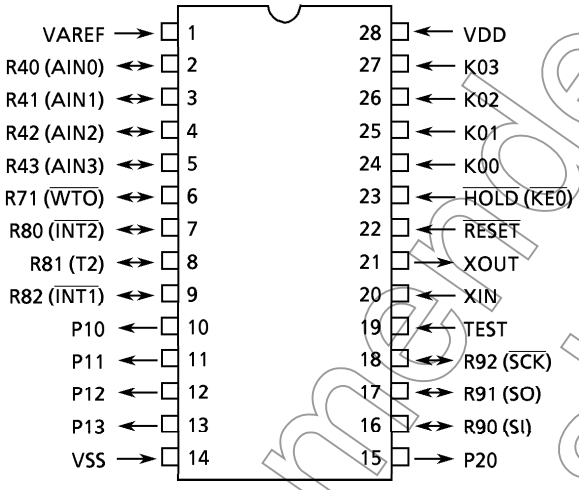
◆High current outputs
LED direct drive capability: typ. 20 mA × 5 bits (Ports P1, P2)
typ. 7 mA × 3 bits (Port R9)

◆Hold function
Battery / Capacitor back-up

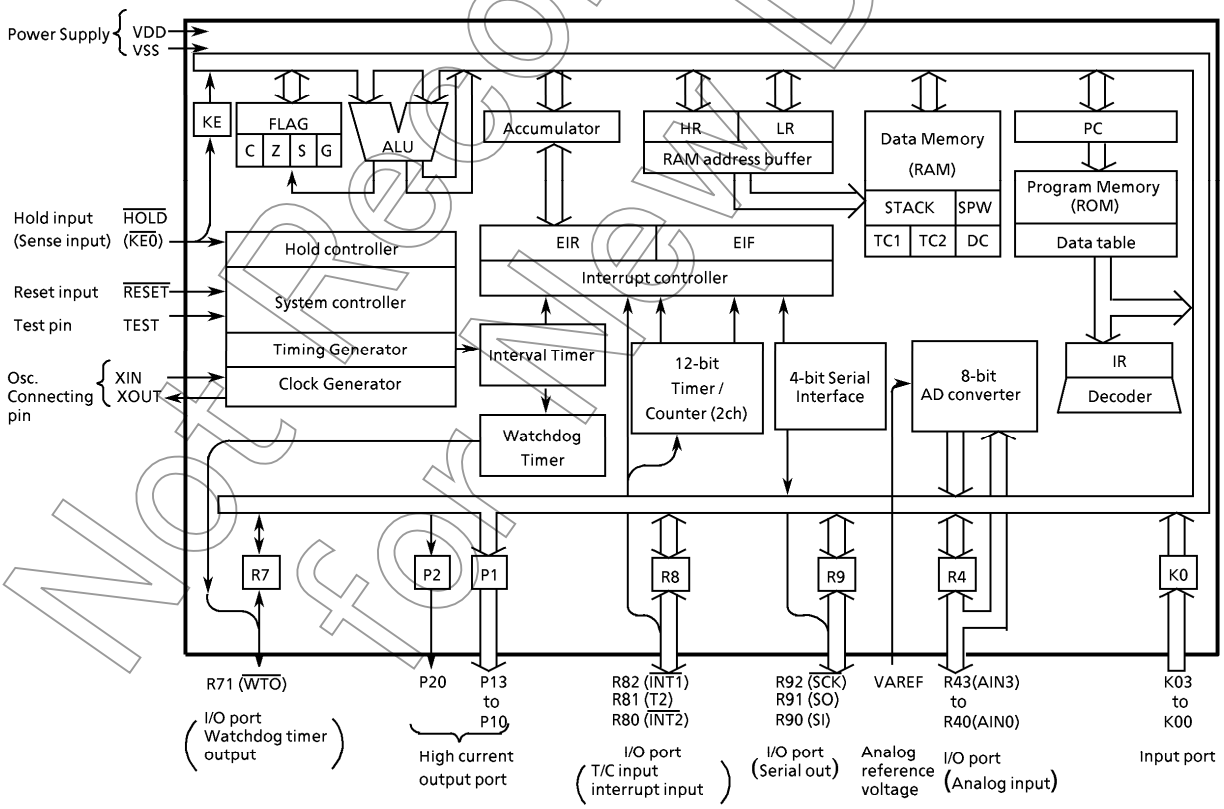
◆Real Time Emulator: BM47214A + BM1152 (SDIP)

Pin Assignment (Top View)

P-SDIP28-400-1.78 / P-SOP28-450-1.27



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
K03 to K00	Input	4-bit input port	
P13 to P10	Output	4-bit output port with latch.	
P20		1-bit output port with latch.	
R43 (AIN3) to R40 (AIN0)	I/O (Input)	4-bit I/O port with latch. When using as input port, the latch must be set to "1".	AD converter analog input
R71 ($\overline{WTO}$)	I/O (Output)	1-bit I/O port with latch. When using as input port or watchdog timer output, the latch must be set to "1".	Watchdog timer output
R82 ($\overline{INT1}$)	I/O (Input)	3-bit I/O port with latch. When using as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	External interrupt 1 input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
R92 ($\overline{SCK}$)	I/O (I/O)	3-bit I/O port with latch. When using as input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
XOUT	Output		
$\overline{RESET}$	Input	Reset signal input	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	HOLD request / release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5 V	
VSS		0 V (GND)	AD converter analog reference voltage (GND)
VAREF		AD converter analog reference voltage	

Operational Description

Conserning the TMP47C241, the hardware configuration and operation are described.
The configuration of basic machine instruction for TMP47C241 is same as TLCS-47 Series.

1. System Configuration

(1) Internal CPU Function

These as the same as the TMP47C203.

(2) Peripheral Hardware Function

① I/O Ports	④ AD converter
② Interval Timer	⑤ Watchdog Timer
③ Timer/Counters	⑥ Serial Interface

2. Peripheral Hardware Function

2.1 Ports

The TMP47C241 has 8 I/O ports (21 pins) each as follows:

① K0	;	4-bit input	
② P1	;	4-bit output	
③ P2	;	1-bit output	
④ R4	;	4-bitinput / output	(shared by the AD converter analog inputs)
⑤ R7	;	1-bit input / output	(shared by the watchdog timer output)
⑥ R8	;	3-bit input / output	shared by external interrupt request input and timer / counter input)
⑦ R9	;	3-bit input / output	(shared by serial port)
⑧ KE	;	1-bit sense input	(shared by hold request / release signal input)

5 pins (typ. 20 mA) of P1, P2 ports and 3pins (typ. 7 mA) of R9 port are high current output ports which can directly drive LEDs.
Table 2-3 lists the port address assignments and the I/O instructions that can access the ports.
The 5-bit to 8-bit data conversion instruction [OUTB @HL] is invalid.

(1) Port K0 (K03 to K00)

Port K0 is a 4-bit input-only port. A pull-up or pull-down resistor can be contained by the mask option.

Figure 2-1. Port K0

(2) Ports P1 (P13 to P10)

Ports P1 is 4-bit high current output ports which can directly drive LEDs, with 4-bit latches. When an input instruction is executed, the latch data is read in these ports. The latch is initialized to "1" during reset.

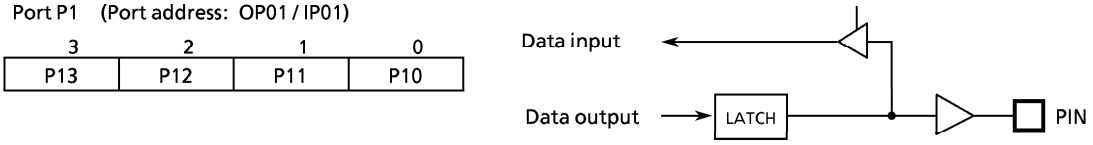


Figure 2-2. Ports P1

(3) Port P2 (P20)

Port P2 is 1-bit output port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. P21, P22 and P23pins do not exist actually. But these pins have the latches.

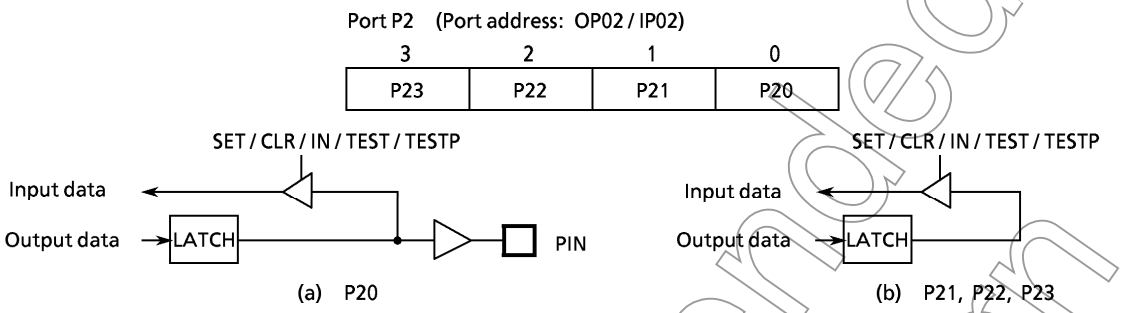


Figure 2-3. Port P2

(4) Ports R4 (R43 to R40)

Ports R4 is 4-bit I/O ports with latch shared by the analog inputs for AD converter. When used as an input ports or analog inputs, the latch should be set to "1". If other port is used as an output, be careful not to execute the output instruction for any port during AD conversion in order to keep accuracy of conversion. The latch is initialized to "1" and analog input is selected R40 (AIN0) pin during reset.

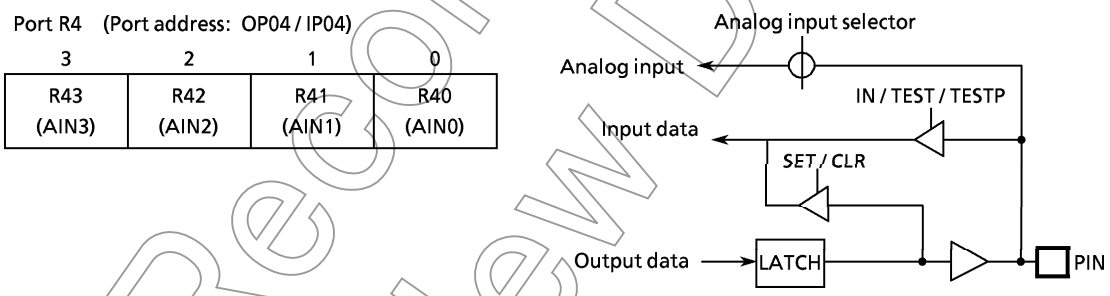


Figure 2-4. Port R4

(5) Port R7 (R71)

1-bit I/O pin with latch. R71 pin is shared by the watchdog timer output. To use R71 pin for the watchdog timer output, the latch should be set to "1". The latch is initialized to "1" during reset. R70, R72, R73 pins do not exist actually but R70 has the latch. In R72 and R73, "1" is read when an input instruction is executed.

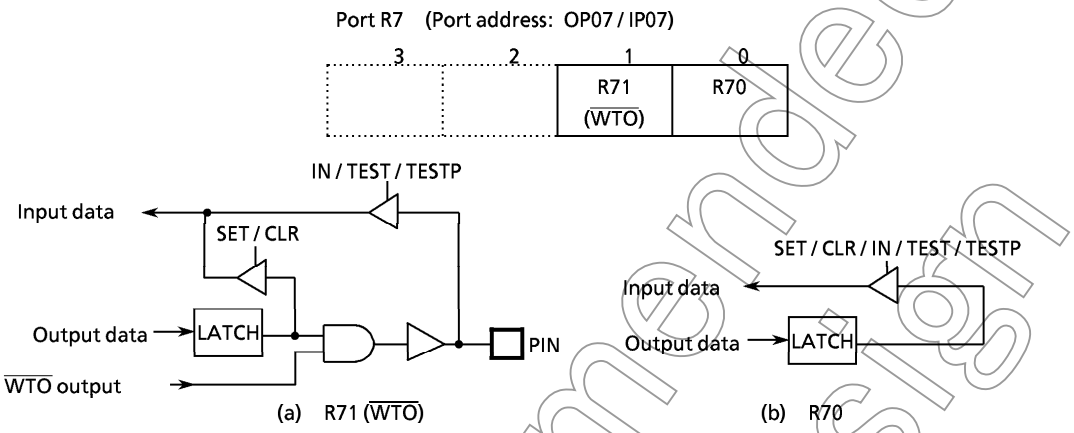


Figure 2-5. Port R7

(6) Port R8 (R82 to R80)

3-bit I/O port with latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset. R83 pins does not exist actually but R83 has the latch. There is no timer / counter 1 external input pin (T1).

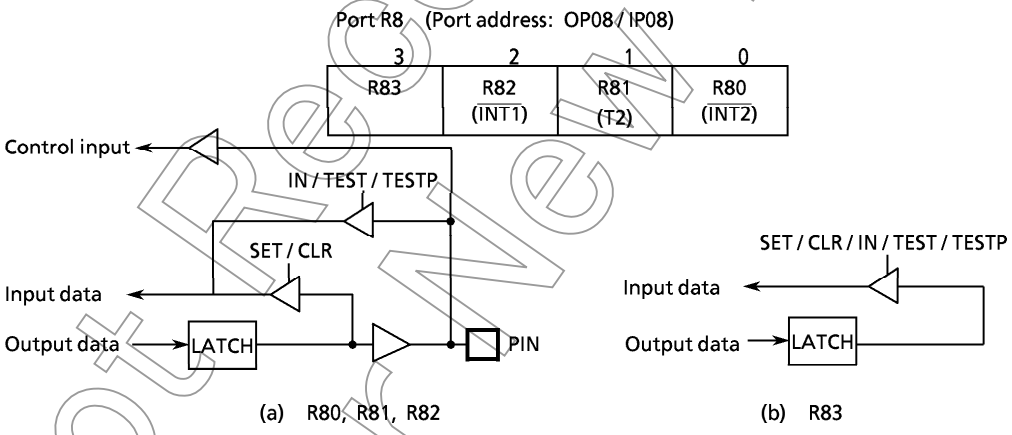


Figure 2-6. Port R8

(7) Port R9 (R92 to R90)

Port R9 is a 3-bit I/O port with a latch. When used as an input, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R9 is shared with the serial port. To use port R9 for the serial port, the latch should be set to "1". To use port R9 for an ordinary I/O port, the serial interface must be disabled.

Although R93 pin dose not exist actually, the set clear instruction for R93 ([SET % OP09, 3] or [CLR % OP09, 3]) should not be execution. However, other instructions can be used, in witch an undefined value is read upon execution of an input instruction.

Port R9 (Port address: OP09 / IP09)

3	2	1	0
	R92 ($\overline{SCK}$)	R91 (SO)	R90 (SI)

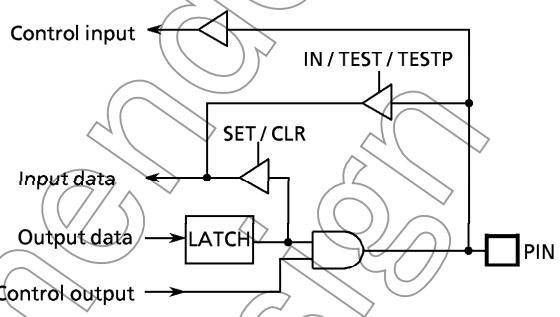


Figure 2-7. Port R9

(8) Port KE ($\overline{KE0}$)

Port KE is a 1-bit sense input port shared with the hold request/release signal input in ($\overline{HOLD}$). This input port is assigned to the least significant bit of Port address IP0E and is processed as the data with inverted polarity. For example, if an input instruction is executed with the pin on the high level, "0" is read.

Example: To wait until $\overline{KE0}$ pin goes low.

```
SWAIT :    TEST    %IP0E,0        ; Waits if KE0 pin = "H".
           B       SWAIT
```

Port KE (Port address: IP0E)

3	2	1	0
(SIOP)	(SEF)		KE0 ($\overline{HOLD}$)

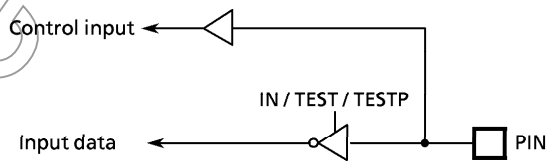


Figure 2-8. Port KE

Table 2-1. Port Address Assignments and Available I/O Instructions

Port Address (**)	Port		Input/Output instruction								
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	—	—	—	—	○	—
01	P1 output latch	P1 output port	○	○	○	—	○	○	—
02	P2 output latch	P2 output port	○	○	○	—	○	○	—
03	——	——	—	—	—	—	—	—	—
04	R4 input port (Analog input)	R4 output port	○	○	○	—	○	○	○
05	——	——	—	—	—	—	—	—	—
06	——	——	—	—	—	—	—	—	—
07	R7 input port	R7 output port (WTO output)	○	○	○	—	○	○	○
08	R8 input port	R8 output port	○	○	○	—	○	○	—
09	R9 input port	R9 output port	○	○	○	—	○	○	—
0A	——	——	—	—	—	—	—	—	—
0B	——	——	—	—	—	—	—	—	—
0C	AD Status input	——	○	—	—	—	—	○	—
0D	AD converted value	——	○	—	—	—	—	○	—
0E	SIO, Hold status	——	○	—	—	—	—	○	—
0F	Serial receive buffer	Serial transmit buffer	○	○	○	—	—	—	—
10_H	Undefined	Hold operation mode control	—	○	—	—	—	—	—
11	Undefined	——	—	—	—	—	—	—	—
12	Undefined	AD analog input selector	—	○	—	—	—	—	—
13	Undefined	AD start register	—	○	—	—	—	—	—
14	Undefined	——	—	—	—	—	—	—	—
15	Undefined	Watchdog Timer control	—	○	—	—	—	—	—
16	Undefined	——	—	—	—	—	—	—	—
17	Undefined	——	—	—	—	—	—	—	—
18	Undefined	——	—	—	—	—	—	—	—
19	Undefined	Interval Timer intrrupt control	—	○	—	—	—	—	—
1A	Undefined	——	—	—	—	—	—	—	—
1B	Undefined	——	—	—	—	—	—	—	—
1C	Undefined	Timer/Counter 1 control	—	○	—	—	—	—	—
1D	Undefined	Timer/Counter 2 control	—	○	—	—	—	—	—
1E	Undefined	——	—	—	—	—	—	—	—
1F	Undefined	Serial interface control	—	○	—	—	—	—	—

Note: "——" means the reserved state. Unavailable for the user programs.

2.2 Interval Timer Interrupt (ITMR)

The interval timer can be used to generate an interrupt with a fixed frequency. Internal time interrupt is control by the command register (OP19). An interval timer interrupt is generated at the first rising edge of the binary counters output after the command has been set. The interval timer is not cleared by command, so that the first interrupt may occur earlier than the preset interrupt period.

Example: To set the interval timer interrupt frequency to fc/2^{12} [Hz].

```
LD      A,  #0110B    ;  OP19←0110B
OUT     A,  %OP19
```

Interval Timer interrupt command register
(Port address: OP19)

3	2	1	0
TMRE		TMRF	

(Initial value: 0000)

TMRE	Interrupt disable/enable
00: Stop	
01: Enable	
1*: (Reserved)	

*Note: *; Don't care*

TMRF	Interrupt frequency	Example: fc = 4.19 MHz
00:	fc / 2^{10} [Hz]	4096 [Hz]
01:	fc / 2^{11}	2048
10:	fc / 2^{12}	1024
11:	fc / 2^{13}	512

Figure 2-9. Interval Timer Interrupt Command Register

2.3 Timer/Counters (TC1, TC2)

The TMP47C241 contain two 12-bit timer/counters (TC1, TC2). RAM addresses are assigned to the count register in unit of 4 bits, permitting the initial value setting and counter reading through the RAM manipulation instruction. When the timer/counter is not used, the mode selection may be set to "stopped" to use the RAM at the address corresponding to the timer / counter for storing the ordinary user-processed data.

	MSB		LSB
	Timer / Counter 1 (TC1)		
	$TC1_H$	$TC1_M$	$TC1_L$
RAM address TMP47C241	(76_H)	(75_H)	(74_H)

	MSB		LSB
	Timer / Counter 2 (TC2)		
	$TC2_H$	$TC2_M$	$TC2_L$
RAM address TMP47C241	($7A_H$)	(79_H)	(78_H)

Figure 2-10. The Count registers of the Timer / Counters (TC1, TC2)

2.3.1 Functions of Timer / Counters

The timer / counters provide the following functions:

① Event counter
② Programmable timer
③ Pulse width measurement

2.3.2 Control of Timer / Counters

The timer / counters are controlled by the command registers. The command register is accessed as port address OP1C for TC1 and port address OP1D for TC2. These registers are initialized to "0" during reset.

Timer / Counter 1 control command register
(Port address: OP1C) (Initial value: 0000)

3	2	1	0
TC1MS		IPR1	

TC1MS	Mode selection

00: Stop
01: Invalid code
10: Timer mode
11: Invalid code

IPR1	Internal pulse rate (interval timer output) selection

Example: At fc = 4.19 MHz

00: $fc/2^{10}$ [Hz] ..... 4096 [Hz]
01: $fc/2^{14}$ 256
10: $fc/2^{18}$ 16
11: $fc/2^{22}$ 1

(a) TC1

Timer / Counter 2 control command register
(Port address: OP1D) (Initial value: 0000)

3	2	1	0
TC2MS		IPR2	

TC2MS	Mode selection

00: Stop
01: Event counter mode
10: Timer mode
11: Pulse width measurement mode

IPR2	Internal pulse rate (interval timer output) selection

Example: At fc = 4.19 MHz

00: $fc/2^{10}$ [Hz] ..... 4096 [Hz]
01: $fc/2^{14}$ 256
10: $fc/2^{18}$ 16
11: $fc/2^{22}$ 1

(b) TC2

Note: fc; Basic clock frequency [Hz]

Figure 2-11. Timer / Counter Control Command Registers

The timer/counter increments at the rising edge of each count pulse. Counting starts with the first rising edge of the count pulse generated after the command has been set. Count operation is performed in one instruction cycle after the current instruction execution, during which the execution of a next instruction and the acceptance of an interrupt are delayed. If counting is requested by both TC1 and TC2 simultaneously, the request by TC1 is preferred. The request by TC2 is accepted in the next instruction cycle. Therefore, during count operation, the apparent instruction execution speed drops as counting occurs more frequently.

The timer / counter causes an interrupt upon occurrence of an overflow (a transition of the count value from FFF_H to 000_H). If the timer / counter is in the interrupt enabled state and the overflow interrupt is accepted immediately after its occurrence, the interrupt is processed in the sequence shown in Figure 2-12. Note that counting continues if there is a count request after overflow occurrence.

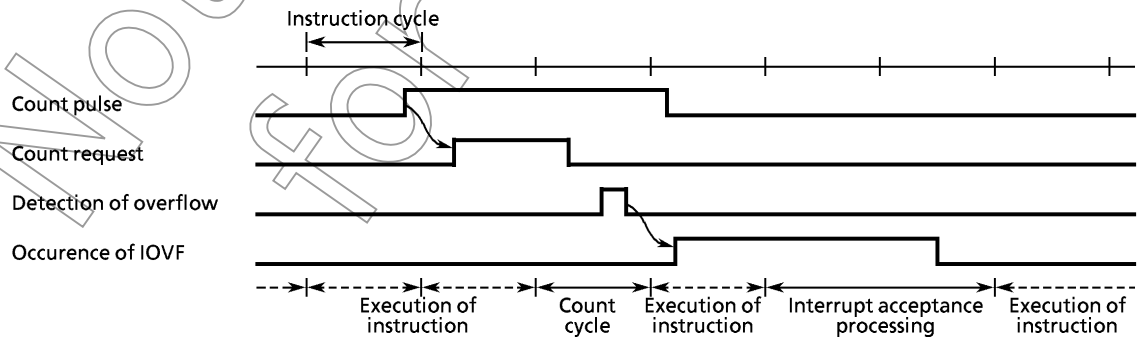


Figure 2-12. Timer / Counter Overflow Interrupt Timing

(1) Event counter mode

In the event counter mode, the timer / counter increments at each rising edge of the external pin (T1, T2) input. T1 and T2 pins are also used as the R83 and R81 pins.

To use these pins as the T/C input, set the output latch of R83 and R83 and R81 to "1".

At reset, the output latch is initialized to "1". The maximum applied frequency of the external pin input is fc/32 for the 1-channel operation; for the 2-channel operation, the frequency is fc/32 for TC1 and fc/40 for TC2. The apparent instruction execution speed drops most to (9/11) × 100 = 82% when TC1 and TC2 are operated at the maximum applied frequency because the count operation is inserted once every 4 instruction cycles for TC1 and every 5 cycles for TC2. For example, the instruction execution speed of 2 μs drops to 3.64 μs.

Example: To operate TC2 in the event counter mode

```
LD      A,  #0100B    ;  OP1D←01**B
OUT     A,  %OP1D
```

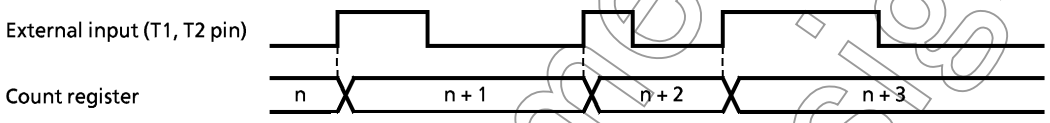


Figure 2-13. Event Counter Mode Timing chart

(2) Timer mode

In the timer mode, the timer/counter increments at the rising edge of the internal pulse generated from the interval timer. One of 4 internal pulse rates can be selected by the command register. The selected rate can be initially set to the timer/counter to generate an overflow interrupt in order to create a desired time interval.

When an internal pulse rate of $fc/2^{10}$ is used, a count operation is inserted once every 128 instruction cycles, so that the apparent instruction execution speed drops by (1/127) × 100 = 0.8 %. For example, the instruction execution speed of 2 μs drops to 2.016 μs.

In the timer mode, R83 (T1) and R81 (T2) pins provide the ordinary I/O ports.

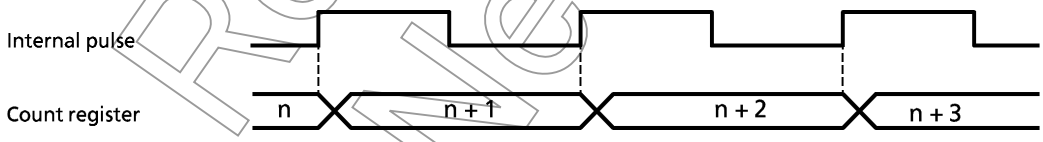


Figure 2-14. Timer Mode Timing chart

Example: To generate an overflow interrupt (at fc = 4 MHz) by the TC1 after 100 ms.

```
LD      HL,  #0F4H    ;  TC1←E79H (setting of the count register)
ST      #9,  @HL+
ST      #7,  @HL+
ST      #0EH,  @HL+
LD      A,  #1000B    ;  OP1C←1000B
OUT     A,  %OP1C
LD      A,  #0100B    ;  EIR←0100B (enables interrupt)
XCH     A,  EIR
EICLR   IL,  110111B  ;  EIF←1, IL3←0
```

**** Calculating the preset value of the counter register***

The preset value of the count register is obtained from the following relation:

2^{12} – (interrupt setting time) × (internal pulse rate)

For example, to generate an overflow interrupt after 100 ms at fc = 4 MHz with the internal pulse rate of fc/2^{10}, set the following value to the count register as the preset value:

$2^{12} - (100 \times 10^{-3}) \times (4 \times 10^{6}/2^{10}) = 3705 = E79_{H}$

* The apparent execution rate is caleulated as following.

$$1 \div \{ \frac{\text{(Fundamental clock frequency) / 8}}{\text{(Internal pulse rate)}} - 1 \} \times 100 \quad [\%]$$

Table 2-2. Internal Pulse Rate Selection

Internal pulse rate	Max. setting time	Example: At fc = 4.194304 MHz	
		Internal pulse rate	Max. setting time
fc/2^{10} [Hz]	2^{22}/fc [s]	4096 [Hz]	1 [s]
fc/2^{14}	2^{26}/fc	256	16
fc/2^{18}	2^{30}/fc	16	256
fc/2^{22}	2^{34}/fc	1	4096

(3) Pulse width measurement mode

In the pulse width measurement mode, the timer / counter increments with the pulse obtained by sampling the external pin (T1, T2) by the internal pulse. As shown in Figure 2-15, the timer / counter increments only while the external pin input is high. The maximum applied frequency to the external pin input must be one that is enough for analyzing the count value. Normally, a frequency sufficient slower than the internal pulse rate setting is applied to the external pin.

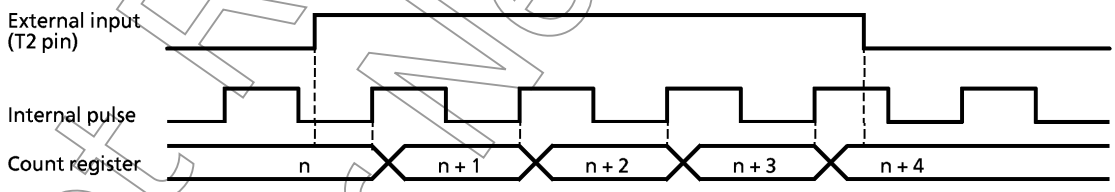


Figure 2-15. Pulse Width Measurement Mode Timing chart

2.4 AD Converter

The TMP47C241 has a 8-bit successive approximate type AD converter and is capable of processing 4 analog inputs.

2.4.1 Circuit configuration

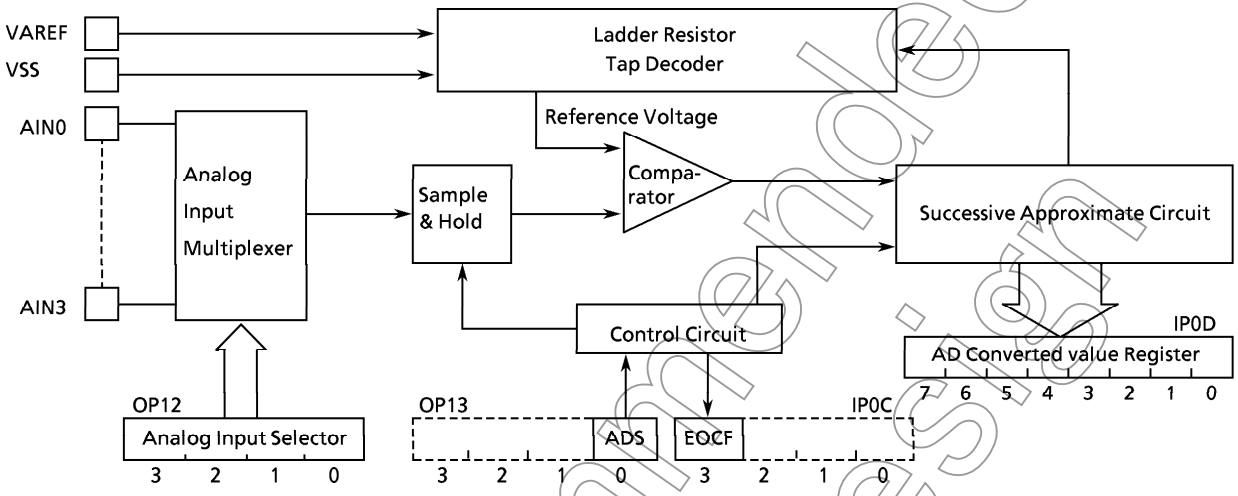


Figure 2-16. Block Diagram of AD Converter

2.4.2 Control of AD converter

The operation of AD converter is controlled by a command register (OP12, OP13, IP0C, IP0D).

(1) Analog input selector (OP12)

Analog inputs (AIN0 through AIN3) are selected by values of this register.

Analog input select command register
(Port address: OP12)

3	2	1	0	
SAIN				(Initial value: 0000)

SAIN	Analog input selection
0000:	R40(AIN0)
0001:	R41(AIN1)
0010:	R42(AIN2)
0011:	R43(AIN3)
01**:	Analog input is not selected.
1***:	Analog input is not selected.

*Note: *; Don't care*

Figure 2-17. Analog input selector

(2) Start of AD conversion (OP13)

AD conversion is started when ADS is set to "1" . After the conversion is started, ADS is cleared by hardware. If ADS is set to "1" during the AD conversion, the conversion is started again at the time. Analog input voltage is hold by the sample hold circuit.

AD conversion start command register
(Port address: OP13)

3	2	1	0	
			ADS	(Initial value: 0000)

ADS	AD conversion enable

1: AD conversion is started (clears after starting)

Figure 2-18. AD conversion start register

(3) AD converter and register (IP0C)

End of conversion flag (EOCF) is a single bit flag showing the end of conversion and is set to "1" when conversion ended. When both upper 4 bits and lower 4 bits of a converted value are read or AD conversion is started, EOCF is cleared to "0".

AD converter status register
(Port address: IP0C)

3	2	1	0
EOCF			

EOCF	End of conversion flag

0: Under AD conversion or before AD conversion
1: End of AD conversion

Figure 2-19. AD converter status register

(4) AD converted value register (IP0D)

An AD converted value is read by accessing port address IP0D. An AD converted value is read by splitting into upper 4 bits and lower 4 bits by a value of LR_0 (LSB of the L-registers).

AD converted value register
(Port address: IP0D)

3	2	1	0
D3	D2	D1	D0
D7	D6	D5	D4

D7 to D0	Reading of an AD converted value

When $LR_0 = 0$, lower 4 bits of the converted value is read.
When $LR_0 = 1$, upper 4 bits of the converted value is read.

Figure 2-20. AD converted value register

2.4.3 How to use AD converter

Apply positive of analog reference voltage to the VAREF pin and negative to the VSS pin. The AD conversion is carried out by splitting reference voltage between VAREF and VSS to bit corresponding voltage by a ladder resistor and making a judgement by comparing it with analog input voltage.
Analog supply current (I_{REF}) is typically 500 μA at VAREF = 5 V.
Note that this ladder resistor is connected to VAREF and VSS even in the HOLD mode. Therefore to reduce the power consumption, VAREF should be disconnected from the analog reference voltage supply.

(1) Start of AD conversion

Prior to conversion, select one of the analog input AIN0 through AIN3 by the analog input selector. Place output of the analog input, which is to be AD converted, in the high impedance state by setting "1". If other port is used as an output, be careful not to execute the output instruction for any port during conversion in order to keep accuracy of conversion.
AD conversion is started by setting ADS (bit 1 of the AD conversion start register). When conversion ends after 24 instruction cycles, EOCF showing the end of conversion is set to "1".
Analog input voltage is sampled during the following 2 instruction cycles after setting ADS.

Note: The sample and hold circuit has capacitor (C_A = 12 pF typ.) with resistor (R_A = 5 kΩ typ.). See I/O circuitry table. This capacitor should be charged or discharged within 2 instruction cycles.

(2) Reading of an AD converted value

After the end of conversion, read an AD converted value is read by splitting into lower 4 bits and upper 4 bits by the AD converted value register (IP0D).
Lower 4 bits of the AD converted value can be read when LR_0 = 0 and upper 4 bits when LR_0 = 1. Usually an AD converted value is stored in RAM by an instruction [IN %p, @HL]. Further, if an AD converted value is read during the conversion, it becomes an indefinite value.

(3) AD conversion with HOLD operation

When the HOLD operation is started during the conversion, the conversion is terminated and an AD converted value becomes indefinite. Therefore, EOCF is kept clear to "0" after release from the HOLD operation. However, if the HOLD operation is started after the end of AD conversion (after EOCF has been set), AD converted value and status of EOCF are held.

Example: Selecting analog input (AIN3), starting AD conversion, monitoring EOCF and storing lower 4 bits and upper 4 bits of a converted value to RAM [10_H] and RAM [11_H] respectively.

```
        LD      A, #3           ;  Selects analog input (AIN3)
        OUT     A, %OP12
        LD      A, #1           ;  Start of AD conversion
        OUT     A, %OP13
SLOOP : TEST    %IP0C, 3        ;  To wait until EOCF goes to "1"
        B       SLOOP
        LD      HL, #10H        ;  HL ← 10H
        IN      %IP0D, @HL      ;  RAM [10H] ← Lower 4 bits
        INC     L               ;  Increment of L registers
        IN      %IP0D, @HL      ;  RAM [11H] ← Upper 4 bits
```

2.5 Watchdog Timer (WDT)

The purpose of the watchdog timer is to detect the malfunction (ranaway) of program due to external noise or other causes and return the operation to the normal condition.

The watchdog timer output is output to R71 must be set to "1". Further, during reset, the output latch of R71 is set to "1", and the watchdog timer becomes disable state.

The initialization at time of runaway will become possible when the $\overline{WTO}$ pin and $\overline{RESET}$ pin are connected each other.

2.5.1 Configuration of Watchdog Timer

The watchdog timer consists of 3-stage binary counter, flip-flop (F/F), and its control circuit. The F/F is set to "1" during reset, and cleared to "0" at the rising edge of the binary counter output.

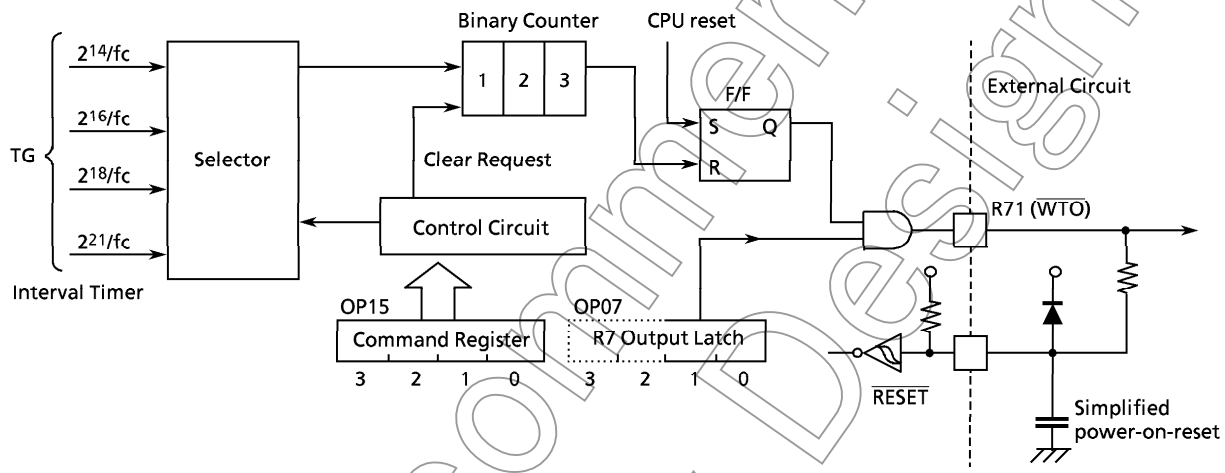


Figure 2-21. Watchdog Timer

2.5.2 Control of watchdog timer

The watchdog timer is controlled by the command register (OP15). This command register is initialized to "0000_B" during reset. The following are procedure to detect the malfunction (runaway) of CPU by the watchdog timer.

① At first, detection time of the watchdog timer should be set and binary counter should be cleared.

② The watchdog timer should be become enable.

③ Binary counter must be cleared before the detection time of the watchdog timer. When the runaway of CPU is taken place for some reason and binary counter is not cleared, the F/F is cleared to "0"at the rising edge of the binary counter and signal of runaway detection is become active ($\overline{WTO}$ output is "L").

Watchdog Timer control command register (Port address: OP15) (Initial value: 0000)

3	2	1	0
RWT	EWT	TWT	

RWT	Clears binary counter

0: Clears binary counter (After clear, automatically "1" is set)

EWT	Enable / Disable

0: Disable
1: Enable

TWT	Setting of watchdog timer detection time

Example: At fC = 4.19 MHz

00: 2^{17}/fc [s] ..... 31.25 [ms]
01: 2^{19}/fc 125
10: 2^{21}/fc 500

Note: fc: Basic clock frequency [Hz]

Figure 2-22. Command Register

Example: To set the watchdog detection time (2^{21}/fc [s]). And to enable the watchdog timer.

```
        LD      A, #0010B       ; OP15 ← 0010B
                                  (Sets WDT detection time. Clears binary counter)
        OUT     A, %OP15
        LD      A, #0110B       ; OP15 ← 0110B (Enables WDT)
        OUT     A, %OP15
        :
        :
        :
        LD      A, #0110B       ; OP15 ← 0110B (Clears binary counter)
        OUT     A, %OP15
        :
        :
```

Within WDT detection time

Note: It is not necessary to set RWT to "1". Note that both EWT (Enable Watchdog Timer) and RWT should not be set to "1" at the same time.

2.6 Serial Interface (SIO)

The TMP47C200B/400B have a serial interface with a 4-bit buffer. The serial interface is connected to the external device via 3 pins (the serial port): R92 ($\overline{SCK}$), R91 (SO), and R90 (SI). The serial port is shared by port R9. For the serial port, the output latch of port R9 must be set to "1". In the transmit mode, R90 pin provides the I/O port; in the receive mode, R91 pin provides the I/O port.

2.6.1 Configuration of Serial Interface

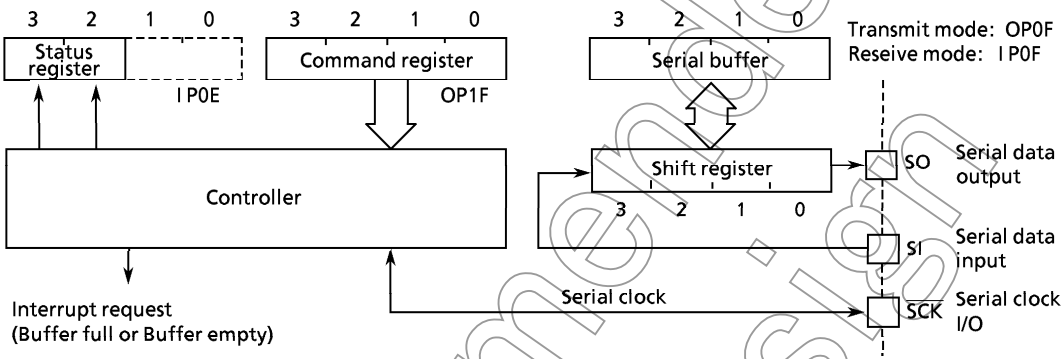


Figure 2-23. Configuration of Serial Interface

2.6.2 Control of Serial Interface

The serial interface is controlled by the command register 1.2 (OP1F) and the staus register (IPOE).

Serial Interface control command register (Port address: OP1F)

3	2	1	0
ESIO	RM	LM	ECKM

(Initial value: 0000)

ESIO	Instructs serial transfer start / terminate
0:	Serial transfer terminate
1:	Serial transfer start

RM	Selects transfer mode
0:	Transmit mode
1:	Receive mode

LM	Selects shift edge
0:	Shift at the trailing edge of serial clock
1:	Shift at the leading edge of serial clock

ECKM	Selects serial clock
0:	Internal clock (output to $\overline{SCK}$ pin)
1:	External clock (input from $\overline{SCK}$ pin)

Note 1: fc: High-frequency clock [Hz]
Note 2: When setting the transfer mode, ESIO must be "0". When Transmit mode, LM must be "1".

Figure 2-24. Serial Interface Control Command Register

Serial Interface status register (Port address: IP0E)

3	2	1	0
SIOF	SEF	(SMF)	(HOLD)

SIOF	Monitors serial transfer operation state

0: Transfer is terminated

1: Transfer is in progress

SEF	Monitors shift operation state

0: Shift operation is terminated

1: Shift operation is in progress

Figure 2-25. Serial Interface Status Register

2.6.3 Serial Clock

For the serial clock, one of the following can be selected according to the contents of the command register:

(1) Clock source selection

a. Internal clock

fc/2^7 [Hz] is used for the serial clock (at fc = 4.194304 MHz, the serial clock frequency is 32.768 kHz). The serial clock is output on the $\overline{SCK}$ pin. Note that at the start of transfer, the $\overline{SCK}$ pin output goes high. This serial interface provides the wait function in which the shift is not occurred until these processings are completed.

The highest transfer rate based on the internal clock is 31250 bits/second (at fc = 4 MHz).

b. External clock

The signal obtained by the clock supplied to the $\overline{SCK}$ pin from the outside is used for the serial clock. In this case, the output latch of R92 ($\overline{SCK}$) must be set to "1" beforehand. For the shift operation to be performed correctly, each of the clock's high and low levels needs two instructions or more to be completed.

(2) Shift edge selection

a. Leading edge

Data is shifted at the leading edge (the falling edge of $\overline{SCK}$ pin input) of the serial clock.

b. Trailing edge

Data is shifted at the trailing edge (the rising edge of $\overline{SCK}$ pin input) of the serial clock. However, in the transmit mode, the trailing edge shift is not supported.

2.6.4 Transfer Modes

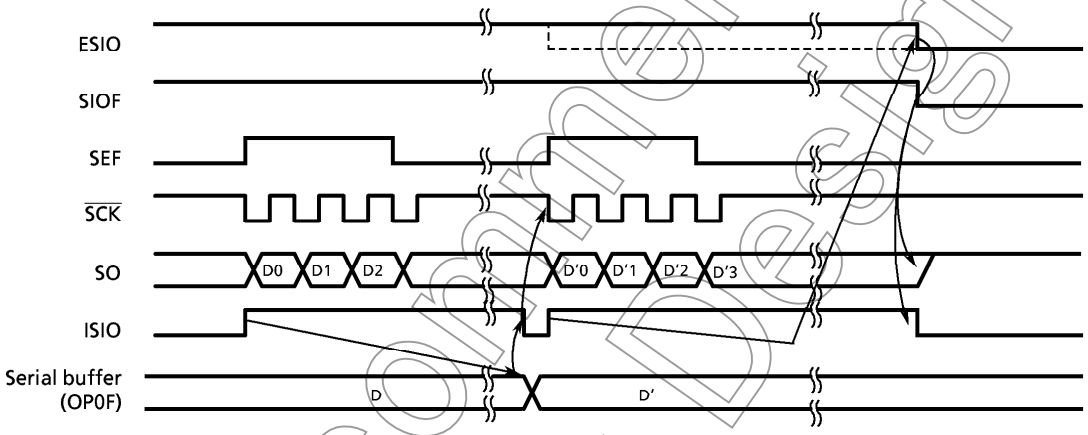
Selection between the transmit mode and the receive mode is performed by RM (bit 2 of the command register).

(1) Transmit mode

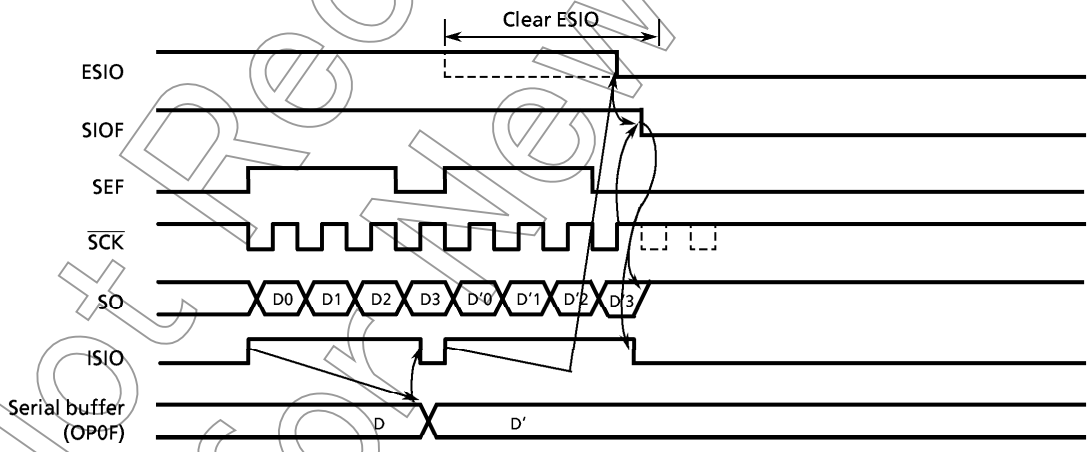
The transmit mode is set to the command register then the first transmit data (4 bits) is written to the buffer register OP0F (if the transmit mode is not set, the data is not written to the buffer register). Then, setting ESIO to "1" starts transmission. The transmit data is output to the SO pin synchronization with the serial clock from the LSB side sequentially. When the LSB is output, the transmit data is moved from the buffer register to the shift register. When the buffer register becomes empty, the buffer empty interrupt (ISIO) to request for the next transmit data is generated. When the interrupt service program writes the transmit data to the buffer register, the interrupt request is reset.

In the operation based on the internal clock, if no more data is set after the transmission of the 4-bit data, the serial clock is stopped and the wait state sets in.
In the operation based on the external clock, the data must be set in the buffer register by the time the next data shift operation starts. Therefore, the transfer rate is determined by the maximum delay time between the occurrence of the interrupt request and the writing of data to the buffer register by the interrupt service program.

To end transmission, ESIO is cleared to "0" instead of writing the next transmit data by the buffer empty interrupt service program. When ESIO is cleared, transmission stops upon termination of the currently shifted-out data. The transmission end can be known by the SIOF state (SIOF goes "0" upon transmission end). In the operation based on the external clock, ESIO must be cleared to "0" before the next data is shifted out. If ESIO is not cleared before, the transmission stops upon transmitting the next data (dummy).



(a) Internal-clock-based operation with wait



(b) External-clock-based operation

Figure 2-26. Transmit Mode

Example 1: To transmit data stored in the RAM (its address is specified by the HL register pair) in synchronization with the internal clock.

```
        LD      A, #0010B       ; OP1F←0010B (Sets the transmit mode of
                                  internal-clock-based operation)
        OUT     A, %OP1F
        OUT     @HL, %OP0F      ; OP0F←RAM [HL] (Writes the first transmit data)
        LD      A, #1010B       ; ESIO←1 (Instructs transmission start)
        OUT     A, %OP1F
```

Example 2: To end transmission (internal-clock-based operation)

```
        LD      A, #0010B       ; ESIO←0 (Instructs transmission end)
        OUT     A, %OP1F
SENDC:  TESTP   %IP0E, 3        ; Waits until SIOF = "0"
        B       SENDC
```

(2) Receive mode

Data can be received when ESIO is set to "1" after setting the receive mode to the command register. The data is put from the SI pin to the shift register in synchronization with the serial clock. Then the 4-bit data is transferred from the shift register to the buffer register (IP0F), upon which the buffer full interrupt (ISIO) to request for reading received data is generated. The received data is read from the buffer register by the interrupt service program. When the data has been read, the interrupt request is reset and the next data is put in the shift register to be transferred to the buffer register.

In the operation based on the internal clock, if the previous received data has not been read from the buffer register at the end of capturing the next data, the serial clock is stopped and the wait operation is performed until the data has been read.

In the operation based on the external clock, the shift operation is performed in synchronization with the externally-supplied clock, so that the data must be read from the buffer register before the next receive data is transferred to it. The maximum transfer rate in the external-clock-based operation is determined by the maximum delay time between the generation of interrupt request and the reading of received data.

In the receive mode, the shift operation may be performed at either the leading edge or the trailing edge. In the leading edge shift operation, data is captured at the leading edge of the serial clock, so that the first shift data must be put in the SI pin before the first serial clock is applied at the start of transfer.

Note: If the transfer modes are changed, the contents of the buffer register are lost.
Therefore, the modes should not be changed until the last received data is read even after the end of reception is instructed (by clearinf ESIO to "0").

Example: To instruct the receive start operation with the internal clock and leading edge shift (with the interrupt enable register already set).

```
        LD      A,#0110B    ;   OP1F←0110B (Sets the receive mode)
        OUT     A,%OP1F
        EI                  ;   EIF←1 (Enables interrupt)
        LD      A,#1110B    ;   ESIO←1 (Instructs receive start)
        OUT     A,%OP1F
         ⋮
```

To end the receive operation, ESIO should be cleared to "0". When ESIO is cleared, the completion of the transfer of the current 4-bit data to the buffer register terminates the receive operation. To confirm the end of the receive operation by program, SIOF should be sensed. SIOF goes "0" at the end of receive operation.

Note: If the receive and transmit modes are switched, the contents of the buffer register are lost. Therefore, the modes should not be switched until the last receive data is read even after the end of reception is instructed (by clearing ESIO to "0").

The receive operation can be terminated in one of the following approaches determined by the transfer rate:

a. When the transfer rate is sufficiently low (the external-clock-based operation):
If ESIO can be cleared to "0" before the next serial clock is applied upon occurrence of buffer full interrupt in the external-clock-based operation, ESIO is cleared to "0" by the interrupt service program, then the last receive data is read.

Example: To instruct the receive end with sufficient low transfer rate (the reading edge shift).

```
        LD      A,#0111B    ;  ESIO←0 (Instructs receive end)
        OUT     A,%OP1F
        IN      %IP0F,A     ;  Acc←IP0F (Reads received data)
```

b. When the transfer rate is sufficiently high (the internal/external clock-based operation):
If the transfer rate is high and, therefore, it is possible that the capture of the next data starts before ESIO is cleared to "0" upon acceptance of an interrupt, ESIO must be cleared to "0" by confirming that SEF (bit 2 of the status register) is set at reading the data proceeding the last data. Then, the data is read.
In the interrupt servicing following the reception of the last data, no operation is needed for termination; only the reading of the received data is performed. This method is generally employed for the internal-clock-based operations. For an external-clock-based operation, ESIO must be cleared and the receive data must be read before the last data is transferred to the buffer register.

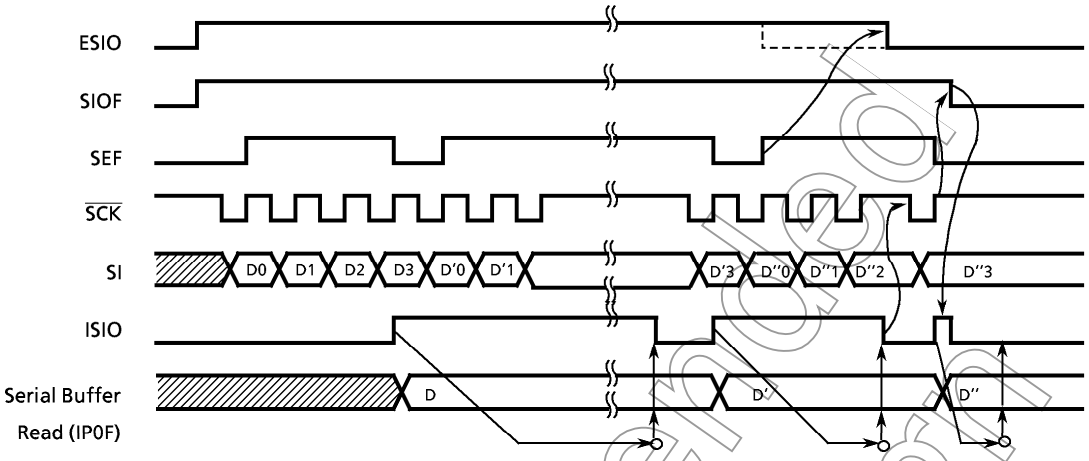
Example: To instruct receive end when the transfer rate is high (the internal clock, reading edge shift).

```
SSEF0:  TEST    %IP0E, 2        ;  Waits until SEF = "1"
        B       SSEF0
        LD      A, #0110B       ;  ESIO←0 (Instructs receive end)
        OUT     A, %OP1F
        IN      %IP0F, A        ;  Acc←IP0F (Reads received data)
```

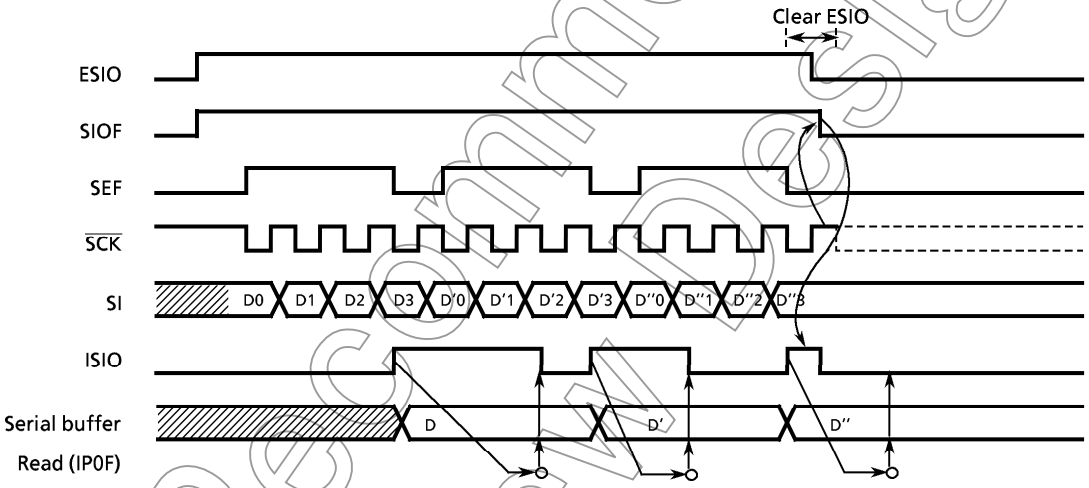
c. One-word reception
When receiving only one word, ESIO is set to "1" then it is returned to "0" after confirming that SEF (bit 2 of the status register) has gone "1". In this case, buffer full interrupt is caused only once, so that the received data is read by the interrupt service program.

Example: To instruction the start/end of one-word reception (the internal clock, the leading edge shift).

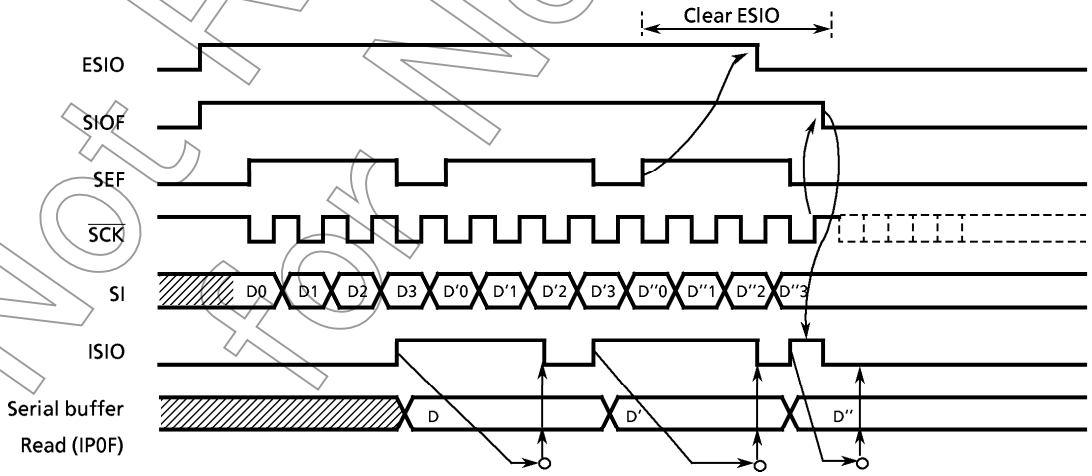
```
        LD      A, #0110B       ;  OP1F←0110B (Sets in the receive mode)
        OUT     A, %OP1F
        EI                      ;  EIF←1 (Enables interrupt)
        LD      A, #1110B       ;  ESIO←1 (Instructs receive start)
        OUT     A, %OP1F
SSEF0:  TEST    %IP0E, 2        ;  Confirms that SEF = "1"
        B       SSEF0
        LD      A, #0110B       ;  ESIO←0 (Instructs receive end)
        OUT     A, %OP1F
```



(a) Internal-clock-based operation, trailing-edge shift (with wait)



(b) External-clock-based operation, reading-edge shift (when transfer rate is low)



(C) Internal-clock-based operation, reading-edge shift (when transfer rate is high)

Figure 2-27. Receive Mode

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

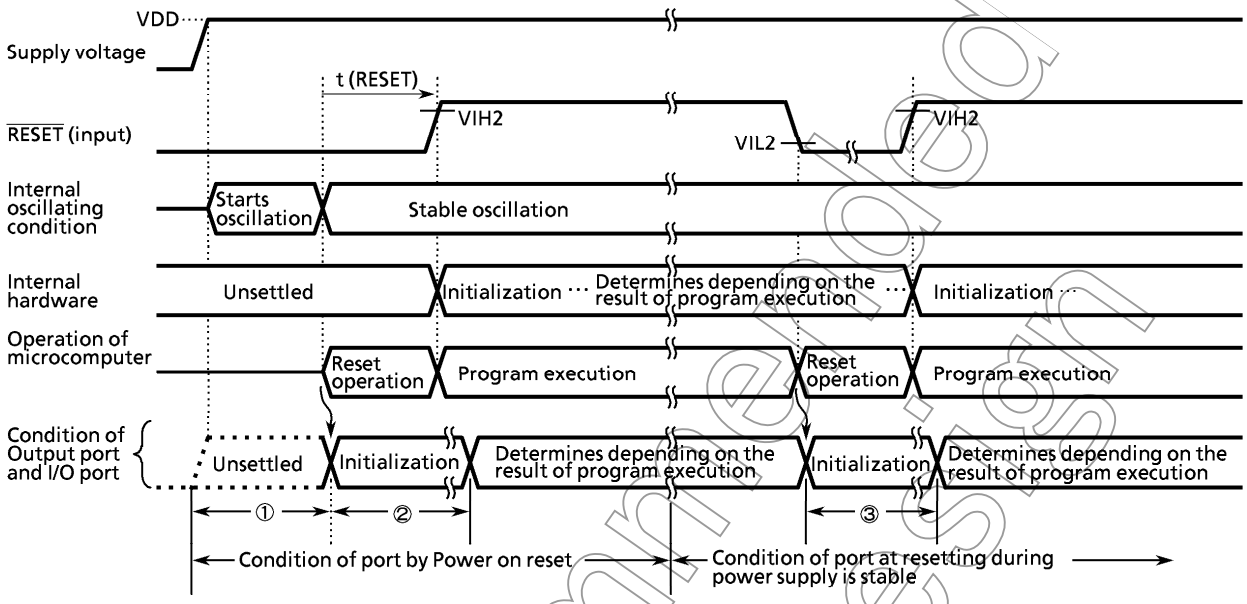


Figure 2-28. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

Note 2: VIL2: Stands for low level input voltage of $\overline{\text{RESET}}$ pin.
VIH2: Stands for high level input voltage of $\overline{\text{RESET}}$ pin.

Note 3: The condition of each port is unstable until the reset operation is started (① in the above Figure). Thus, when using port as an output pin, in the term of ①, to prevent the malfunction of external application circuit, insert the circuit outside of microcomputer between the output pin of Port and input pin of external application circuit.

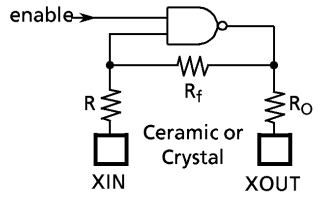
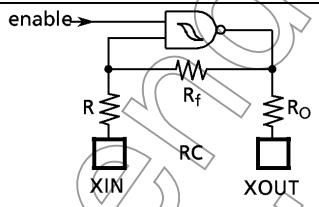
Note 4: The term starting from reset operation to the program which accesses port is executed (②, ③ in the above Figure), the condition of port becomes on the status of initialization by Reset operation. The initial condition of port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ② and ③, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and/or pull-down resistor.

Input / Output Circuitry

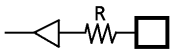
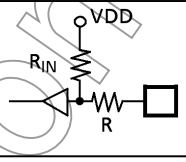
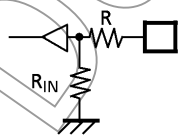
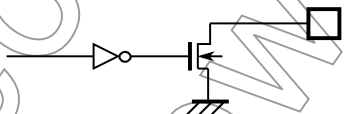
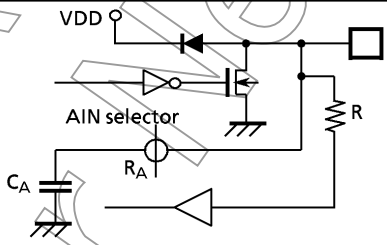
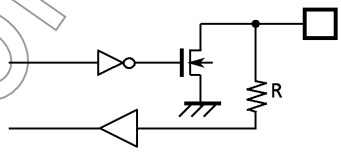
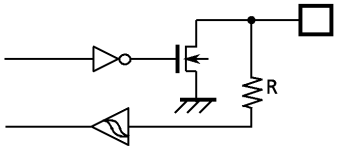
The input / output circuitries of the TMP47C241 (code SA-SC or SG) are shown as below.

(1) Control pins

The input / output circuitries of the TMP47C241 control pins except XIN and XOUT pins are similar to that of the TMP47C200B.

Pins	I/O	Circuitry and Code		Remarks
		SA, SB, SC	SG	
XIN XOUT	Input Outut			Resonator connecting pins R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_o = 2 kΩ (typ.)

(2) I/O Ports

Port	I/O	Input / Output Circuitry and Code			Remarks
		SA, SG	SB	SC	
K0	Input				Pull-up/Pull-down resistor R_{IN} = 70 kΩ (typ.) R = 1 kΩ (typ.)
P1 P2	Output				Sink open drain output Initial "Hi-Z" High current I_{OL} = 20 mA (typ.)
R4	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.) Analog input R_A = 5 kΩ (typ.) C_A = 12 pF (typ.)
R7	I/O				Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R8 R9	I/O				Sink open drain output Initial "Hi-Z" High current (R9) I_{OL} = 7 mA (typ.) Hysteresis input R = 1 kΩ (typ.)

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 7	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P1, P2, R7 to R9	– 0.3 to 10	
	V_{OUT3}	Analog inputs	– 0.3 to V_{DD} + 0.3	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Port R9	15	
	I_{OUT3}	Ports R4, R7, R8	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2, R9	120	mA
Power Dissipation [Topr = 70°C]	PD		300	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		fc = 6.0 MHz	4.5	6.0	V
			fc = 4.2 MHz	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	In the normal operating area	V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input		V_{DD} × 0.75		
	V_{IH3}		In the HOLD mode	V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	In the normal operating area	0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input			V_{DD} × 0.25	
	V_{IL3}		In the HOLD mode		V_{DD} × 0.1	
Clock Frequency	fc		V_{DD} = 4.5 V to 6.0 V	0.4	6.0	MHz
			V_{DD} = 2.7 V to 6.0 V		4.2	
			In the RC oscillation		2.5	

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

DC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	kΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Ports R, P (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Low Output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
	I_{OL2}	Port R9		—	7	—	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5 V, fc = 4 MHz	—	2	4	mA
			V_{DD} = 3.0 V, fc = 4 MHz	—	1	2	
			V_{DD} = 3.0 V, fc = 400 kHz	—	0.5	1	
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1: Typ. values show those at Topr = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3 V / 0.2 V (V_{DD} = 5.5 V), 2.8 V / 0.2 V (V_{DD} = 3.0 V)

AD Conversion Characteristics

(Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	—	V_{DD}	V
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{SS}	2.7	—	—	V
Analog Input Voltage	V_{AIN}		V_{SS}	—	V_{AREF}	V
Analog Supply current	I_{REF}		—	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V	—	—	± 1	LSB
Zero Point Error			—	—	± 1	
Full Scale Error			—	—	± 1	
Total Error			—	—	± 2	

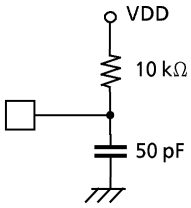
AC Characteristics

(V_{SS} = 0 V, Topr = – 30 to 70°C)

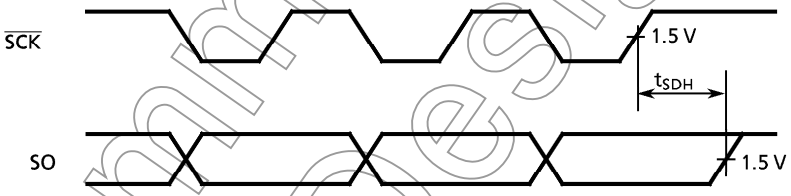
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Instruction Cycle Time	t_{cy}	V_{DD} = 4.5 to 6.0 V	1.3	—	20	μs
		V_{DD} = 2.7 to 6.0 V	1.9			
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
AD Sampling Time	t_{AIN}		—	4	—	μs
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 0.3	—	—	μs

Note: Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)

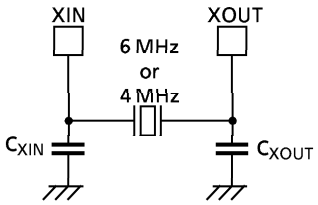


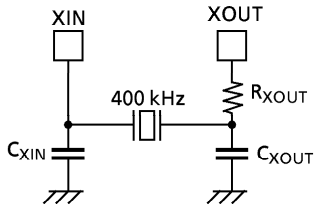
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 2.7 to 6.0 V, Topr = – 30 to 70°C)

(1) 6 MHz
Ceramic Resonator
CSA6. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF

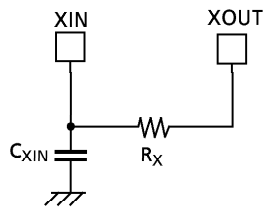
(2) 4 MHz
Ceramic Resonator
CSA4. 00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4. 00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30 pF
FCR4.0M5 (TDK) $C_{XIN} = C_{XOUT}$ = 33 pF
Crystal Oscillator
204B-6F 4. 0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20 pF





(3) 400 kHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220 pF, R_{XOUT} = 6.8 kΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100 pF, R_{XOUT} = 10 kΩ

(4) RC Oscillation (V_{SS} = 0 V, V_{DD} = 5.0 V, Topr = 25°C)
2 MHz (typ.) C_{XIN} = 33 pF, R_X = 10 kΩ
400 kHz (typ.) C_{XIN} = 100 pF, R_X = 26 kΩ



Typical Characteristics