TOSHIBA

TOSHIBA Original CMOS 4-Bit Microcontroller

TLCS-47 Series

TMP47C206MG
TMP47C206PG

TOSHIBA CORPORATION

Semiconductor Company

Document Change Notification

The purpose of this notification is to inform customers about the launch of the Pb-free version of the device. The introduction of a Pb-free replacement affects the datasheet. Please understand that this notification is intended as a temporary substitute for a revision of the datasheet.

Changes to the datasheet may include the following, though not all of them may apply to this particular device.

1. Part number

   Example: TMPxxxxxxF → TMPxxxxxxFG

   All references to the previous part number were left unchanged in body text. The new part number is indicated on the prelims pages (cover page and this notification).

2. Package code and package dimensions

   Example: LQFP100-P-1414-0.50C → LQFP100-P-1414-0.50F

   All references to the previous package code and package dimensions were left unchanged in body text. The new ones are indicated on the prelims pages.

3. Addition of notes on lead solderability

   Now that the device is Pb-free, notes on lead solderability have been added.

4. RESTRICTIONS ON PRODUCT USE

   The previous (obsolete) provision might be left unchanged on page 1 of body text. A new replacement is included on the next page.

5. Publication date of the datasheet

   The publication date at the lower right corner of the prelims pages applies to the new device.

1. Part number

2. Package code and dimensions

Previous Part Number (in Body Text)	Previous Package Code (in Body Text)	New Part Number	New Package Code	OTP
TMP47C206P	P-DIP20-300-2.54A	TMP47C206PG	DIP20-P-300-2.54A	TMP47P206VPG
TMP47C206M	P-SOP20-300-1.27	TMP47C206MG	SOP20-P-300-1.27	TMP47P206VMG

*: For the dimensions of the new package, see the attached Package Dimensions diagram.

3. Addition of notes on lead solderability

The following solderability test is conducted on the new device.

Lead solderability of Pb-free devices (with the G suffix)

Test	Test Conditions	Remark
Solderability	(1) Use of Lead (Pb) ·solder bath temperature = 230°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux (2) Use of Lead (Pb)-Free ·solder bath temperature = 245°C ·dipping time = 5 seconds ·the number of times = once ·use of R-type flux	Leads with over 95% solder coverage till lead forming are acceptable.

4. RESTRICTIONS ON PRODUCT USE

The following replaces the "RESTRICTIONS ON PRODUCT USE" on page 1 of body text.

RESTRICTIONS ON PRODUCT USE 20070701-EN

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc.
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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

5. Publication date of the datasheet

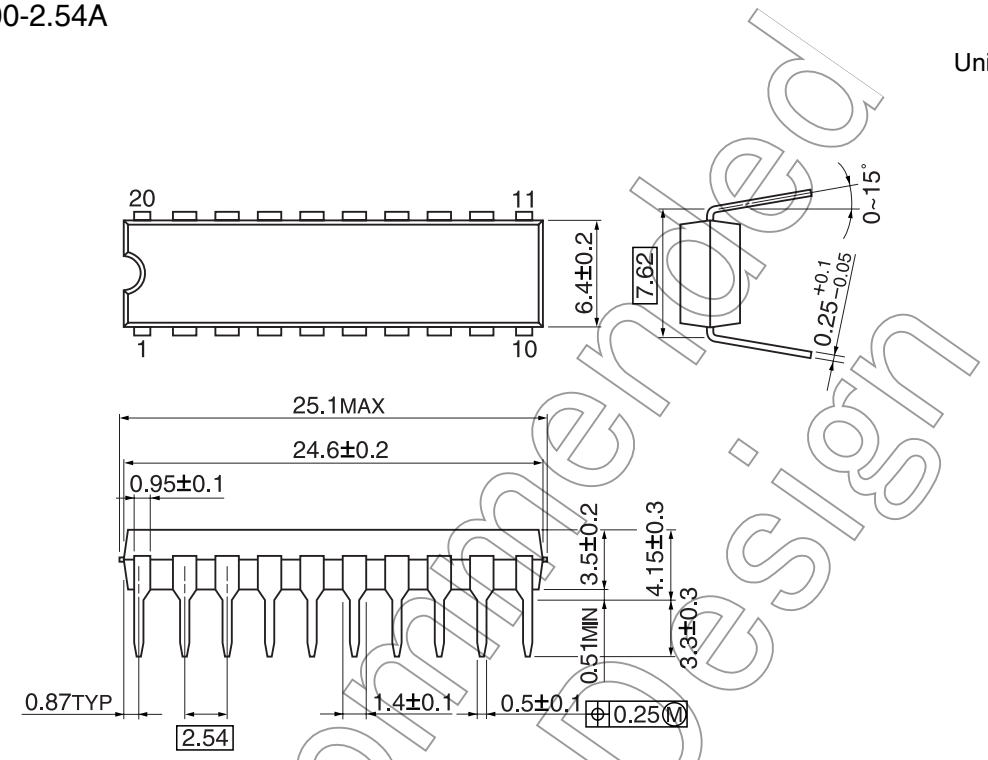
The publication date of this datasheet is printed at the lower right corner of this notification.

(Annex)

Package Dimensions

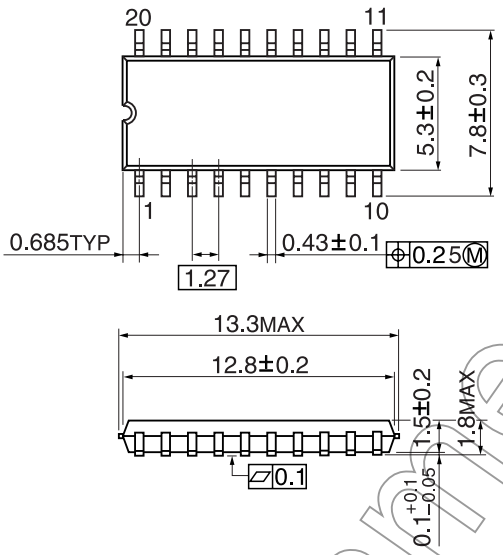
DIP20-P-300-2.54A

Unit: mm



SOP20-P-300-1.27

Unit: mm



CMOS 4-Bit Microcontroller

TMP47C206M/P

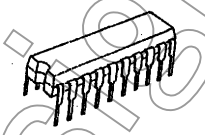
The TMP47C206 has Low Voltage Detector, Pulse output, Zero-cross detector based on the TLCS-470 series.

Part No.	ROM	RAM	Package	OTP
TMP47C206P	2048 × 8-bit	128 × 4-bit	P-DIP20-300-2.54A	TMP47P206VP
TMP47C206M			P-SOP20-300-1.27	TMP47P206VM –

Features

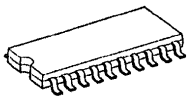
- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time: 1.0 μs (at 8 MHz)
- ◆ 90 basic instructions
  Instruction set is the same as TLCS-470 series
- ◆ Table look-up instructions
- ◆ Subroutine nesting: 15 levels max
- ◆ 5 interrupt sources (External: 2, Internal: 3)
  All sources have independent latches each,and selectable priority exists for external interrupts
- ◆ I/O port (15pins including 3 Tri-state I/O ports)
- ◆ Two 12-bit Timer/Counters
  Timer,event counter,and pulse width measurement mode
- ◆ Interval Timer
- ◆ Watchdog Timer
- ◆ Pulse output
  Buzzer drive/carrier for remote controller
- ◆ RESET Output
- ◆ Zero-cross detector interrupt (Wake-Up possible in HOLD mode)
- ◆ Low Voltage Detector
- ◆ High current outputs
  LED direct drive capability or TRIAC control:
  typ.20 mA × 5 bits (Port 4, R50)
- ◆ Hold function
  Battery/Capacitor back-up
- ◆ Real Time Emulator: BM47C206

P-DIP20-300-2.54A



TMP47C206P

P-SOP20-300-1.27

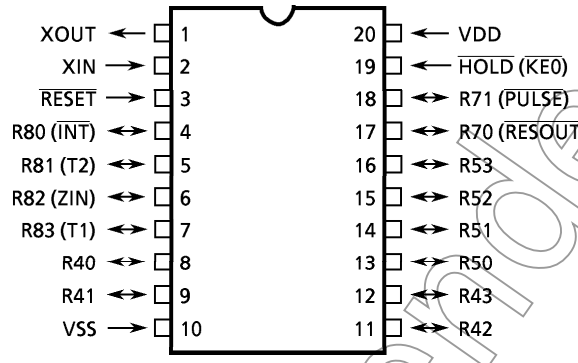


TMP47C206M

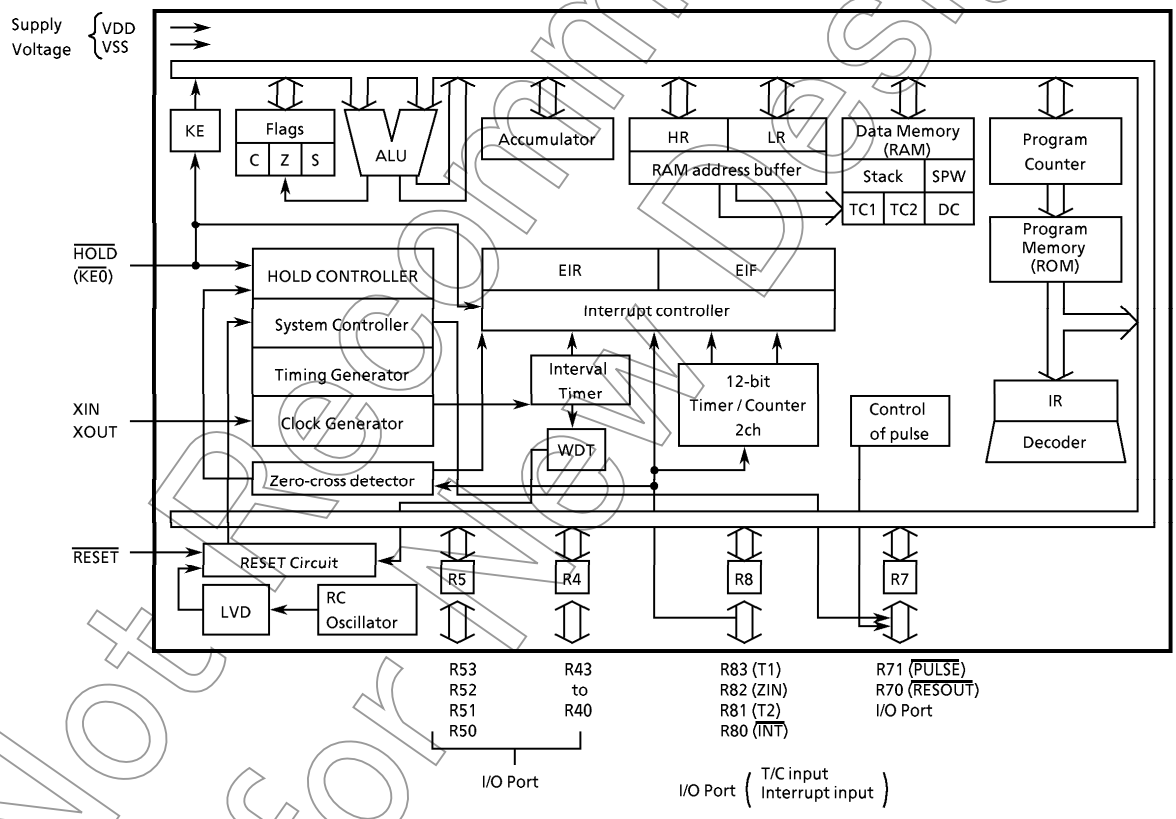
000707EBA1

Pin Assignment

P-DIP20-300-2.54A / P-SOP20-300-1.27



Block Diagram



Pin Function

Pin Name	Input / Output	Functions	
R43 to R40	I/O (Output)	4-bit I/O port with latch (R7 port has only 2-bit). When used as input port,the latch must be set to "1". Every bit data is possible to be set,cleared and tested by the bit manipulation instruction of the L-register indirect addressing.	High Current Port
R53 to R51			Tri-State port
R50			High Current port
R71 ($\overline{\text{PULSE}}$)			Pulse output
R70 ($\overline{\text{RESOUT}}$)			Reset signal output
R83 (T1)	I/O (Input)	4-bit I/O port with latch. When used as input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	Timer / Counter 1 external input
R82 (ZIN)			zero-cross interrupt input
R81 (T2)			Timer / Counter 2 external input
R80 ($\overline{\text{INT}}$)			External interrupt input
XIN	Input	Resonator connecting pins.	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	Input	Reset signal input	
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)	Hold request / release signal input	Sense input
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	

Operational Description

1. System Configuration

- Internal CPU Function
  - 2.1 Program Counter (PC)
  - 2.2 Program Memory (ROM)
  - 2.3 H Register, L Register
  - 2.4 Data Memory (RAM)
    - Stack
    - Stack Pointer Word (SPW)
    - Data Counter (DC)
  - 2.5 ALU and Accumulator
  - 2.6 Flags
  - 2.7 System Controller
  - 2.8 Interrupt Function
  - 2.9 Reset Circuit
    - Reset Output
    - Low Voltage Detector
- Peripheral Hardware Function
  - 3.1 I/O Ports
  - 3.2 Interval Timer
  - 3.3 Timer / Counters (TC1, TC2)
  - 3.4 Watchdog Timer
  - 3.5 Pulse Output
  - 3.6 Zero-cross detector

2. Internal CPU Function

2.1 Program Counter (PC)

The program counter is a 11-bit binary counter which indicates the address of the program memory storing the next instruction to be executed. Normally, the PC is incremented by the number of bytes of the instruction every time it is fetched. When a branch instruction or a subroutine instruction has been executed or an interrupt has been accepted, the specified values listed in Table 2-1 are set to the PC. The PC is initialized to "0" during reset.

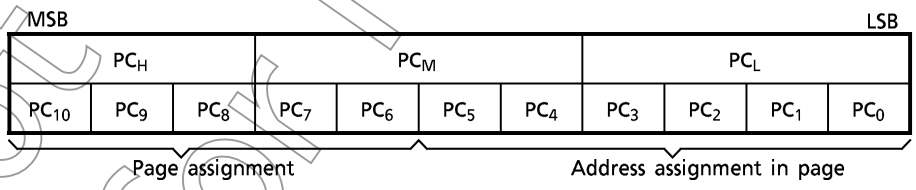


Figure 2-1. Configuration of Program Counter

The PC can directly address a 2048-byte address space. However, with the short branch, the following points must be considered:

- Short branch instruction [BSS a]
  In [BSS a] instruction execution, when the branch condition is satisfied, the value specified in the instruction is set to the lower 6 bits of the PC. That is, [BSS a] becomes the in-page branch instruction. When [BSS a] is stored at the last address of the page, the upper 5 bits of the PC point the next page, so that branch is made to the next page.

Table 2-1. Status Change of Program Counter

Instruction or Operation		Condition		Program Counter (PC)										
				PC_{10}	PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0
Execution of Instruction	BS a	SF = 1 (Branch condition is satisfied)		Immediate data specified by the instruction										
		SF = 0 (Branch condition is not satisfied)		+ 2										
	BSS a	SF = 1	Lower 6-bit address ≠ 111111	Hold							Immediate data specified by the instruction			
			Lower 6-bit address = 111111 (last address in page)	+ 1							Immediate data specified by the instruction			
		SF = 0		+ 1										
	CALL a			Immediate data specified by the instruction										
	CALLS a			0	0	0	The data generated by the immediate data specified by the instruction					1	1	0
	RET			The return address restored from stack										
	RETI			The return address restored from stack										
	Others			Incremented by the number of bytes in the instruction										
Interrupt acceptance				0	0	0	0	0	0	0	Interrupt vector			0
Reset				0	0	0	0	0	0	0	0	0	0	0

2.2 Program Memory (ROM)

Programs and fixed data are stored in the program memory. The instruction to be executed next is read from the address indicated by the contents of the PC.
The fixed data can be read by using the table look-up instructions.

- Table look-up instructions
  [LDL A, @DC], [LDH A, @DC+]

  The table look-up instructions read the lower and upper 4 bits of the fixed data stored at the address specified in the data counter (DC) to place them into the accumulator. [LDL A, @DC] instruction reads the lower 4 bits of fixed data, and [LDH A, @DC+] instruction reads the upper 4 bits.
  The DC is a 12-bit register, allowing it to address the entire program memory space.

  Example: When [LDL A, @DC] instruction is executed with the DC value being $7A0_H$ and the contents of program memory address $7A0_H$ being 58_H, "8" is stored in the accumulator; when [LDH A, @DC+] instruction is executed, "5" is stored in the accumulator and the DC value is incremented to $7A1_H$.

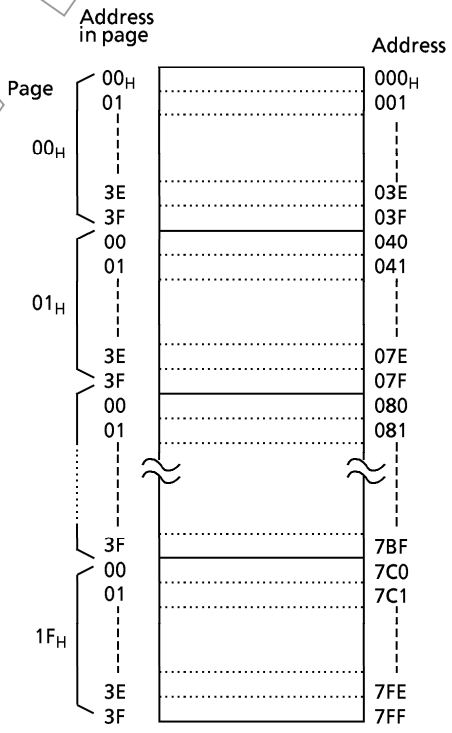


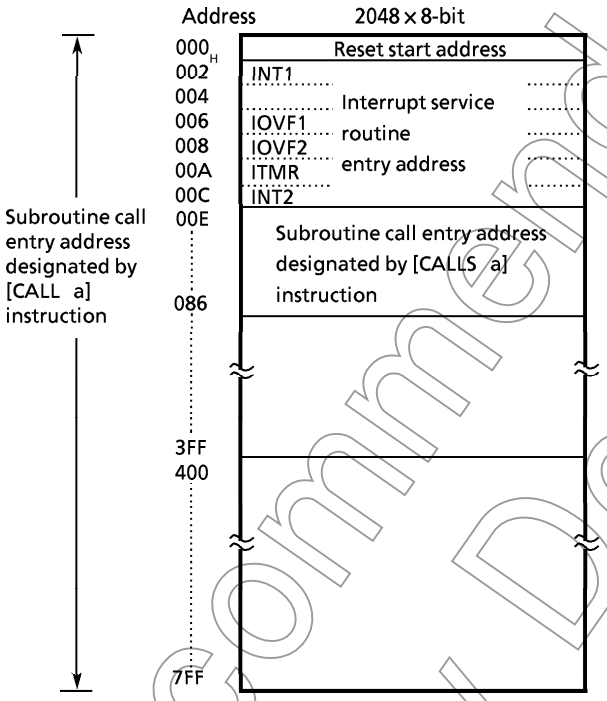
Figure 2-2. Configuration of Program Memory

2.2.1 Program Memory Capacity

The TMP47C206 has 2048 × 8 bits (addresses 000_H through $7FF_H$) of program memory (mask ROM).

2.2.2 Program Memory Map

Figure 2-3 shows the program memory map. Address 000_H to 086_H of the program memory are also used for special purposes.



Note: Address 004_H and 005_H can be used to store ordinary user's processing data.

Figure 2-3. Program Memory Map

2.3 H Register and L Register

The H register and the L register are 4-bit general registers. They are also used as a register pair (HL) for the data memory (RAM) addressing pointer. The RAM consists of pages, each page being 16 words long (1 word = 4 bits). The H register specifies a page and the L register specifies an address in the page.

The L register has the auto-post-increment/decrement capability, implementing the execution of composite instructions. For example, [ST A, @HL+] instruction automatically increments the contents of the L register after data transfer.

During the execution of [SET @L], [CLR @L], or [TEST @L] instructions, the L register is also used to specify the bits corresponding to I/O port pins R53-R40, R70, R71 (the indirect addressing of port bits by the L register).

Example: To write immediate values "5" and "F_H" to data memory addresses 10_H and 11_H.

```
LD      HL,#10H          ;  HL←10H
ST      #5,@HL+          ;  RAM[10H]←5H, LR←LR+1
ST      #0FH,@HL+        ;  RAM[11H]←FH, LR←LR+1
```

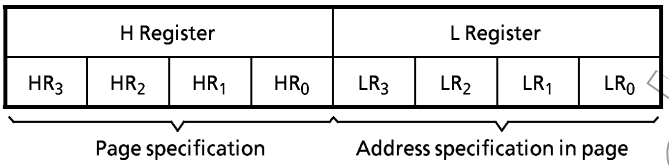


Figure 2-4. Configuration of H and L Registers

2.4 Data Memory (RAM)

The TMP47C206 has 128 × 4 bits (addresses 00_H through $7F_H$) of the data memory (RAM).

There are three ways to address the data memory.

(1) Register-indirect addressing mode

In this mode, a page is specified by the H register and an address in the page by the L register.

Example: LD A, @HL ; Acc←RAM [HL]

(2) Direct addressing mode

In this mode, an address is directly specified by the 8 bits of the second byte (operand) in the instruction field.

Example: LD A, 2CH ; Acc←RAM [$2C_H$]

(3) Zero-page addressing mode

In this mode, an address in zero-page (addresses 00_H through $0F_H$) is specified by the lower 4 bits of the second byte (operand) in the instruction field.

Example: ST #3, 05H ; RAM [05_H] ←3

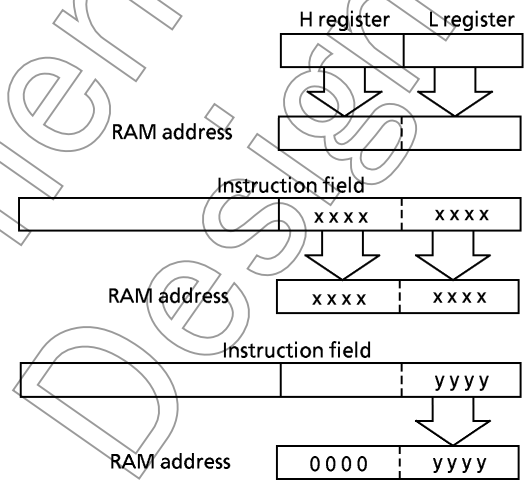
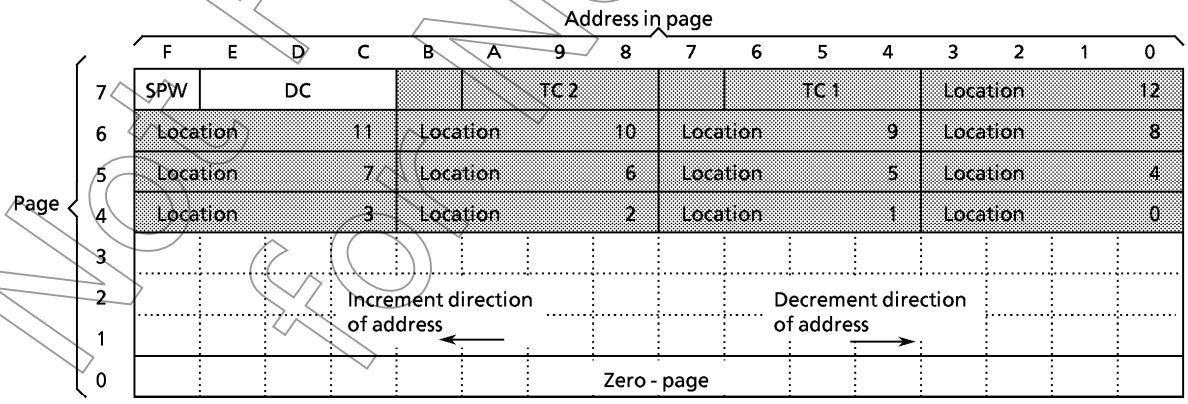


Figure 2-5. Addressing mode

2.4.1 Data Memory Map

Figure 2-6 shows the data memory map. The data memory is also used for the following special purpose.

① Stack and Stack Pointer Word (SPW)
② Data Counter (DC)
③ Count registers of the timer / counters (TC1, TC2)
④ Zero-page



Note 1: ▨ *denotes the stack area.*
Note 2: *The TC1 and TC2 areas are shared by the locations 13 and 14.*

Figure 2-6. Data Memory Map (TMP47C206)

(1) Stack

The stack provides the area in which the return address is saved before a jump is performed to the processing routine at the execution of a subroutine call instruction or the acceptance of an interrupt. When a subroutine call instruction is executed, the contents (the return address) of the program counter are saved; when an interrupt is accepted, the contents of the program counter and flags are saved.

When returning from the processing routine, executing the subroutine return instruction [RET] restores the contents of the program counter from the stack; executing the interrupt return instruction [RETI] restores the contents of the program counter and flags.

The stack consists of up to 15 levels (locations 0 through 14) which are provided in the data memory (addresses 40_H through $7B_H$). Each location consists of 4-word data memory. Locations 13 and 14 are shared with the count registers of the timer / counters (TC1, TC2) to be described later.

The save / restore locations in the stack are determined by the stack pointer word (SPW). The SPW is automatically decremented after save, and incremented before restore. That is, the value of the SPW indicates the stack location number for the next save.

(2) Stack Pointer Word (SPW)

Address $7F_H$ in the data memory is called the stack pointer word, which identifies the location in the stack to be accessed (save or restore).

Generally, location number 0 to 12 can be set to the SPW, providing up to 13 levels of stack nesting. Locations 13 and 14 are shared with the timer / counters to be described later; therefore, when the timer / counters are not used, the stack area of up to 15 levels is available. Address $7F_H$ is assigned to the SPW, so that the contents of the SPW cannot be set "15" in any case.

The SPW is automatically updated when a subroutine call is executed or an interrupt is accepted. However, if it is used in excess of the stack area permitted by the data memory allocating configuration, the user-processed data may be lost. (For example, when the user-processed data area is in an address range 00_H through $4F_H$, up to location 4 of the stacks are usable. If an interrupt is accepted with location 4 already used, the user-processed data stored in addresses $4C_H$ through $4F_H$ corresponding to the location 3 area is lost.)

The SPW is not initialized by hardware, requiring to write the initial value (the location with which the use of the stack starts) by using the initialization routine. Normally, the initial value of "12" is used.

Example: To initialize the SPW (when the stack is used from location 12)

```
LD      A,#12       ;  SPW←12
ST      A,0FFH
```

(3) Data Counter (DC)

The data counter is a 12-bit register to specify the address of the data table to be referenced in the program memory (ROM). Data table reference is performed by the table look-up instructions [LDL A, @DC] and [LDH A, @DC+]. The data table may be located anywhere within the program memory address space.

The DC is assigned with a RAM address in unit of 4 bits. Therefore, the RAM manipulation instruction is used to set the initial value or read the contents of the DC.

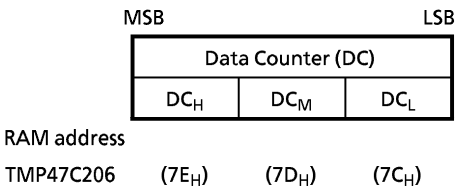


Figure 2-7. Data Counter

Example: To set the DC to 380_H.

```
LD      HL,#07CH    ;  Sets RAM address of DCL to HL register pair.
ST      #0H,@HL+    ;  DC ← 380H
ST      #8H,@HL+
ST      #3H,@HL+
```

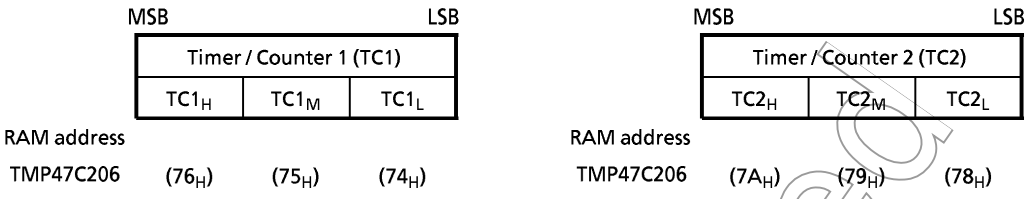


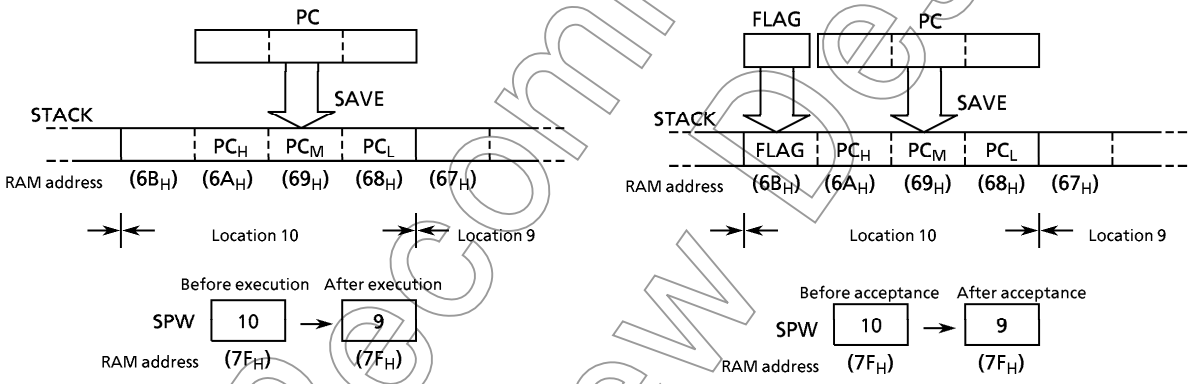
Figure 2-8. Count Registers of the Timer / Counters (TC1, TC2)

(4) Count registers of the timer / counters (TC1, TC2)

The TMP47C206 has two channels of 12-bit timer / counters. The count register of the timer / counter is assigned with a RAM addresses in unit of 4 bits, so that the initial value is set and the contents are read by using the RAM manipulation instruction.

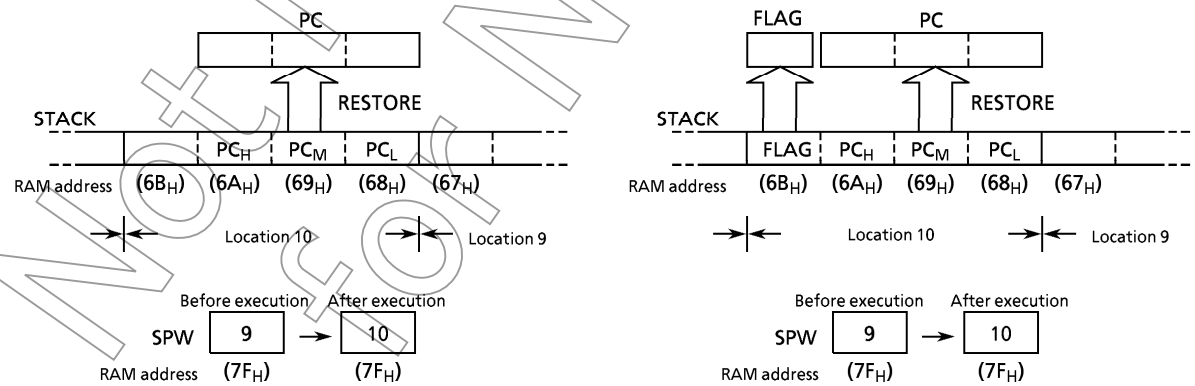
The count registers are shared with the stack area (locations 13 and 14) described before, so that the stack is usable from location 13 when the timer / counter 1 is not used. When none of timer / counter 1 and timer / counter 2 are used, the stack is usable from location 14.

When both timer / counter 1 and timer/counter 2 are used, the data memory locations at addresses 77_H and $7B_H$ can be used to store the user-processed data.



(a) At execution of the subroutine call instruction

(b) At acceptance of an interrupt



(c) At execution of the subroutine return instruction

(d) At execution of the interrupt return instruction

Figure 2-9. Accessing Stack (Save / Restore) at the TMP47C206

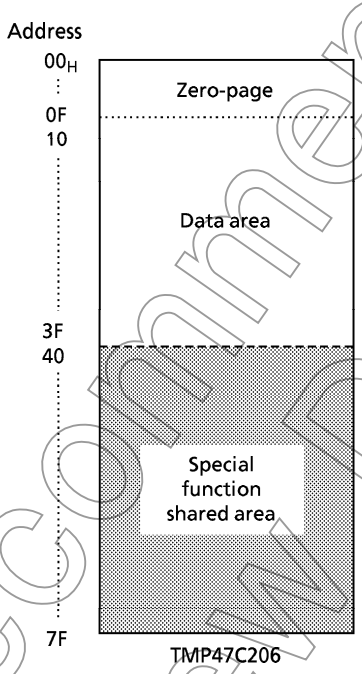
(5) Zero-page

The 16 words (at addresses 00_H through $0F_H$) of the zero page of the data memory can be used as the user flags or pointers by using zero-page addressing mode instructions (comparison, addition, transfer, and bit manipulation), providing enhanced efficiency in programming.

Example: To write immediate data "8" to address 09_H if bit 2 at address 04_H in the RAM is "1".

```
        TEST    04H,2       ;  Skips if bit 2 at address 04H in the RAM is "0".
        B       SKIP
        ST      #8,09H      ;  Writes "8" to address 09H in the RAM
SKIP:
```

2.4.2 Data Memory Capacity



Note: The technical data sheets for the TMP47P206V shall also be referred to.

Figure 2-10. Data Memory Capacity and Address Assignment

When power-on is performed, the contents of the RAM become unpredictable, so that they must be initialized by the initialization routine.

Example: To clear RAM (use common to the TMP47C206)

```
        LD      HL, #00H        ;  HL←00H
SCLRRAM:ST      #0, @HL+        ;  RAM [HL] ←0, LR←LR + 1
        B       SCLRRAM
        ADD     H, #1           ;  HR←HR + 1
        CMPR    H, #7
        B       SCLRRAM
```

2.5 ALU and Accumulator

2.5.1 Arithmetic / Logic Unit (ALU)

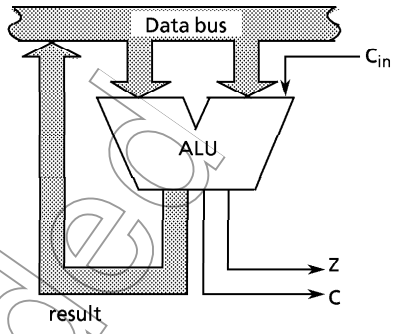
The ALU performs the arithmetic and logic operations specified by instructions on 4-bit binary data and outputs the result of the operation, the carry information (C), and the zero detect information (Z).

(1) Carry information (C)

The carry information indicates a carry-out from the most significant bit in an addition. A subtraction is performed as addition of two's complement, so that, with a subtraction, the carry information indicates that there is no borrow to the most significant bit. With a rotate instruction, the carry indicates the data shifted out from the accumulator.

(2) Zero detect information (Z)

This information is "1" when the operation result or the data to be transferred to the accumulator/data memory is "0000_B".



Note: C_{in} indicates the carry input specified by instruction

Figure 2-11. ALU

Example: The carry information and zero detect information for 4-bit additions and subtractions.

Operation	Result	C	Z	Operation	Result	C	Z
4 + 2 =	6	0	0	8 − 1 =	7	1	0
7 + 9 =	0	1	1	2 − 2 =	0	1	1
9 + 9 =	2	1	0	5 − 8 =	−3 (1101_B)	0	0

2.5.2 Accumulator (Acc)

The accumulator is a 4-bit register used to hold source data or results of the operations and data manipulations.

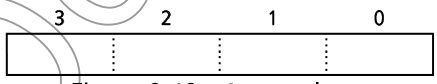


Figure 2-12. Accumulator

2.6 Flags

There are a carry flag (CF), a zero flag (ZF) and a status flag (SF), each consisting of 1 bit. These flags are set or cleared according to the condition specified by an instruction. When an interrupt is accepted, the flags are saved on the stack along with the program counter. When the [RETI] instruction is executed, the flags are restored from the stack to the states set before interrupt acceptance.

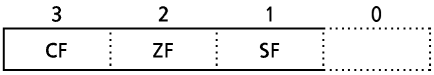


Figure 2-13. Flags

(1) Carry flag (CF)

The carry flag holds the carry information received from the ALU at the execution of an addition / subtraction with carry instruction, a compare instruction, or a rotate instruction. With a carry flag test instruction, the CF holds the value specified by it.

① Addition / subtraction with carry instructions [ADDC A, @HL], [SUBRC A, @HL]
The CF becomes the input (C_{in}) to the ALU to hold the carry information.

② Compare instructions [CMPR A, @HL], [CMPR A, #k]
The CF holds the carry information (non-borrow).

③ Rotate instructions [ROLC A], [RORC A]
The CF is shifted into the accumulator to hold the carry information (the data shifted out from the accumulator).

④ Carry flag test instructions [TESTP CF], [TEST CF]
With [TESTP CF] instruction, the content of the CF is transferred to the SF then the CF is set to "1".
With [TEST CF] instruction, the value obtained by inverting the content of the CF is transferred to the SF then the CF is cleared to "0".

(2) Zero flag (ZF)

The zero flag holds the zero detect information (Z) received from the ALU at the execution of an operational instruction, a rotate instruction, an input instrcution, or a transfer-to-accumulator instruction.

(3) Status flag (SF)

The status flag provides the branch condition for a branch instruction. Branch is performed when this flag is set to "1". Normally the SF is set to "1", so that any branch instruction can be regarded as an unconditional branch instruction. When a branch instruction is executed upon set or clear of the SF according to the condition specified by an instruction, this instruction becomes a conditional branch instruction. During reset, the SF is initialized to "1", other flags are not affected.

Example: When the following instructions are executed with the accumulator, H register, L register, data memory (address 07_H), and carry flag being set to "C_H", "0", "7", "5", and "1" respectively, the contents of the accumulator and flags become as follows:

Instruction	Acc after execution	Flag after execution		
		CF	ZF	SF
ADDC A, @HL	2_H	1	0	0
SUBRC A, @HL	9_H	0	0	0
CMPR A, @HL	C_H	0	0	1
AND A, @HL	4_H	1	0	1
LD A, @HL	5_H	1	0	1

Instruction	Acc after execution	Flag after execution		
		CF	ZF	SF
LD A, #0	0_H	1	1	1
ADD A, #4	0_H	1	1	0
DEC A	B_H	1	0	1
ROLC A	9_H	1	0	0
RORC A	E_H	0	0	1

2.7 System Controller

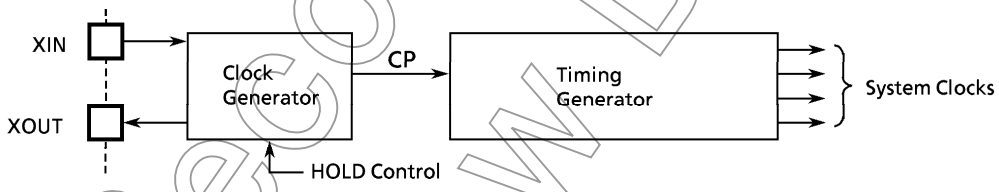
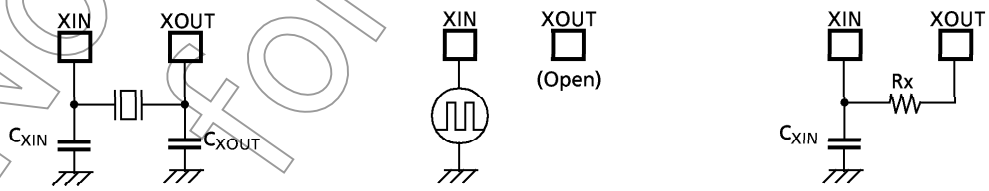


Figure 2-14. Clock Generator and Timing Generator

2.7.1 Clock Generator

The clock generator provides the basic clock pulse (CP) by which the system clock to be supplied to the CPU and the peripheral hardware is produced. The CP can be easily obtained by connecting the resonator to the XIN and XOUT pins. (RC oscillation is also possible, depending on the mask option) The clock from the external oscillator is also available. In the hold operating mode, the clock generator stops oscillating.



(a) Crystal or ceramic resonator (b) External oscillator (c) RC oscillation (mask option)

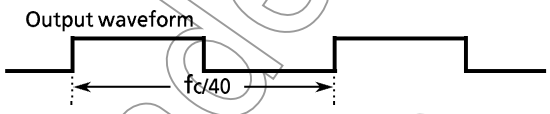
Figure 2-15. Examples of Oscillator Connection

Note: Accurate adjustment of the oscillation frequency

Although the hardware to monitor the CP externally and directly is not provided, the oscillation frequency can be adjusted by making the program to output the pulse with a fixed frequency to the port with the all interrupts disabled and timer/counters stopped and monitoring this pulse. With a system requiring the oscillation frequency adjustment, the adjusting program must be created beforehand.

Example: To output the oscillation frequency adjusting monitor pulse to port R40.

```
SFCCHK:   SET    %OP04,0
          CLR    %OP04,0
          BSS    SFCCHK
```



2.7.2 Timing Generator

The timing generator produces the system clocks from basic clock pulse (CP) which are supplied to the CPU and the peripheral hardware.

The timing generator consists of a 18-stage binary counter with a divided-by-16 prescaler. The basic clock (frequency: fc) provides the prescaler. Therefore, the output frequency at the last stage is $fc/2^{22}$[Hz]. During reset, the binary counter is cleared to "0", however, the prescaler is not cleared.

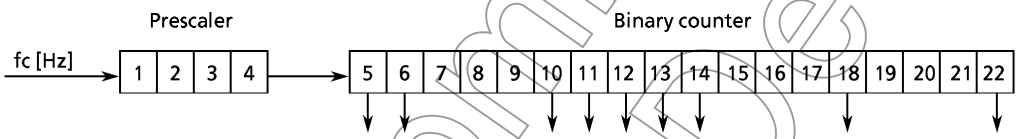


Figure 2-16. Configuration of Interval Timer

The timing generator provides the following functions:

① Generation of an internal source clock for interval timer
② Generation of an internal source clock for timer / counters
③ Generation of a warm-up time for releasing of the hold operating mode
④ Source clock for a Pulse output
⑤ Source clock for a Watchdog timer

2.7.3 Instruction Cycle

The instruction execution and the on-chip peripheral hardware operations are performed in synchronization with the basic clock pulse (CP: fc [Hz]). The smallest unit of instruction execution is called an instruction cycle. The instruction set consists of 1-cycle instructions and 2-cycle instructions. The former requires 1 cycle for their execution; the latter, 2 cycles. Each instruction cycle consists of 4 states (S1 through S4). Each state consists of 2 basic clock pulses. In the TMP47C206, [BSL a] instruction can not be used.

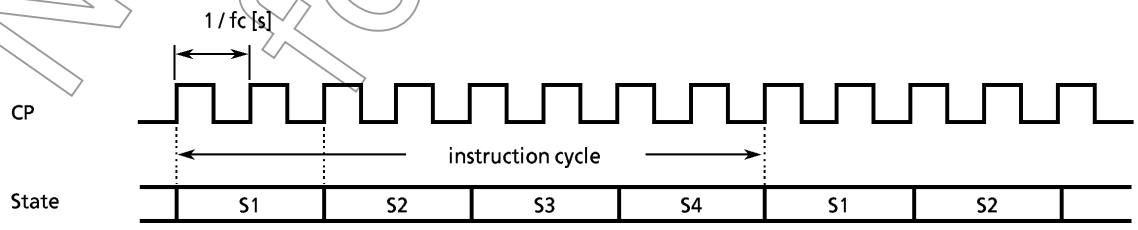


Figure 2-17. Instruction Cycle

2.7.4 Hold Operating Mode

The hold feature stops the system and holds the system's internal states active before to stop and enter a low power mode. The hold operation is controlled by the command register (OP10) and the $\overline{\text{HOLD}}$ pin input. The $\overline{\text{HOLD}}$ pin input state can be known by the status register (IP0E). The $\overline{\text{HOLD}}$ pin is shared with the $\overline{\text{KE0}}$ pin.

(1) Starts Hold Operating Mode

The hold operating mode consists of the level-sensitive release mode and the edge-sensitive release mode. The hold operation is started when the command is set to the command register and holds the following states during the hold operation:

① The oscillator stops and the system's internal operations are all held up.
② The timing generator is cleared to "0".
③ The states of the data memory, registers, and latches value are kept during the HOLD mode.
④ The program counter holds the address of the instruction to be executed after the instruction ([OUT A, %OP10] or [OUT @HL, %OP10]) which starts the hold operating mode.

Hold operating mode command register
(Port address: OP10, Initial value: *0**)

3	2	1	0
HLDMS		HWUT	

HLDMS	Starts hold operation
01:	Starts hold operation in edge-release mode
11:	Starts hold operation in level-release mode
*0:	(Unused)

HWUT	Warm-up time at release of the hold
	Example: At fc = 8 MHz
00:	2^{18}/fc [s] ..... 32.75 [ms]
01:	2^{14}/fc 2.05
10:	(Unused)
11:	2^{6}/fc 0.008

Hold operating mode status register
(Port address: IP0E)

3	2	1	0
(undefined)			HOLD (KE0)

HOLD	$\overline{\text{HOLD}}$ pin input state
0:	$\overline{\text{HOLD}}$ pin is high
1:	$\overline{\text{HOLD}}$ pin is low

*Note 1: *; Don't care*
Note 2: Do not access the OP10 when HOLD mode is not used.
Note 3: An undefined value is read from bit1 to bit3 of the IP0E with an input instruction.
Note 4: When R82 (ZIN) is used as HOLD release Don't use KE0 port as input.

Figure 2-18. Hold Operating Mode Command Register / Status Register

CAUTION: Minimum warm-up time depends upon oscillator characteristics. Please check carefully the electrical specification of your oscillator.

a. Level-sensitive release (back-up) mode

In this mode, the hold operation is released by setting the $\overline{\text{HOLD}}$ pin to the high level. This mode is used for the capacitor backup while power supply is off or for the battery backup for long hours.
If the instruction to start the hold operation is executed with the $\overline{\text{HOLD}}$ pin input being high, the hold operation does not start but the release sequence (warm-up) starts immediately. Therefore, to start the hold operation in the level-sensitive release mode, the low level on $\overline{\text{HOLD}}$ pin (the hold operation request) must be detected in the program. This detection is performed in one of the two ways below:

① Testing HOLD (bit 0 of the status register)
② Applying the $\overline{\text{HOLD}}$ pin input also to $\overline{\text{INT}}$ pin to generate an external interrupt 1 request.

Example: To test HOLD to start the hold operation in the level-sensitive release mode (the warm-up time = 2^{14}/fc).

```
SHOLDH: TEST    %IP0E, 0    ;  Waits until HOLD pin input goes low.
        B       SHOLDH
        LD      A, #1101B   ;  OP10←1101B
        OUT     A, %OP10
```

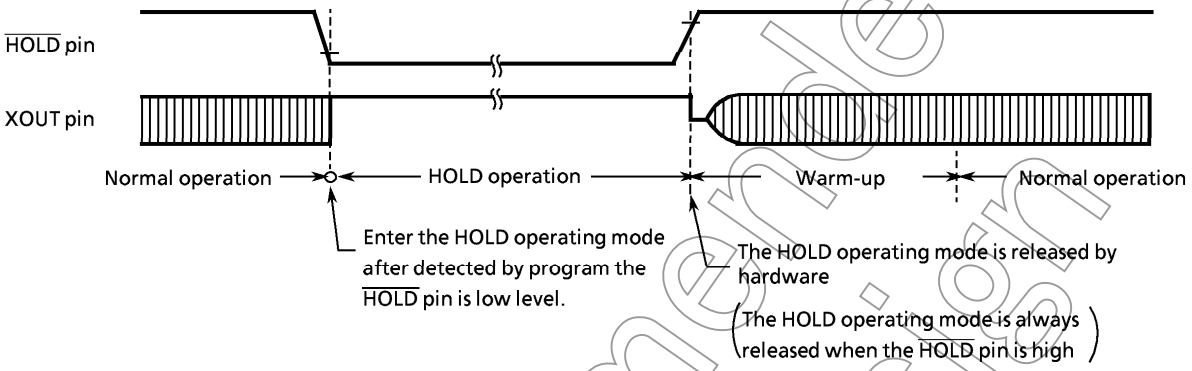


Figure 2-19. Level-sensitive release mode

b. Edge-sensitive release (clock) mode

In this mode, the hold operation is released at the rising edge of the HOLD pin input. This mode is used for applications in which a relatively short-time program processing is repeated at a certain cycle. This cyclic signal (for example, the clock supplied from the low power dissipation oscillator is input to HOLD pin). In the edge-sensitive mode, even if the HOLD pin input is high, the hold operation is performed.

Example: To start the hold operation in the edge-sensitive release mode (the warm-up time = 2^{14}/fc).

```
        LD      A, #0101B   ;  OP10←0101B
        OUT     A, %OP10
```

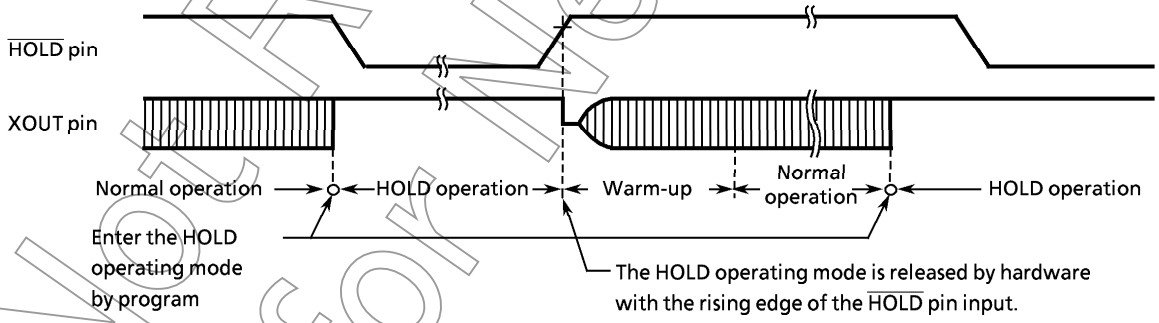


Figure 2-20. Edge-sensitive release mode

Note 1: In the hold operation, the dissipation of the power associated with the oscillator and the internal hardware is lowered; however, the power dissipation associated with the pin interface (depending on the external circuitry and program) is not directly determined by the hardware operation of the hold feature. This point should be considered in the system design and the interface circuit design.

Note 2: In the CMOS circuitry, a current does not flow when the input level is stable at the power voltage level (V_{DD} / V_{SS}); however, when the input level gets higher than the power voltage level (by approximately 0.3 to 0.5 V), a current begins to flow. Therefore, if cutting off the output transistor at an I/O port (the open drain output pin with an input transistor connected) puts the pin signal into the high-impedance state, a current flows across the ports input transistor, requiring to fix the level by pull-up or other means.

(2) Releases of the Hold Operating Mode

The hold operating mode is released in the following sequence:

① The oscillator starts

② Warm-up is performed in order to wait for oscillation to stabilize. During the warm-up , all the internal operations are stopped. One of three warm-up delays can be selected by program depending on the characteristics of the oscillator used.

③ When the warm-up time has elapsed, normal operation restarts from the instruction next to the instruction which starts the hold operation. At this time, the interval timer starts from the reset state "0".

The warm-up time is obtained by dividing the basic clock by the interval timer, so that, if the frequency at releasing the hold operation is unstable, the warm-up time shown in Figure 2-18 includes an error. Therefore, the warm-up time must be handled as an approximate value. The hold operation is also released by setting the $\overline{\text{RESET}}$ pin to the low level. In this case, the normal reset operation follows immediately.

Note: To release the hold operation at a low voltage, the following points must be considered:
When the power voltage rises from the hold voltage to the operating voltage, the $\overline{\text{RESET}}$ pin input is also at the high level and its voltage rises with the power voltage.
In this case, if a time-constant circuit or the like is externally attached, the voltage rise of the $\overline{\text{RESET}}$ pin input occurs after the power voltage rise. If the voltage level of the $\overline{\text{RESET}}$ pin input gets under the non-inverted high input voltage of the $\overline{\text{RESET}}$ pin input (the hysteresis input), a reset operation may happen.

2.8 Interrupt Function

2.8.1 Interrupt Controller

There are 5 interrupt sources (2 external and 3 internal). The prioritized multiple interrupt capability is supported. The interrupt latches (IL_5 through IL_0) to hold interrupt requests are provided for the interrupt sources. Each interrupt latch is set to "1" when an interrupt request is made, asking the CPU to accept the interrupt. The acceptance of interrupt can be permitted or prohibited by program through the interrupt enable master flip-flop (EIF) and interrupt enable register (EIR). When two or more interrupts occur simultaneously, the one with the highest priority determined by hardware is serviced first.

Table 2-2. Interrupt Sources

Interrupt Source		OP07	Priority	Interrupt Latch	Enable conditions	Entry address
External	External Interrupt $\overline{\text{INT}}$ (INT1)	x0xx	(highest) 1	IL_5	EIF = 1	002_H
	External Interrupt ZIN (INT1)	x1xx				
Internal	TC1 overflow Interrupt (IOVF1)	–	2	IL_3	EIF = 1, EIR_2 = 1	006_H
	TC2 overflow Interrupt (IOVF2)	–	3	IL_2	EIF = 1, EIR_1 = 1	008_H
	Interval Timer Interrupt (ITMR)	–	4	IL_1		$00A_H$
External	External Interrupt ZIN (INT2)	x0xx	(lowest) 5	IL_0	EIF = 1, EIR_0 = 1	$00C_H$
	External Interrupt $\overline{\text{INT}}$ (INT2)	x1xx				

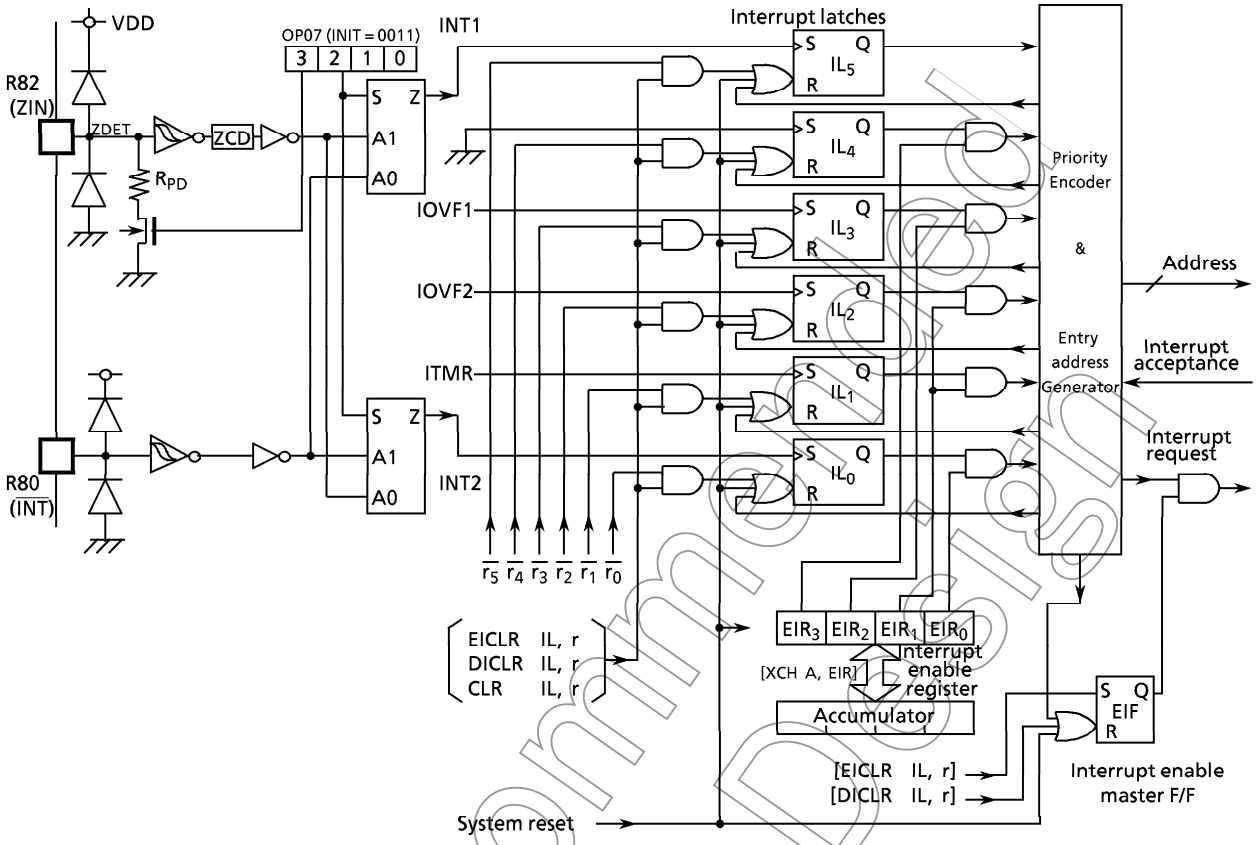


Figure 2-21. Interrupt Controller Block Diagram

(1) Interrupt enable master flip-flop (EIF)

The EIF controls the enable / disable of all interrupts. When this flip-flop is cleared to "0", all interrupts are disabled; when it is set to "1", the interrupts are enabled.

When an interrupt is accepted, the EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts. When the interrupt service program has been executed, the EIF is set to "1" by the execution of the interrupt return instruction [RETI], being put in the enabled state again.

Set or clear of the EIF in program is performed by instructions [EICLR IL, r] and [DICLR IL, r], respectively. The EIF is initialized to "0" during reset.

(2) Interrupt enable register (EIR)

The EIR is a 4-bit register specifies the enable or disable of each interrupt except INT1. An interrupt is enabled when the corresponding bit of the EIR is "1", and an interrupt is disabled when the corresponding bit of the EIR is "0". Bit 1 of the EIR (EIR_1) is shared by both IOVF2 and ITMR interrupts.

Read/write on the EIR is performed by executing [XCH A, EIR] instruction. The EIR is initialized to "0" during reset.

(3) Interrupt latch (IL_5 through IL_0)

An interrupt latch is provided for each interrupt source. The IL is set to "1" when an interrupt request is made to ask the CPU for accepting the interrupt. Each IL is cleared to "0" upon acceptance of the interrupt. It is initialized to "0" during reset.

The ILs can be cleared independently by interrupt latch operation instructions ([EICLR IL, r], [DICLR IL, r], and [CLR IL, r]) to make them cancel interrupt requests or initialize by program. When the value of instruction field (r) is "0", the interrupt latch is cleared; when the value is "1", the IL is held. Note that the ILs cannot be set by instruction.

Example 1: To enable IOVF1, INT1, and INT2 interrupts.

```
LD      A,#0101B    ;  EIR←0101B
XCH     A,EIR
EICLR   IL,111111B  ;  EIF←1
```

Example 2: To set the EIF to "1", and to clear the interrupt latches except ITMR to "0".

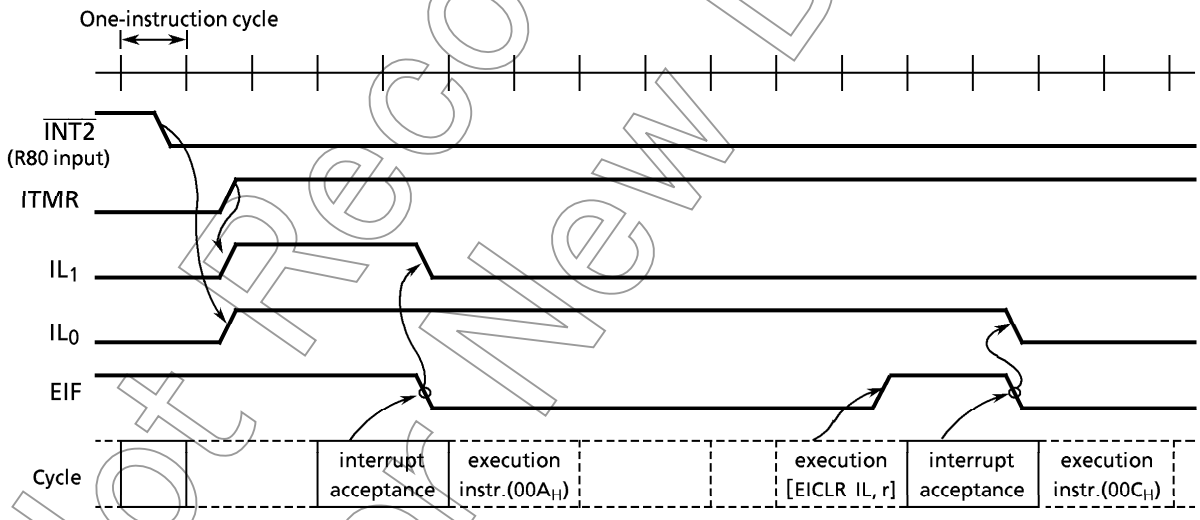
```
EICLR   IL,000010B  ;  EIF←1, IL0←0, IL2 – IL5←0
```

2.8.2 Interrupt Processing

An interrupt request is held until the interrupt is accepted or the IL is cleared by the reset or the interrupt latch operation instruction. The interrupt acknowledge processing is performed in 2 instruction cycles after the end of the current instruction execution (or after the timer/counter processing if any). The interrupt service program terminates upon execution of the interrupt return instruction [RETI].

The interrupt acknowledge processing consists of the following sequence:

① The contents of the program counter and the flags are saved on the stack.
② The interrupt entry address corresponding to the interrupt source is set to the program counter.
③ The status flag is set to "1".
④ The EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts.
⑤ The interrupt latch for the accepted interrupt source is cleared to "0".
⑥ The instruction stored at the interrupt entry address is executed. (Generally, in the program memory space at the interrupt entry address, the branch instruction to each interrupt processing program is stored.)



Note 1: It is assumed that there is no other interrupt request and EIR = 0011_B.
Note 2: The value r in the [EICLR IL, r] instruction is assumed as 111111_B.
Note 3: [ ] denotes the execution of an instruction.

Figure 2-22. Interrupt Timing chart (Example)

To perform the multi-interrupt, the EIF is set to "1" in the interrupt service program, and the acceptable interrupt source is selected by the EIR. However, for the INT1 interrupt, the interrupt service is disabled under software control because it is not disabled by the EIR.

Example: The INT1 interrupt service is disabled under software control (Bit 0 of RAM [05_H] are assigned to the disabling switch of interrupt service).

```
PINT1:  TEST    05H,0    ;  Skips if RAM [05H] 0 is "1"
        B       SINT1
        RETI
SINT1:   ⋮
```

The interrupt return instruction [RETI] performs the following operations:

① Restores the contents of the program counter and the flags from the stack.
② Sets the EIF to "1" to provide the interrupt enable state again.

In the interrupt processing, the program counter and flags are automatically saved or restored but the accumulator and other registers are not. If it is necessary to save or restore them, it must be performed by program as shown in the following example. To perform the multi-interrupt, the saving RAM area never be overlapped.

Example: To save and restore the accumulator and HL register pair.

```
XCH     HL, GSAV1      ;  RAM [GSAV1] ↔ HL
XCH     A, GSAV1 + 2   ;  RAM [GSAV1 + 2] ↔ Acc
```

Note: The lower 2 bits of GSAV1 should be "0's".

2.8.3 External Interrupts

When an external input (INT1 or INT2) occurs,the interrupt latch is set at the rising edge and falling edge of R82 pin input (INT1 or INT2). In the case of R80 pin input, the interrupt latch is set at the falling edge. The external interrupt input is the hysteresis type, each of high and low level time requires 2 or more instruction cycles for a correct interrupt operation.

The internal interrupt INT1 cannot be disabled by the EIR, so it is always accepted in the interrupt enable state (EIF = "1"). Therefore,when the external interrupt pin ($\overline{INT}$ or ZIN) correponding to INT1 is used for the I/O port, the interrupt return [RET I] instruction must be stored at the interrupt entry address to perform dummy interrupt processing.

The internal interrupt INT2 can be disabled by the EIR. When the external interrupt pin ($\overline{INT}$ or ZIN) corresponding to INT2 is used for the I/O port, EIR_0 should be set to "0" then interrupt is not requested.

2.9 Reset Function

When the RESET pin is held to the low level for 3 or more instruction cycles, or low voltage is detected or WDT counter overflowed, reset is performed to initialize the internal states.

When the RESET input goes high and Vdd is higher than V_{LV} (detection voltage by LVD) the reset status is cleared and program execution starts from address 000H.

The reset pin is a hysteresis input with pull-up resistor (220 kΩ typ.) and capacitance (10 pF typ.) and diode. Externally attaching a capacitor implement simplified power-on reset.

Table 2-3. Initialization of Internal registers after Reset Operation

On-chip hardware	Initial value	On-chip hardware	Initial value
Program counter (PC)	000_H	Output latch (I/O ports or Output ports)	Refer to "INPUT / OUTPUT Circuitry".
Status flag (SF)	1		
Interrupt enable master flip-flop (EIF)	0		
Interrupt enable register (EIR)	0_H	Command register	Refer to the description of each relative command register.
Interrupt latch (IL)	"0"		
Interval timer	"0"		

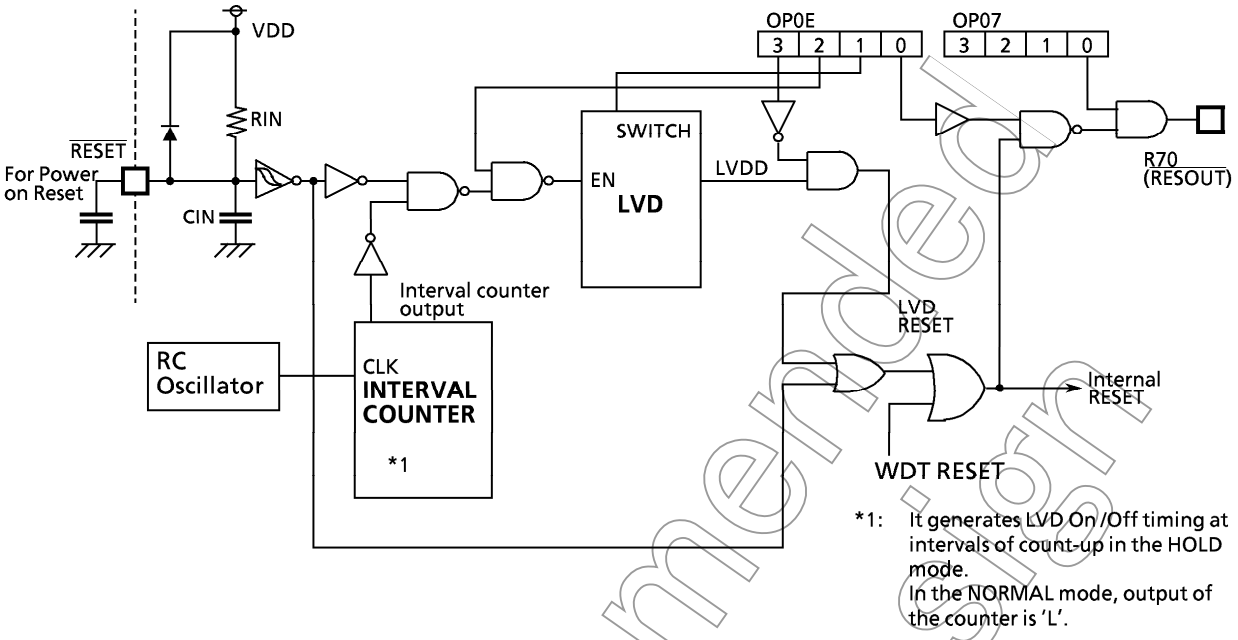


Figure 2-23. Block Diagram of Reset Circuit

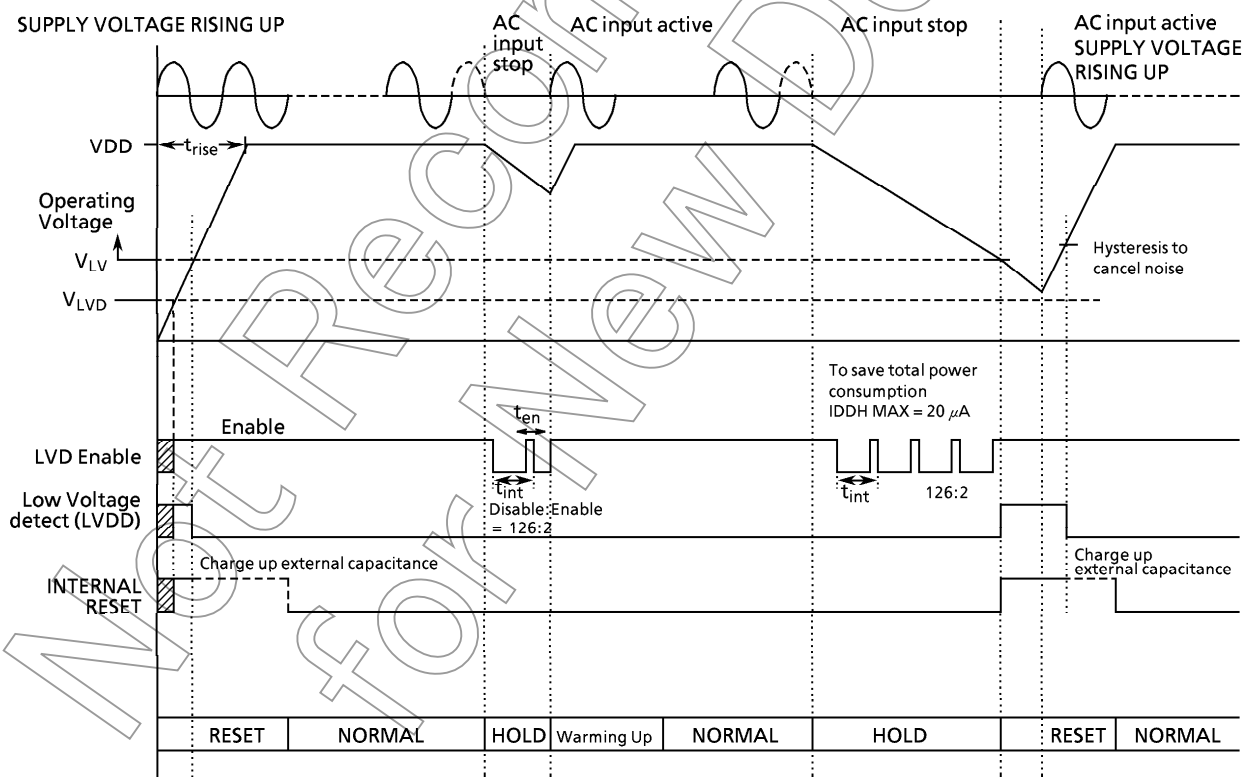


Figure 2-24. Power-Up and Power Save (HOLD mode) Timing Chart

2.9.1 Reset output

R70 port is initially reset output and monitored CPU reset status. When CPU is in reset R70 output is Low level. This output can be also used to reset external peripherals.

By setting RESCTL register(OP0E 0 bit) to "1" , WDT reset signal output is disabled. In the case of LVD reset and setting low level to RESET pin, the reset signal is output in spite of RESCTL status.But the reset signal by WDT is controlled by RESCTL register.

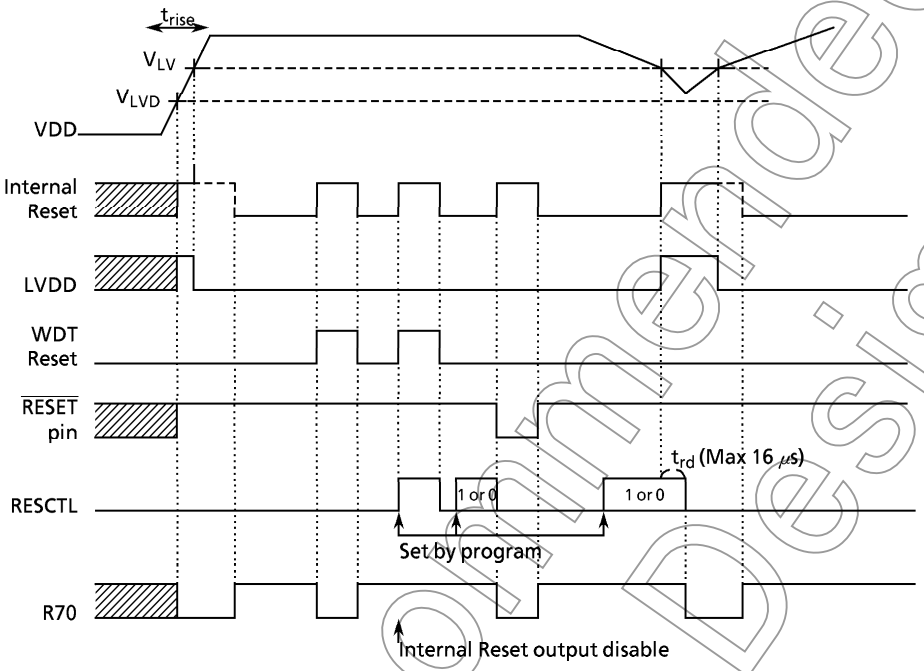


Figure 2-25. RESOUT Timing Chart

2.9.2 Low Voltage Detector (LVD)

The TMP47C206 has on-chip Low Voltage Detector and it is controlled by register.

To save power consumption in the HOLD mode, LVD can be operated intermittently by setting LVDDTY register to "1".

The detection voltage is selectable by setting LVSEL register (OP0E 1 bit) depend on operating frequency. CPU will not be reset by setting LVCTL register (OP0E 3 bit) to "1".

(Port address: OP0E Initial value: 0000)

3	2	1	0
LVCTL	LVDDTY	LVSEL	RESCTL

LVCTL	LVD Reset Control
0:	Reset using LVD
1:	Reset without using LVD

LVDDTY	LVD duty set
0:	Always enable in the HOLD mode
1:	Intermittent operation in the HOLD mode

LVSEL	Detection Voltage Selection
0:	min. 2.7 V (For min. Vpp at fc > 4.2 MHz)
1:	min. 2.2 V (For min. Vpp at fc > 4.2 MHz)

RESCTL	WDT Reset Signal Output Control
0:	Output enable
1:	Output disable

Figure 2-26. RESET/LVD Control Register

3. Peripheral Hardware Function

3.1 Ports

The data transfer with the external circuit and the command / status / data transfer with the internal circuit are performed by using the I/O instructions (13 kinds). There are 4 types of ports:

① I/O port ; Data transfer with external circuit
② Command register ; Control of internal circuit
③ Status register ; Reading the status signal from internal circuit
④ Data register ; Data transfer with internal circuit

These ports are assigned with port addresses (00_H through $1F_H$). Each port is selected by specifying its port address in an I/O instruction. Table 3-2 lists the port address assignments and the I/O instructions that can access the ports.

3.1.1 I/O Timing

(1) Input timing

External data is read from an input port or an I/O port in the S3 state of the second instruction cycle during the input instruction (2-cycle instruction) execution. This timing cannot be recognized from the outside, so that the transient input such as chattering must be processed by program.

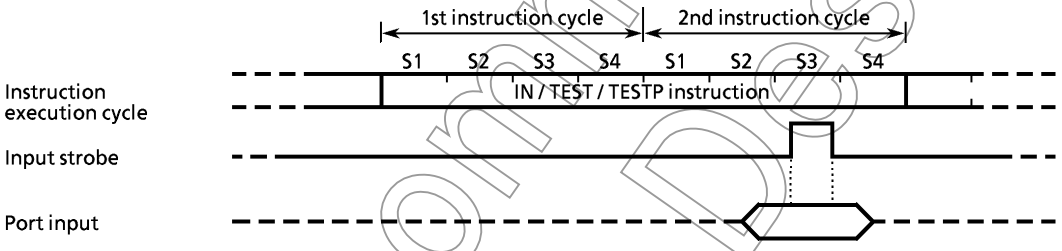


Figure 3-1. Input Timing

(2) Output timing

Data is output to an output port or an I/O port in the S4 state of the second instruction cycle during the output instruction (2-cycle instruction) execution.

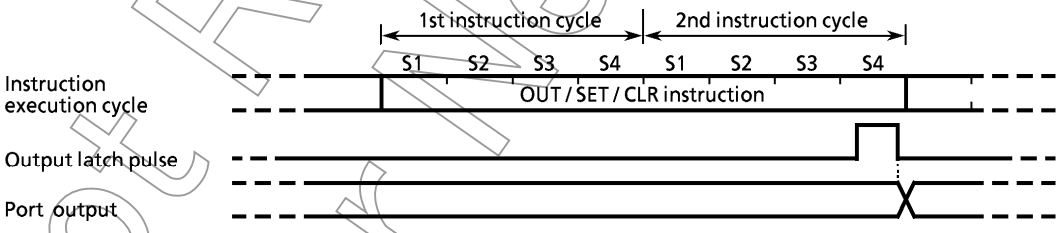


Figure 3-2. Output Timing

3.1.2 I/O Ports

The TMP47C206 have 5 I/O ports (15 pins) each as follows:

① R4, R5 ; 4-bit input / output
② R7 ; 2bit input / output (shared with Reset signal output / pulse output)
③ R8 ; 4-bit input / output (shared with external interrupt input and timer / counter input)
④ KE ; 1-bit sense input (shared with hold request / release signal input)

Each output port contains a latch, which holds the output data. The input ports have no latch; therefore, it is necessary to hold the data externally until it is read or to read it twice or more before processing it.

(1) Port R4 (R43 to R40), R5 (R53 to R50), R7 (R71 to R70)

Ports R4 and R5 are 4-bit I/O port with a latch. When used as an input port, the corresponding latch must be set to "1". The latches are initialized to "1" during reset. R4 and R50 ports can directly drive LEDs.

R51 to 53 port output buffers are Tri-state, and each bit can be controlled independently by the program. Controlling the Tri-state is performed by the command register accessed as port address OP00.
When some bits of the OP00 is 0, the corresponding bit of the output buffers becomes high impedance state.

Port R7 is 2-bits I/O port with latch. R70 pin is shared by the Reset signal output. To use R70 pin for the Reset signal output, the latch should be set to "1". The latch is initialized to "1" during reset. During Reset, R70 port output Reset signal (Low level). Reset by Low Voltage Detection and low level input from RESET pin cannot be controlled by register but WDT reset output can be controlled by setting RSTCTL register (OP0E 0bit). R71 pin is normal I/O pin.

These 3 ports (10 pins) can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions ([SET @L], [CLR @L], and [TEST @L]). Table 3-1 lists the pins (I/O ports) that correspond to the contents of L register.

Example: To clear R43 output as specified by the L register indirect addrressing bit manipulation instruction.

```
LD      L, #0011B       ;  Sets R43 pin address to L register
CLR     @L              ;  R43←0
```

Table 3-1. Relationship between L register contents and I/O port bits

L register 3 2 1 0	PIN
0 0 0 0	R40
0 0 0 1	R41
0 0 1 0	R42
0 0 1 1	R43

L register 3 2 1 0	PIN
0 1 0 0	R50
0 1 0 1	R51
0 1 1 0	R52
0 1 1 1	R53

L register 3 2 1 0	PIN
1 1 0 0	R70
1 1 0 1	R71

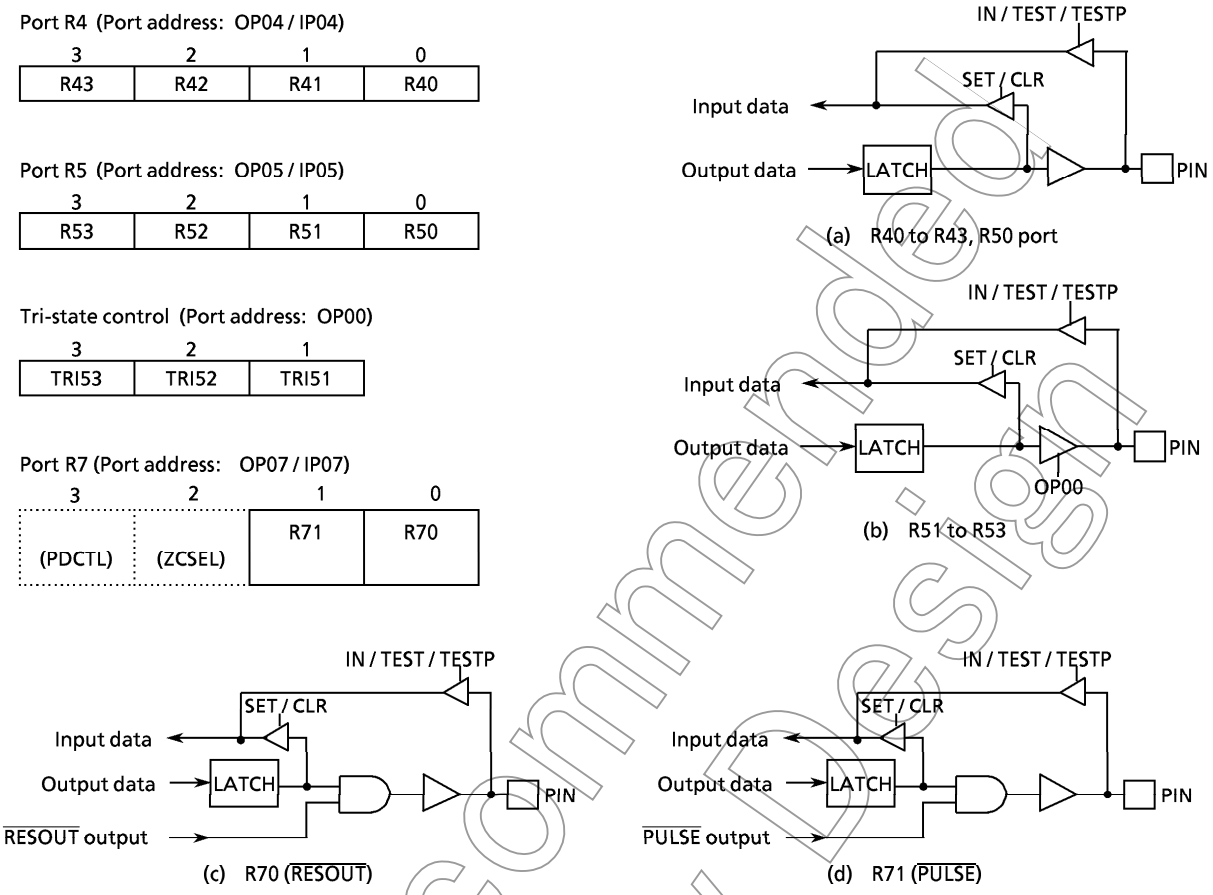


Figure 3-3. Ports R4, R5 and R7

(2) Port R8 (R83 to R80)

Port R8 is a 4-bit I/O port with a latch. When used as an input port, the latch must be set to "1". The latch is initialized to "1" during reset.

Port R8 is shared with the external interrupt input pin and Zero-cross input pin and the timer/counter input pin. To use this port for one of these functional pins, the latch should be set to "1". To use it for an ordinary I/O port, the acceptance of external interrupt should be disabled or the event counter/pulse width measurement modes of the timer/counter should be disabled.

Note: If the interrupt enable master flip-flop is enabled, the interrupt request is always accepted. A dummy interrupt processing must be performed (only the interrupt return instruction [RETI] is executed) when the external pin corresponding to INT1 (R80 or R82) is used as input port.

As for external interrupt 2, interrupt request is not accepted by setting the bit 0 of the interrupt enable register (EIR_0) "0".

When R82 (ZIN) pin is assigned INT1, INT1 occurs upon detection of the rising and falling edge of pin input.

In the case of R80 ($\overline{INT}$), it occurs upon detection of the falling edge.

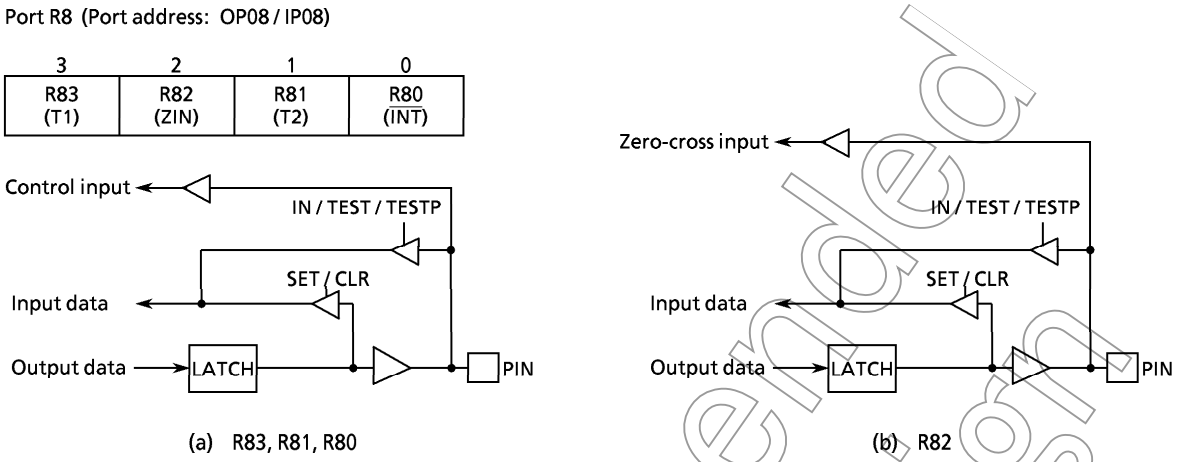


Figure 3-4. Port R8

(3) Port KE ($\overline{KE0}$)

Port KE is a 1-bit sense input port shared with the hold request / release signal input in ($\overline{HOLD}$). This input port is assigned to the least significant bit of Port address IP0E and is processed as the data with inverted polarity. For example, if an input instruction is executed with the pin on the high level, "0" is read. The bit1 through bit3 of port KE, have an undefined value when an input instruction is executed.

Example: To wait until $\overline{KE0}$ pin goes low.

```
SWAIT   :   TEST    %IP0E,0        ; Waits if KE0 pin = "H".
            B       SWAIT
```

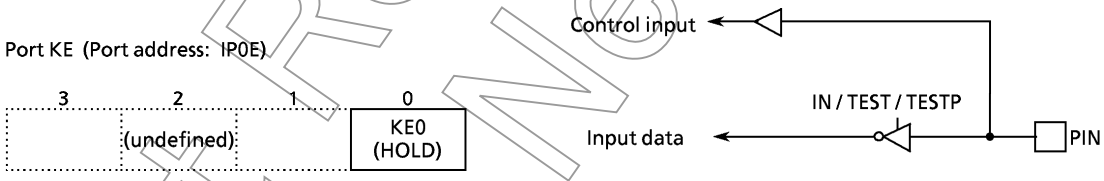


Figure 3-5. Port KE

Note: Please fix $\overline{KE0}$ level to high when R82 (ZIN) is used as HOLD release.

Table 3-2. Port Address assignments and available I/O Instructions

Port address (**)	Port		Input / Output instructions							
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	—	Tri-state (R51 to 53) control	—	○	○	—	—	—	—
01	—	—	—	—	—	—	—	—	—
02	—	—	—	—	—	—	—	—	—
03	—	—	—	—	—	—	—	—	—
04	R4 input port	R4 output port	○	○	○	—	○	○	○
05	R5 input port	R5 output port	○	○	○	—	○	○	○
06	—	—	—	—	—	—	—	—	—
07	R7 input port	R7 output port & R8 control	○	○	○	—	○	○	○
08	R8 input port	R8 output port	○	○	○	—	○	○	○
09	—	—	—	—	—	—	—	—	—
0A	—	—	—	—	—	—	—	—	—
0B	—	—	—	—	—	—	—	—	—
0C	—	—	—	—	—	—	—	—	—
0D	—	—	—	—	—	—	—	—	—
0E	HOLD status	LVD control	○	○	○	—	—	—	—
0F	—	—	—	—	—	—	—	—	—
10_H	Undefined	Hold operating mode control	—	—	—	—	—	—	—
11	Undefined	—	—	—	—	—	—	—	—
12	Undefined	—	—	—	—	—	—	—	—
13	Undefined	—	—	—	—	—	—	—	—
14	Undefined	—	—	—	—	—	—	—	—
15	Undefined	Watchdog timer control	—	—	—	—	—	—	—
16	Undefined	—	—	—	—	—	—	—	—
17	Undefined	Pulse output control	—	—	—	—	—	—	—
18	Undefined	—	—	—	—	—	—	—	—
19	Undefined	Interval Timer interrupt control	—	—	—	—	—	—	—
1A	Undefined	—	—	—	—	—	—	—	—
1B	Undefined	—	—	—	—	—	—	—	—
1C	Undefined	Timer / Counter 1 control	—	—	—	—	—	—	—
1D	Undefined	Timer / Counter 2 control	—	—	—	—	—	—	—
1E	Undefined	—	—	—	—	—	—	—	—
1F	Undefined	—	—	—	—	—	—	—	—

Note: "——" means the reserved state. Unavailable for the user programs.

3.2 Interval Timer Interrupt (ITMR)

The interval timer can be used to generate an interrupt with a fixed frequency. For an interval timer interrupt, one of 4 frequencies can be selected by command. The command register (OP19) is initialized to "0" during reset. An interval timer interrupt is generated at the first rising edge of the binary counters output after the command has been set. The interval timer is not cleared by command, so that the first interrupt may occur earlier than the preset interrupt period.

Example: To set the interval timer interrupt frequency to $fc/2^{15}$ [Hz].

```
LD      A, #0110B    ;  OP19←0110B
OUT     A, %OP19
```

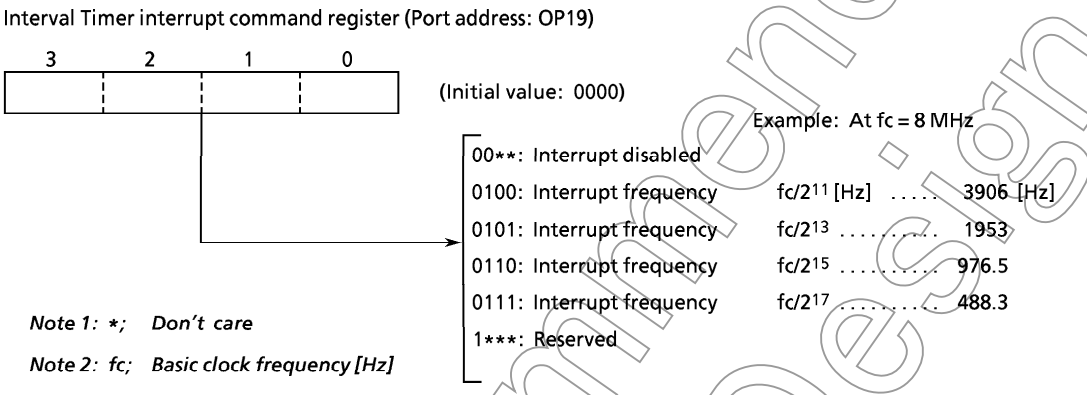


Figure 3-6. Interval Timer Interrupt Command Register

3.3 Timer/Counters (TC1, TC2)

The TMP47C206 contain two 12-bit timer/counters (TC1, TC2). RAM addresses are assigned to the count register in unit of 4 bits, permitting the initial value setting and counter reading through the RAM manipulation instruction. When a timer/counter is not used, the mode selection may be set to "stopped" to use the corresponding RAM addresses for storing the ordinary user-processed data.

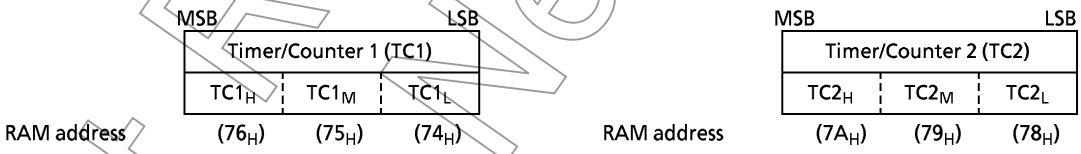


Figure 3-7. The Count registers of the Timer/Counters (TC1, TC2)

3.3.1 Functions of Timer/Counters

The timer/counters provide the following functions:

① Event counter
② Programmable timer
③ Pulse width measurement

3.3.2 Control of Timer/Counters

The timer/counters are controlled by the command registers. The command register is accessed as port address OP1C for TC1 and port address OP1D for TC2. These registers are initialized to "0" during reset.

Timer/Counter 1 control command register (Port address: OP1C)

3	2	1	0	
TC1MS		IPR1		(Initial value: 0000)

TC1MS	Mode selection
00:	Stop
01:	Event counter mode
10:	Timer mode
11:	Pulse width measurement mode

IPR1	Internal pulse rate (interval timer output) selection	
	Example:	At fc = 8 MHz
00:	$fc/2^6$ [Hz]	125000 [Hz]
01:	$fc/2^8$	31250
10:	$fc/2^{10}$	7812.5
11:	$fc/2^{14}$	488.3

Timer/Counter 2 control command register (Port address: OP1D)

3	2	1	0	
TC2MS		IPR2		(Initial value: 0000)

TC2MS	Mode selection
00:	Stop
01:	Event counter mode
10:	Timer mode
11:	Pulse width measurement mode

IPR2	Internal pulse rate (interval timer output) selection	
	Example:	At fc = 8 MHz
00:	$fc/2^{10}$ [Hz]	7812.5 [Hz]
01:	$fc/2^{14}$	488.3
10:	$fc/2^{18}$	30.5
11:	$fc/2^{22}$	1.9

Note: fc; Basic clock frequency [Hz]

Figure 3-8. Timer/Counter Control Command Registers

The timer/counter increments at the rising edge of each count pulse. Counting starts with the first rising edge of the count pulse generated after the command has been set. Count operation is performed in one instruction cycle after the current instruction execution, during which the execution of a next instruction and the acceptance of an interrupt are delayed. If counting is requested by both TC1 and TC2 simultaneously, the request by TC1 is preferred. The request by TC2 is accepted in the next instruction cycle. Therefore, during count operation, the apparent instruction execution speed drops as counting occurs more frequently.

The timer/counter causes an interrupt upon occurrence of an overflow (a transition of the count value from FFF_H to 000_H). If the timer/counter is in the interrupt enabled state and the overflow interrupt is accepted immediately after its occurrence, the interrupt is processed in the sequence shown in Figure 3-9. Note that counting continues if there is a count request after overflow occurrence.

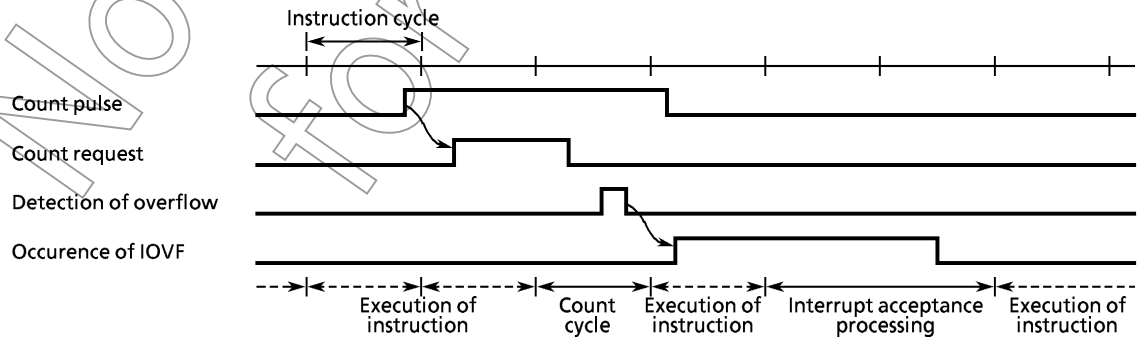


Figure 3-9. Timer/Counter Overflow Interrupt Timing

(1) Event counter mode

In the event counter mode, the timer/counter increments at each rising edge of the external pin (T1, T2) input. The maximum applied frequency of the external pin input is fc/32 for the 1-channel operation; for the 2-channel operation, the frequency is fc/32 for TC1 and fc/40 for TC2. The apparent instruction execution speed drops most to (9/11) × 100 = 82% when TC1 and TC2 are operated at the maximum applied frequency because the count operation is inserted once every 4 instruction cycles for TC1 and every 5 cycles for TC2. For example, the instruction execution speed of 1 μs drops to 1.82 μs.

Example: To operate TC2 in the event counter mode

```
LD      A,  #0100B    ;  OP1D←01**B
OUT     A,  %OP1D
```

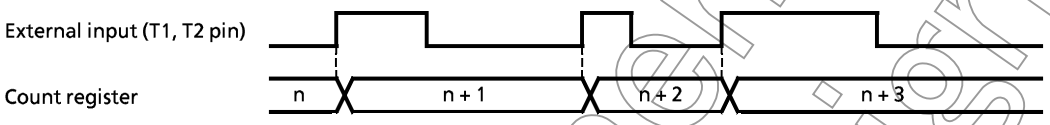


Figure 3-10. Event Counter Mode Timing chart

(2) Timer mode

In the timer mode, the timer/counter increments at the rising edge of the internal pulse generated from the timing generator. One of 4 internal pulse rates can be selected by the command register. The time interval of an overflow interrupt is defined by the following formulation.

$$1 \div \left\{ \frac{fc/8}{\text{(Internal pulse rate)}} - 1 \right\} \times 100 \quad [\%]$$

When an internal pulse rate of $fc/2^{10}$ is used, a count operation is inserted once every 128 instruction cycles, so that the apparent instruction execution speed drops by (1/127) × 100 = 0.8%. For example, the instruction execution speed of 1 μs drops to 1.008 μs.

In the timer mode, R83 (T1) and R81 (T2) pins provide the ordinary I/O ports.

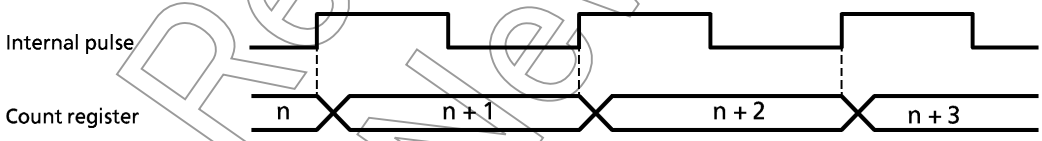


Figure 3-11. Timer Mode Timing chart

Example: To generate an overflow interrupt (at fc = 8 MHz) by the TC1 after 50 ms.

```
LD      HL,  #0F4H    ;  TC1←E79H (setting of the count register)
ST      #9,  @HL+
ST      #7,  @HL+
ST      #0EH,  @HL+
LD      A,  #1000B    ;  OP1C←1000B
OUT     A,  %OP1C
LD      A,  #0100B    ;  EIR←0100B (enables interrupt)
XCH     A,  EIR
EICLR   IL,  110111B  ;  EIF←1, IL3 ←0
```

How to calculate the preset value of the counter register

The preset value of the count register is obtained from the following relation:

2^{12} – (interrupt setting time) × (internal pulse rate)

For example, to generate an overflow interrupt after 50 ms at fc = 8 MHz with the internal pulse rate of $fc/2^{10}$, set the following value to the count register as the preset value:

$2^{12} - (50 \times 10^{-3}) \times (8 \times 10^{6}/2^{10}) = 3705 = E79_H$

Table 3-3. Internal Pulse Rate Selection

Internal pulse rate	Max. setting time	Example: At fc = 8 MHz	
		Internal pulse rate	Max. setting time
fc / 2^6 [Hz]	2^{18}/fc [s]	125000 [Hz]	0.0328 [s]
fc / 2^8	2^{20}/fc	31250	0.13
fc / 2^{10}	2^{22}/fc	9812.5	0.52
fc / 2^{14}	2^{26}/fc	488.3	8.4
fc / 2^{18}	2^{30}/fc	30.5	134
fc / 2^{22}	2^{34}/fc	1.9	2147

(3) Pulse width measurement mode

In the pulse width measurement mode, the timer/counter increments with the pulse obtained by sampling the external pins (T1, T2) by the internal pulse. As shown in Figure 3-12, the timer/counter increments only while the external pin input is high. The maximum applied frequency to the external pin input must be one that is enough for analyzing the count value. Normally, a frequency sufficiently slower than the internal pulse rate setting is applied to the external pin.

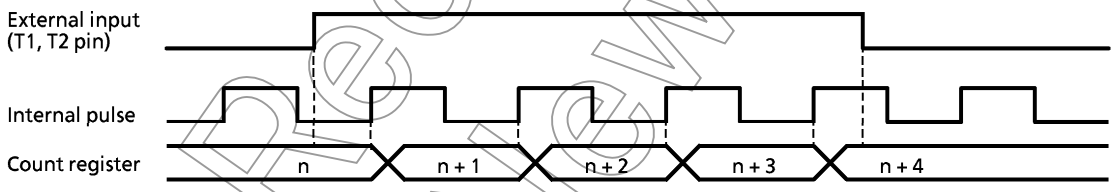


Figure 3-12. Pulse Width Measurement Mode Timing chart

3.4 Watchdog Timer (WDT)

The watchdog timer capability is provided to quickly detect the CPU malfunction such as endless looping caused by noises or the other incident, and restore the CPU to the normal state. The WDT is enabled after reset.

The WDT consists of 10 binary counters, a flip-flop, and a controller. Source input clock of binary counters is $fc/2^{15}$[Hz]. The flip-flop is set to "1" during reset, and cleared to "0" on the rising edge of the binary counter output. The WDT is controlled by the command register (OP15). The command register is initialized to "1000_B" during reset.

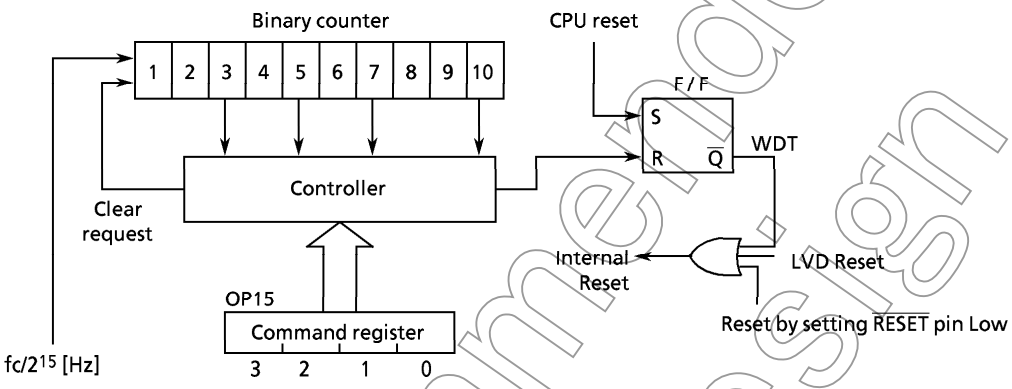


Figure 3-13. Configuration of Watchdog Timer

To detect the CPU malfunction by the WDT:

① Set the WDT detection time, clear the binary counters and Enable the WDT.
② Clear the binary counters within WDT detection time that was set in ①. If a CPU malfunction occurs, preventing the binary counters from being cleared, the flip-flop is cleared to "0" on the rising edge of the binary counter output, making the malfunction detection signal active.

Example: To enable the with detection time of $63 \times 2^{15}/fc$ [s]

```
                LD      A, #0001B     ; OP15 ← 0001B (Set WDT detection time, clear binary
                                                      counters and Enable the WDT)
                OUT     A, %OP15
                :
Within WDT      :
detection timer :
                LD      A, #0001B     ; OP15 ← 0001B (Clear binary counters)
                OUT     A, %OP15
                :
                :
```

Note: It is necessary to clear the binary counter prior to enabling watchdog timer.

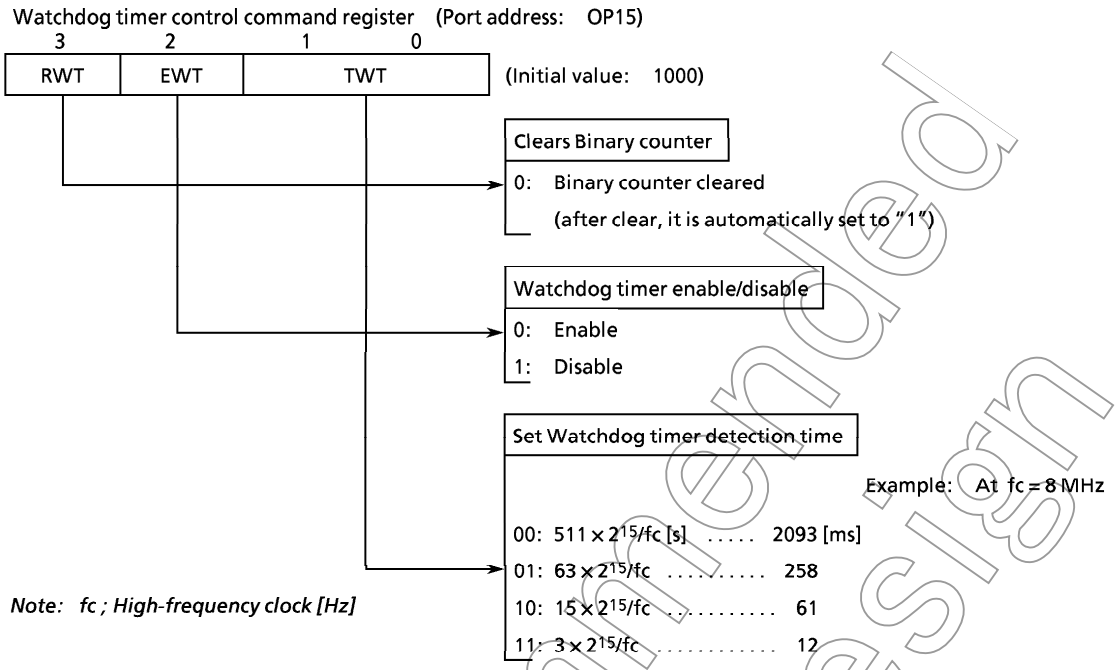


Figure 3-14. Watchdog Timer Control Command Register

3.5 Pulse output

Pulse output is used for buzzer drive and remote control carrier. Pulse output is shared with the R71 pin. Pulse output is asynchronous.

3.5.1 Circuit Configuration

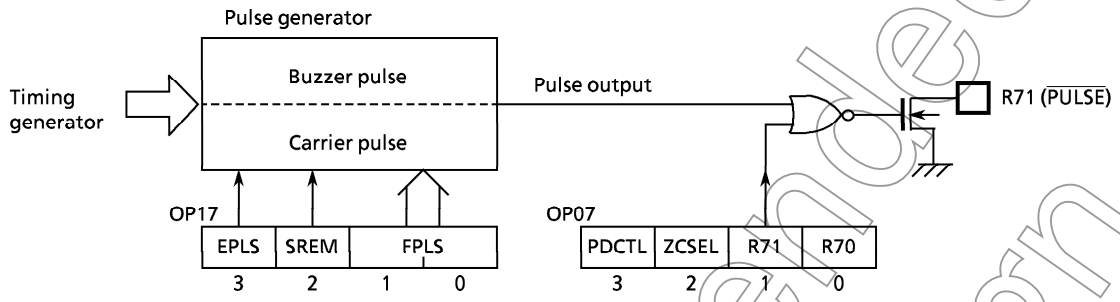


Figure 3-15. Pulse Generator

3.5.2 Control of pulse

The pulse output is controlled by the command register (OP17) and R71 output latch data (bit 1 of OP07). At reset, the OP17 is initialized to "0000_B" and pulse output is disabled. To use the pulse output, instruct start/stop of pulse after pulse output is enabled by the OP17.

Also, pulse output is "L" level (the OP17 is cleared to "0000_B") during the HOLD operating mode. External LED and so on may be destroyed if HOLD operation is executed during output of pulse. Therefore, HOLD operating mode should be execute after pulse is stopped (after R71 output latch set to "1").

Example: Buzzer pulse of 2 kHz is output (fc = 8 MHz)

```
LD      A, #1000B
OUT     A, %OP17  ;   OP17←1000B
  ⋮
CLR     %OP07, 1  ;   Pulse start
  ⋮
SET     %OP07, 1  ;   Pulse stop
```

(Port address: OP17 Initial value: 0000)

3	2	1	0
EPLS	SREM	FPLS	

EPLS	Pulse enable/disable

0: Disable
1: Enable

SREM	Selects output mode

0: Buzzer pulse (1/2 duty)
1: Remote control carrier (1/3 duty)

PFLS	Selects output frequency

00: $fc/2^{12}$, $fc/(2^2 \times 3)$ [Hz]
01: $fc/2^{11}$, $fc/(2^4 \times 3)$
10: $fc/2^{10}$, $fc/(2^5 \times 3)$
11: $fc/2^9$, (Unused)

Buzzer Carrier

Figure 3-16. Pulse Output Control

Table 3-4. Pulse Output Frequency

FPLS	Buzzer pulse		Carrier pulse	
	Pulse rate	at fc = 8 MHz	Pulse rate	frequency
00	$fc / 2^{12}$ [Hz]	1.953 [kHz]	$fc / (2^2 \times 3)$ [Hz]	83.3 [kHz] (fc = 1 MHz)
01	$fc / 2^{11}$	3.906	$fc / (2^4 \times 3)$	37.5 (fc = 1.8 MHz)
10	$fc / 2^{10}$	7.812	$fc / (2^5 \times 3)$	37.5 (fc = 3.6 MHz)
11	$fc / 2^9$	15.625	Don't use	–

(1) Buzzer pulse

The buzzer pulse can be selected one of the four pulse rates by the program. The buzzer pulse is output only when the R71 output latch is "0". "H" level is output when the output latch is "1".

Note: When a piezoelectric buzzer is connected to the pin, voltage may be generated by the buzzer due to thermal or mechanical shock. In such cases, there is danger of the pin being destroyed so a zener diode should be always connected for the protection.

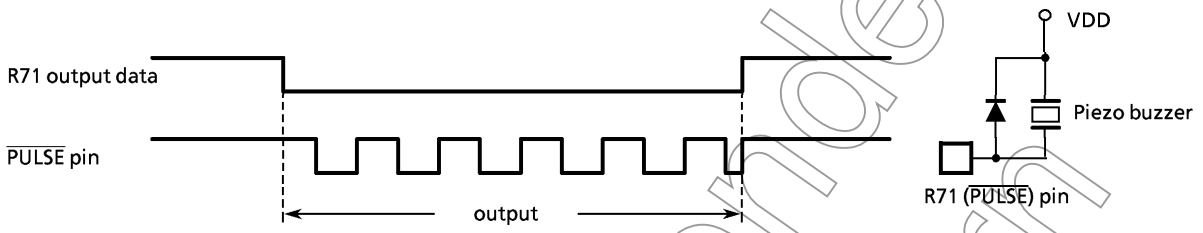


Figure 3-17. Circuit Example of Buzzer Pulse and Timing

(2) Carrier pulse for remote control signal transmitter

The remote control transmitting carrier has a frequency in Table 3-4, which is the basic clock (fc) divided by 12, 48 or 96. Also, the remote control transmitting carrier is output only when the R71 output latch is "0". "H" level is output when the output latch is "1".

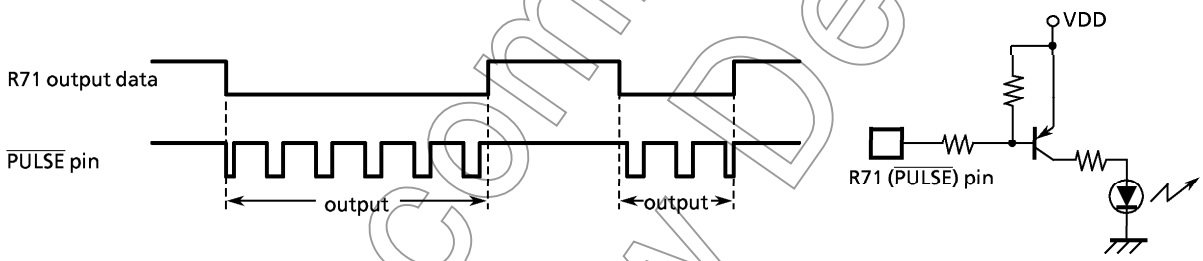


Figure 3-18. Circuit Example of Carrier Pulse and Timing

3.6 Zero-cross detector (ZCD)

R82 pin is used for zero-cross detection input (ZIN) and usually connected to an external resistor in order to reduce the injection current. (Refer to electrical specification) To use the zero-cross detector, the R82 output latch must be set to "1" (it is set to "1" after reset).

This function can be used for commercial power supply frequency input, and time base or triac control. ZIN pin is shared by the external interrupt 1 or 2 selected by ZCSEL register (OP07 2bit). The INT1 and INT2 occurs at the rising and falling edge of the pin input by setting interrupt enable master flip-flop (EIF) to "1".

The device can wake up from HOLD mode by zero-cross input. To avoid erroneous detection of AC due to external cable, it is necessary to fix R82 input level by setting PDCTL OP07 3 bit) to "1".

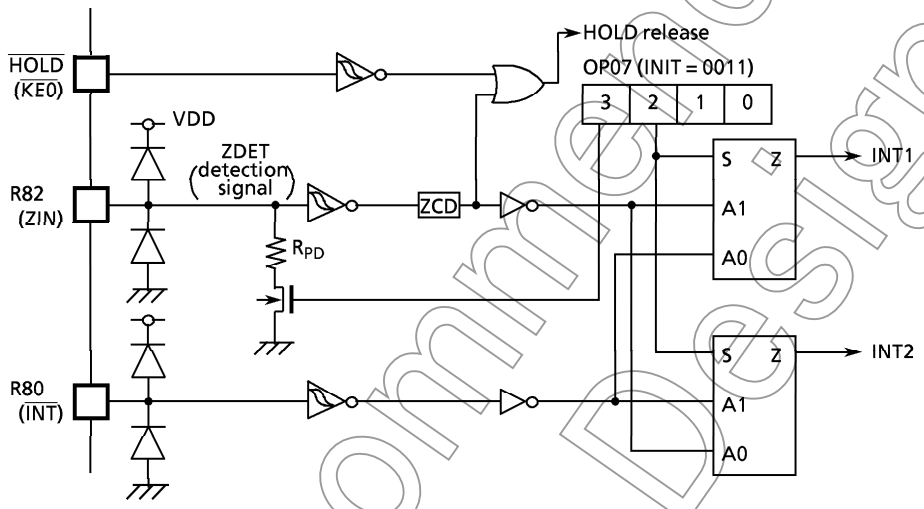


Figure 3-19. Zero-cross Detector

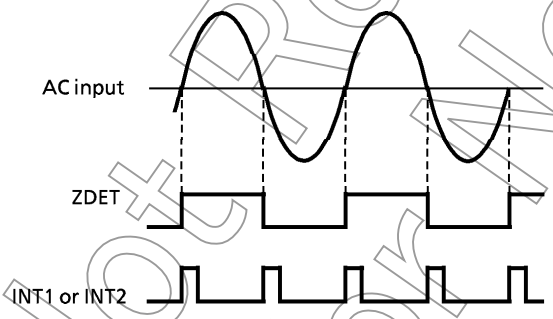


Figure 3-20. Detection Signal

OP07 INIT = 0011

3	2	1	0
PDCTL	ZCSEL	R71	R70

PDCTL: Pull-down resistor control
0: disable
1: enable

ZCSEL: Interrupt selection
0: R82 = INT2 R80 = INT1
1: R82 = INT1 R80 = INT2

Figure 3-21. ZCD control

Note: Please fix $\overline{KE0}$ level to high when R82 (ZIN) is used as HOLD release.

Port Condition by RESET Operation

The transition of Port condition by RESET operation is shown as below.

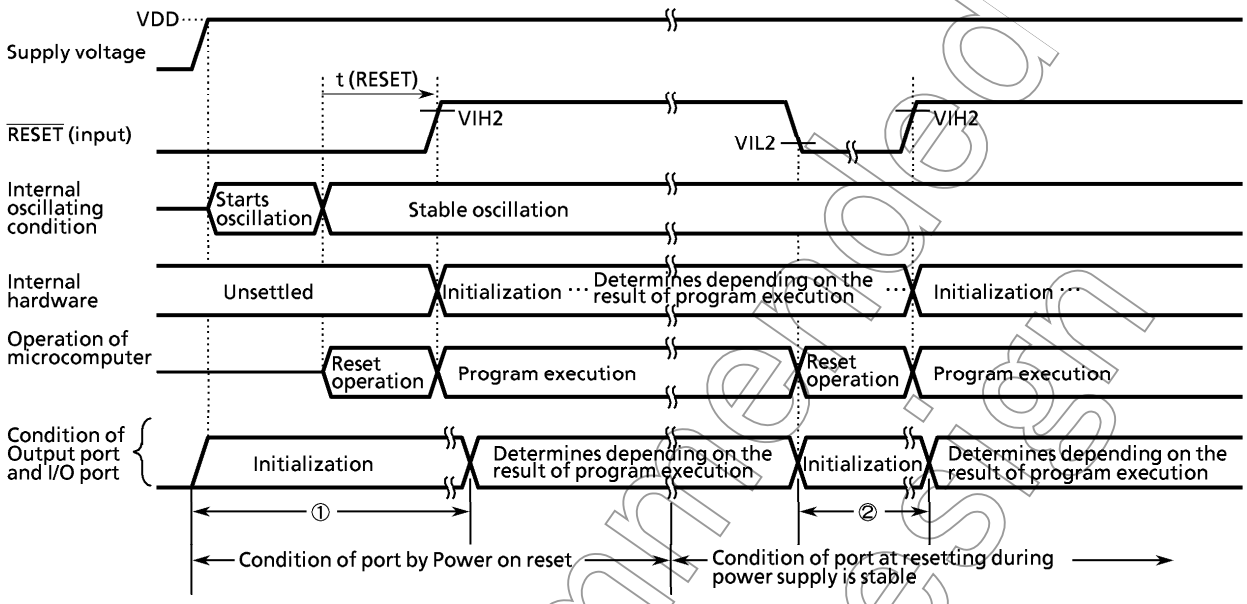


Figure 3-22. Port condition by Reset operation

Note 1: t (RESET) > 24/fc

Note 2: VIL2: Stands for low level input voltage of $\overline{\text{RESET}}$ *pin.*
VIH2: Stands for high level input voltage of $\overline{\text{RESET}}$ *pin.*

Note 3: The term from power on reset to the time program is executed (above ①) and also the term starting from reset operation during power supply is stable to the program is executed (above ②), the port is on the initial condition. The initial condition of Port differs from I/O circuit by each port, refer to the section of "INPUT/OUTPUT CIRCUITRY". Thus, when using Port as an output pin, in the term of the above ① and ②, the voltage level on the signal that connects with the output pin of Port to the input pin of external application circuit should be determined by the external circuitry such as pull-up resistor and / or pull-down resistor.

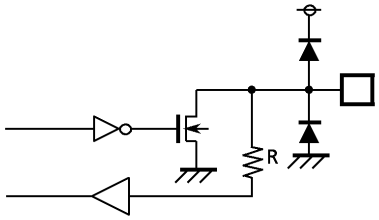
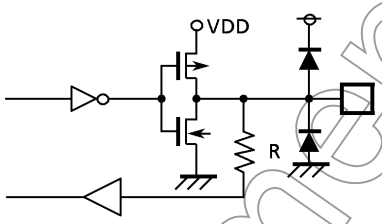
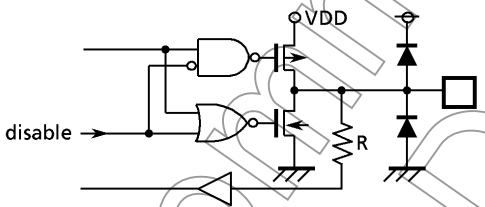
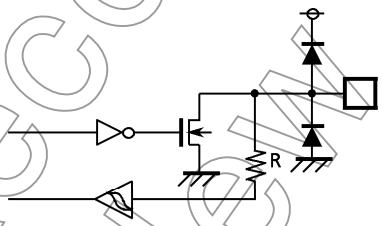
Input / Output Circuitry

The input / output circuity of TMP47C206 I/O port is as follows.

(1) Control pins

Control Pin	I/O	Circuitry and Code	Remarks
XIN XOUT	Input Output	FB: enable, R, R_f, R_O, Ceramic or Crystal, XIN, XOUT FE: enable, R, R_f, R_O, RC, XIN, XOUT	Resonator connecting pins R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_O = 2 kΩ (typ.)
$\overline{RESET}$	Input	VDD, R_{IN}, R	Hysteresis input Pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	R	Hysteresis input R = 1 kΩ (typ.)

(2) I/O ports

Port	I/O	Input / Output Circuitry	Remarks
R4 R70 R71	I/O		Sink open drain output Initial "Hi-Z" R = 1 kΩ (typ.)
R50	I/O		Push-pull output Initial "High" R = 1 kΩ (typ.)
R51 R52 R53	I/O		Tri-state Initial "Hi-Z" R = 1 kΩ (typ.)
R8	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1 kΩ (typ.)

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Port R4, R50	30	V
	I_{OUT2}	Port R51 to R53, R8, R70, R71	3.2	
Output Current (Total)	ΣI_{OUT1}	Port R4, R50	100	mA
	ΣI_{OUT2}	Port R51 to 53, R8, R70, R71	28.8	
Power Dissipation [Topr = 85°C]	PD	SOP	150	mW
		DIP	250	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 40 to 85	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}	Normal mode	Crystar or ceramic	fc = 8 MHz	4.0 (2.7) (Note 2)	5.7	V
				fc = 4.2 MHz	4.0 (2.2) (Note 2)		
			RC	fc = 2.5 MHz	4.0 (2.2) (Note 2)		
		HOLD mode	–	–	4.0 (2.0) (Note 2)		
Input High Voltage	V_{IH1}	Except Hysteresis Input	In the normal operating area		V_{DD} × 0.7	V_{DD}	V
	V_{IH2}	Hysteresis Input			V_{DD} × 0.75		
	V_{IH3}		In the HOLD mode		V_{DD} × 0.9		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	In the normal operating area		0	V_{DD} × 0.3	V
	V_{IL2}	Hysteresis Input				V_{DD} × 0.25	
	V_{IL3}		In the HOLD mode			V_{DD} × 0.1	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7 to 5.7 V		1	8	MHz
			V_{DD} = 2.2 to 5.7 V			4.2	
			V_{DD} = 2.2 to 5.7 V (RC)			2.5	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: LVD id initially enable and initial Min. V_{DD} is 4.0 V. After LVD is disabled above 4.0 V. Min. V_{DD} will be 2.7 or 2.2 to 2.0 V.

DC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1} (Note 1)	$\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.7 V, V_{IN} = 5.7 V / 0 V	–	–	± 2	μA
	I_{IN2}	Open drain output ports					
Input Resistance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Pull down Resistance	R_{PD}	R82		22	70	160	
Input Low Current	I_{IL}	Push-pull output ports	V_{DD} = 5.7 V, V_{IN} = 0.4 V	–	–	– 2	mA
Output Leakage Current	I_{LO}	Open drain output ports	V_{DD} = 5.7 V, V_{OUT} = 5.7 V	–	–	2	μA
Output High Voltage	V_{OH}	Push-pull output ports	V_{DD} = 4.5 V, I_{OH} = – 100 μA	4.8	–	–	V
			V_{DD} = 4.5 V, I_{OH} = – 200 μA	2.4	–	–	
			V_{DD} = 2.2 V, I_{OH} = – 5 μA	2.0	–	–	
Output Low Voltage	V_{OL1}	Port R8, R7, R51 to R53	V_{DD} = 4.5 V, I_{OL} = 3.3 mA	–	–	1.0	V
			V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
			V_{DD} = 2.2 V, I_{OL} = 20 μA	–	–	0.1	
	V_{OL2}	Port R4, R50	V_{DD} = 4.5 V, I_{OL} = 15 mA	–	–	1.0	
			V_{DD} = 4.5 V, I_{OL} = 7 mA	–	–	0.4	
			V_{DD} = 2.2 V, I_{OL} = 50 μA	–	–	0.1	
Output Low Current	I_{OL1}	Port R8, R7, R51 to R53	V_{DD} = 4.5 V, V_{OL} = 0.4 V	1.6	–	–	mA
	I_{OL2}	Port R4, R50	V_{DD} = 4.5 V, V_{OL} = 1.0 V	15	–	–	
			V_{DD} = 4.5 V, V_{OL} = 0.4 V	7	17	–	
Supply Current (in the Normal operating mode) (Note 2)	I_{DD}		V_{DD} = 5.7 V, fc = 8 MHz	–	3	6	mA
			V_{DD} = 5.7 V, fc = 4 MHz	–	2	4	
			V_{DD} = 3.0 V, fc = 4 MHz	–	1	2	
			V_{DD} = 3.0 V, fc = 1 MHz	–	0.6	1.2	
Supply Current (in the HOLD operating mode) (Note 2)	I_{DDH}	LVD always Enable	V_{DD} = 5.7 V	–	50	200	μA
		LVD On and Off	V_{DD} = 5.7 V	–	2.5	20	
Injection Current	I_{ZC}	R82		–	–	1	mA

< General Conditions >

Typ. values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 1: Input Current I_{INT1}: The current through resistor is not included.

Note 2: Supply Current: V_{IN} = 5.5 V / 0.2 V (V_{DD} = 5.7 V) or 2.8 V / 0.2 V (V_{DD} = 3.0 V)

AC Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Instruction Cycle Time	tcy		V_{DD} = 2.7 to 5.7 V	1.0	–	8	μs
			V_{DD} = 2.2 to 5.7 V	1.9			
			RC Oscillation	3.2			
High level Clock pulse Width	t_{WCH}	For external clock operation	$V_{DD} \geqq 2.7$ V	60	–	–	ns
			$V_{DD} < 2.7$ V	120			
Low level Clock pulse Width	t_{WCL}		$V_{DD} \geqq 2.7$ V	60			
			$V_{DD} < 2.7$ V	120			
Delay Reset Output Signal	t_{rd}	fc = 1 MHz		–	–	16	μs

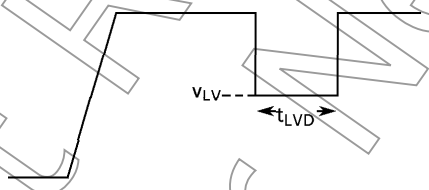
Low Voltage Detector Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter		Symbol	Conditions		Min	Typ.	Max	Unit
LVD internal time	(Note 1)	t_{int}			8.5	–	128	ms
LVD Enable time	(Note 1)	t_{en}			100	–	–	μs
LVD pulse width	(Note 1, 2)	t_{LVD}			50	–	–	μs
Detection Voltage	(Note 3)	V_{LV}	LVDDTY = 0	LVDD = 0	2.7	3.3	3.8	V
			LVDDTY = 1	LVDD = 0	2.2	2.7	3.3	
LVD Operating Voltage	(Note 1)	V_{LVD}			2.0	–	–	V

Note 1: These parameters are characterized but not tested.

Note 2: Less than Min. t_{LVD}, CPU will not be reset.



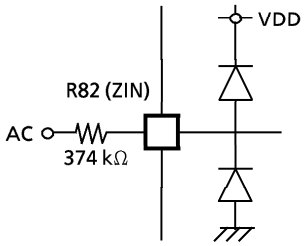
Note 3: Detection voltage has typ. 0.2 V hysteresis (Refer to Figure 2-24)

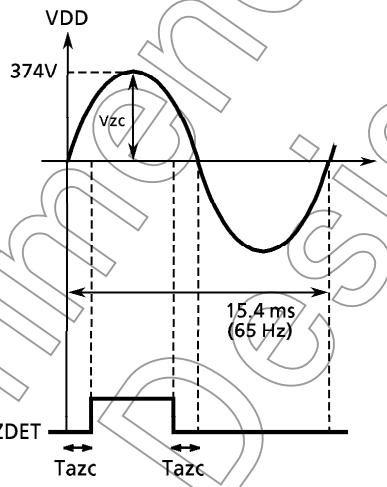
Zero-Cross Detection Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

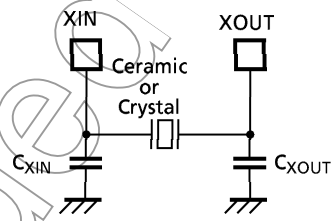
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Zero-cross Accuracy	Tazc	fzc = 45 to 65 Hz	–	–	90	μs
Injection Current	Izc		–	–	1	mA
Pull-down resistance	R_{PD}		22	70	160	kΩ

(*) Measurement conditions





Recommended Oscillating Conditions (V_{SS} = 0 V, V_{DD} = 2.2 to 5.7 V, Topr = – 40 to 85°C)



(1) 8 MHz
Ceramic Resonator

CSA8.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-8.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC8004A4	(NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF

(2) 6 MHz
Ceramic Resonator

CSA6.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-6.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC6004A4	(NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF

(3) 4 MHz
Ceramic Resonator

CSA4.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-4.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC4004A4	(NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF

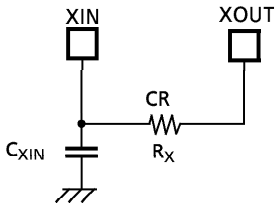
Crystal Oscillator

204B-6F 4.0000	(TOYOCOM)	$C_{XIN} = C_{XOUT}$ = 20 pF

(4) 1 MHz
Ceramic Resonator

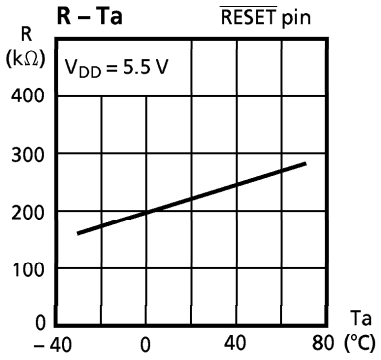
CSA1.00MGU	(MURATA)	$C_{XIN} = C_{XOUT}$ = 30 pF
KBR-1.0MS	(KYOCERA)	$C_{XIN} = C_{XOUT}$ = 30 pF
EFOEC1004A4	(NATIONAL)	$C_{XIN} = C_{XOUT}$ = 30 pF

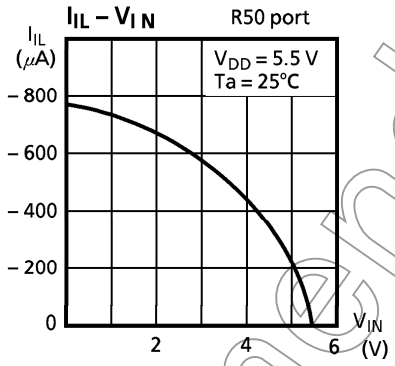
(5) RC Oscillation (V_{SS} = 0 V, V_{DD} = 5.0 V, Topr = 25°C)
2 MHz (Typ.) C_{XIN} = 33 pF, R_X = 10 kΩ

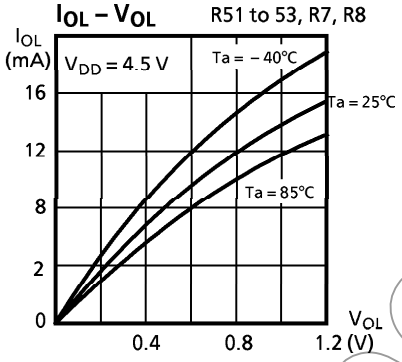


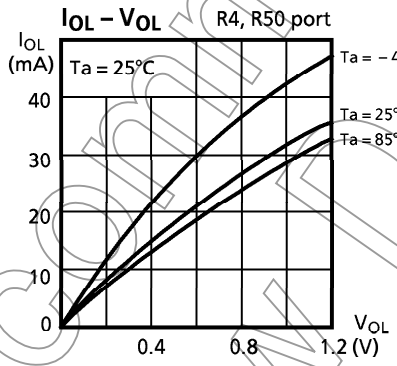
Typical Characteristics

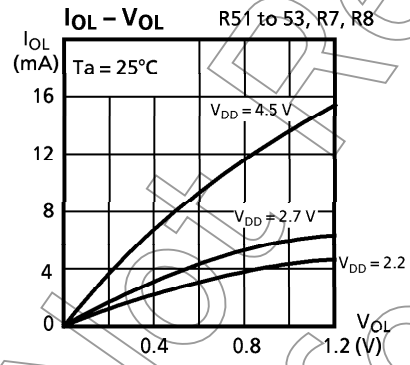
These graphs are for design guidance and not tested or guaranteed.
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of distribution while "max" or "min" represents (mean + 3σ) and (mean – 3σ) respectively were σ is standard deviation.

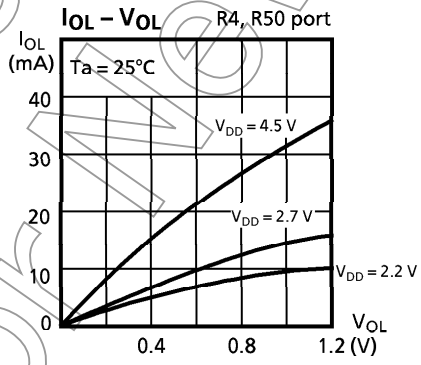




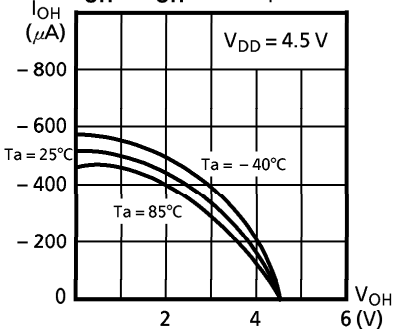




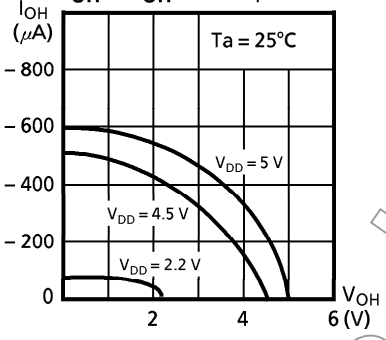




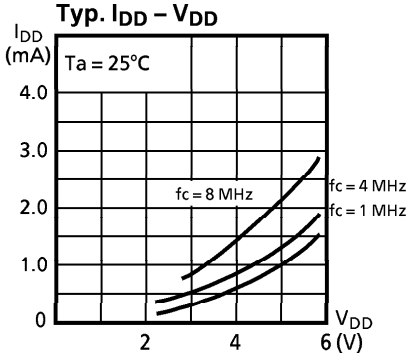
I_{OH} – V_{OH} R5 port



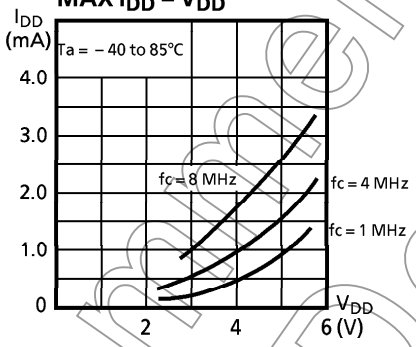
I_{OH} – V_{OH} R5 port



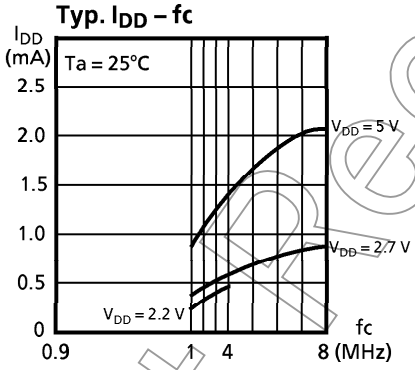
Typ. I_{DD} – V_{DD}



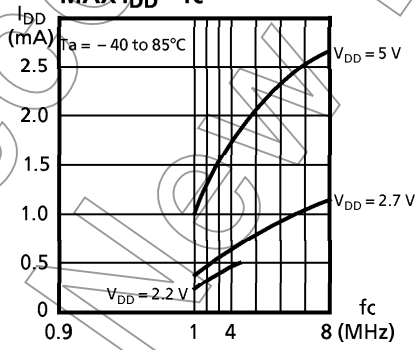
MAX I_{DD} – V_{DD}



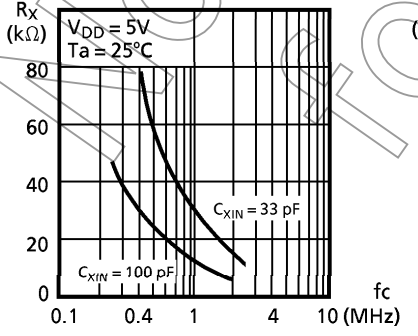
Typ. I_{DD} – fc



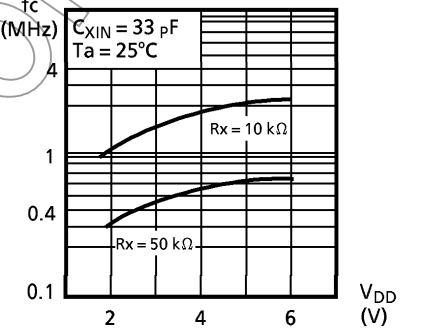
MAX I_{DD} – fc



fc – R_X (RC)



fc – V_{DD} (RC)



Operating area