BURR - BROWN®

VFC101

Synchronized VOLTAGE-TO-FREQUENCY CONVERTER

FEATURES

- FULL-SCALE FREQUENCY SET BY SYSTEM CLOCK
- MULTIPLE INPUT RANGES: 5V, 8V, 10V Full Scale
- ACCURATE 5V REFERENCE VOLTAGE
- LOW NONLINEARITY: 0.02% max at 100kHz FS
- LOW GAIN DRIFT: 40ppm/°C

APPLICATIONS

- INTEGRATING A/D CONVERTER
- MULTICHANNEL DATA ACQUISITION
- FREQUENCY-TO-VOLTAGE CONVERSION
- VOLTAGE ISOLATION

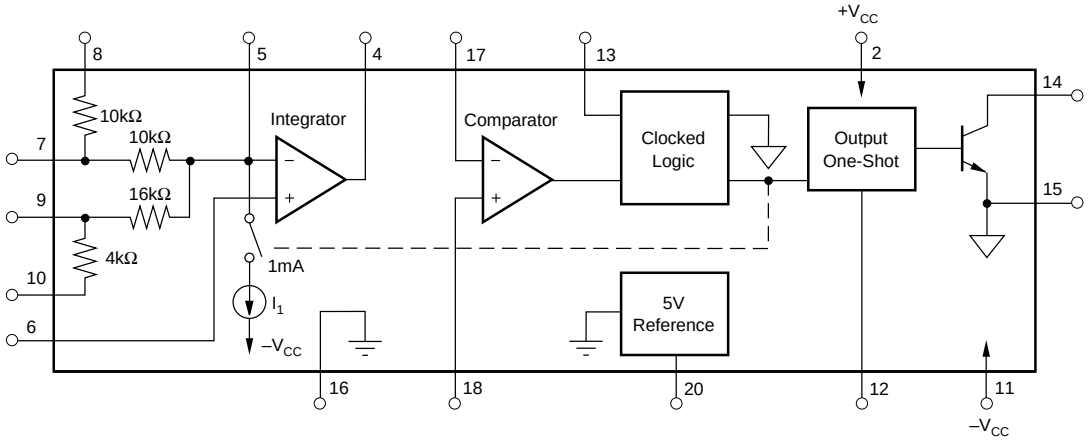
DESCRIPTION

The VFC101 voltage-to-frequency converter uses the proven charge-balance technique with internal digital logic to control the critical reference integration period. Reference timing is derived from an external clock signal which accurately sets the full-scale frequency. This technique eliminates the errors and drift from external timing components which are required with other VFCs.

Internal resistors provide accurate full-scale input ranges of 5V, 8V or 10V inputs without external resistors or trimming. An accurate 5V reference voltage output is useful for bridge or sensor excitation. With simple pin interconnections, it can provide half-scale offset to allow bipolar input voltages.

The open-collector frequency output interfaces easily to CMOS or TTL circuitry. Output one-shot circuitry may be used to optimize the output pulse width for optical couplers or transformers.

The VFC101 is packaged in a surface-mount 20-pin PLCC (plastic leaded chip carrier) package.



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PDS-779B

Printed in U.S.A. October, 1993

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC101JN MIN	VFC101JN TYP	VFC101JN MAX	VFC101KN MIN	VFC101KN TYP	VFC101KN MAX	UNITS
TRANSFER FUNCTION								
Voltage-to-Frequency Mode	$f_{OUT} = f_{CLOCK} (V_{IN}/2V_{FS})$							
Gain Error[1]	FSR[2] = 100kHz		±0.3	±0.5		*	*	% of FSR
Linearity Error	FSR = 100kHz, Over Temperature		±0.01	±0.025		*	±0.02	% of FSR
	FSR = 500kHz, C_{OS} = 60pF		±0.02	±0.05		*	*	% of FSR
	FSR = 1MHz, C_{OS} = 60pF		±0.05	±0.1		*	*	% of FSR
Gain Drift[2]	FSR = 100kHz		±50	±80		±30	±40	ppm of FSR/°C
Referred to Internal V_{REF}			10	±25		*	±15	ppm of FSR/°C
Offset Referred to Input			±1	±3		*	±2	mV
Offset Drift			±12	±100		±6.5	±25	µV/°C
Power Supply Rejection	Full Supply Range			0.02			0.015	%/V
Response Time	To Step Input Change	One Period of New Output Frequency Plus One Clock Period						
Frequency-to-Voltage Mode	$V_{OUT} = 2V_{FS} (f_{IN}/f_{CLOCK})$							
Gain Accuracy[1]	FSR = 100kHz		±0.3	±0.5		*	*	%
Linearity Error	FSR = 100kHz		±0.01	±0.025		*	±0.02	%
Input Resistors								
Resistance			±30			*		%
Temperature Coefficient (T_C)[2]			±50	±100		*	*	ppm°C
INTEGRATOR OP AMP								
V_{OS}[1]			±150	±1000		*	*	µV
V_{OS} Drift			±5	±25		*	±15	µV/°C
I_B			±50	±100		±25	±50	nA
I_{OS}			100	200		50	100	nA
A_{OL}	Z_{LOAD} = 5kΩ/10,000pF	100	120		*	*		dB
CMRR		80	105		*	*		dB
CM Range		–7.5		+0.1	*		*	V
V_{OUT} Range	Z_{LOAD} = 5kΩ/10,000pF	–0.2		+12		*	*	V
Bandwidth			14			*		MHz
COMPARATOR INPUTS								
Input Bias Current (I_S)	$-V_{CC} + 4V < V_{IN} < +V_{CC}$			5			*	µA
CLOCK INPUT (Referenced to Digital Common)								
Frequency (maximum operating)			4			*		MHz
Threshold Voltage			1.4			*		V
	Over Temperature	0.8		2	*		*	V
Voltage Range		$-V_{CC} + 3$		$+V_{CC}$	*		*	V
Input Current			0.5	5		*	*	µA
Rise Time				2			*	µs
OPEN COLLECTOR OUTPUT (Referenced to Digital Common)								
V_{OL}	I_{OUT} = 10mA			0.4			*	V
I_{OL}				15			*	mA
I_{OH} (off leakage)	V_{OUT} = 30V		0.01	10		*	*	µA
Delay Time, Positive Clock								
Edge to Output Pulse			300			*		ns
Fall Time			100			*		ns
Output Capacitance			5			*		pF
OUTPUT ONE-SHOT								
Pulse Width Out	Nominal PW_{OUT} = (5ns/pF) x C_{OS} – 90ns; C_{OS} = 300pF	1	1.4	2	*	*	*	µs
REFERENCE VOLTAGE								
Accuracy	No Load	4.9	5	5.1	4.95	*	5.05	V
Drift[2]			±60	±105		±40	±55	ppm/°C
Current Output (sourcing)		10			*			mA
Power Supply Rejection				0.015			*	%/V
Output Impedance			0.5	2		*	*	Ω
POWER SUPPLY								
Rated Voltage			±15			*		V
Operating Voltage Range	$+V_{CC}$	+7.5		+28.5	*		*	V
	$-V_{CC}$	–7.5		–28.5	*		*	V
Total Supply	$+V_{CC} - (-V_{CC})$	15		36	*		*	V
Digital Common		$-V_{CC} + 2$		$+V_{CC} - 4$	*		*	V
Quiescent Current: $+I_{CC}$	Over Temperature		10.6	15		*	*	mA
$-I_{CC}$			9.6	15		*	*	mA

SPECIFICATIONS (CONT)

ELECTRICAL

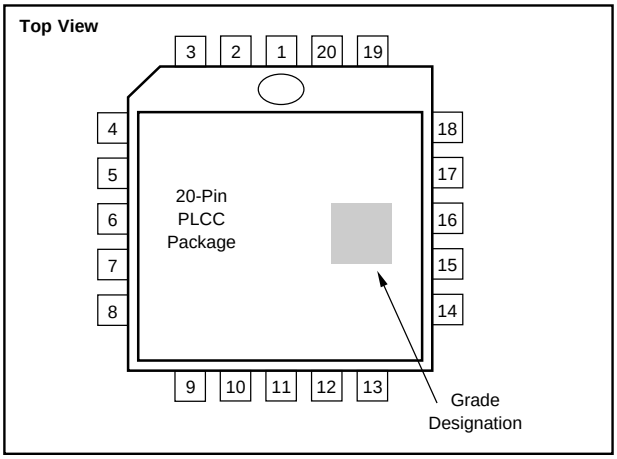
At T_A = +25°C and ±15VDC supplies unless otherwise noted.

PARAMETER	CONDITIONS	VFC101JN			VFC101KN			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification		0		+70	*		*	°C
Storage		–65		+150	*		*	°C
θ_{JA}			90			*		°C/W
θ_{JC}			35			*		°C/W

* Specification same as JN grade.

NOTES: (1) Offset and gain error can be trimmed to zero. (2) Specified by the box method: (max – min) ÷ (Avg x ΔT).

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN #	DESCRIPTION
1	NC
2	$+V_{CC}$ Power Supply
3	NC
4	V_{OUT} Integrator Amp Output
5	C_{INT}, Integrator Inverting Input
6	$+V_{IN}$, Integrator Noninverting Input
7	V_{IN}, 5V FS
8	V_{IN}, 10V FS
9	V_{IN}, 8V FS
10	V_{IN}, 10V FS
11	$–V_{CC}$ Power Supply
12	C_{OS}, Output One-Shot Capacitor
13	f_{CLOCK} Input
14	f_{OUT} Frequency Output
15	Digital Ground
16	Analog Ground
17	– Comparator Input
18	+ Comparator Input
19	NC
20	V_{REF} +5V Reference Output

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($+V_{CC}$ to $–V_{CC}$)	36V
$+V_{CC}$ to Analog Common	28V
$–V_{CC}$ to Analog Common	28V
Integrator Out Short-Circuit to Ground	Indefinite
Integrator Differential Input	±10V
Integrator Common-Mode Input	$–V_{CC}$ +5V to +2V
V_{IN} (pins 7, 8, 9, 10)	$±V_{CC}$
Clock Input	$±V_{CC}$
V_{REF} Out Short-Circuit to Ground	Indefinite
C_{OS} (Pin 12)	0 to $+V_{CC}$
f_{OUT} (referred to digital common)	–0.5V to 36V
Digital Common	$±V_{CC}$
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
VFC101JN	20-Pin PLCC	181
VFC101KN	20-Pin PLCC	181

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

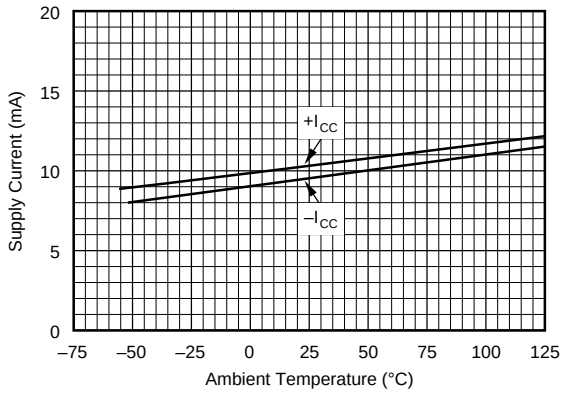
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
VFC101JN	20-Pin PLCC	0°C to +70°C
VFC101KN	20-Pin PLCC	0°C to +70°C

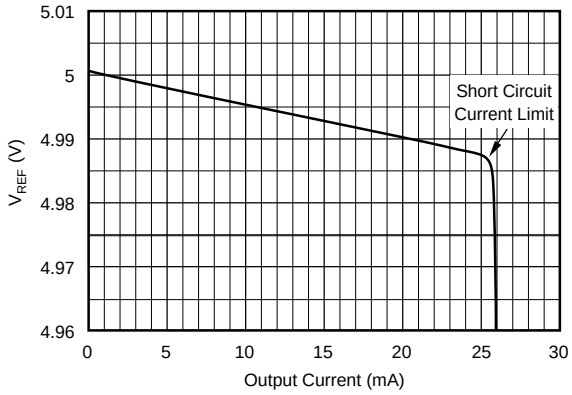
TYPICAL PERFORMANCE CURVES

At +25°C, $\pm V_{CC}$ = 15VDC, and in circuit of Figure 1, unless otherwise specified.

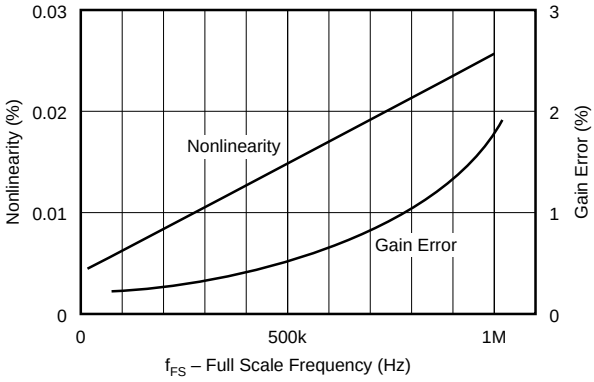
QUIESCENT CURRENT vs TEMPERATURE



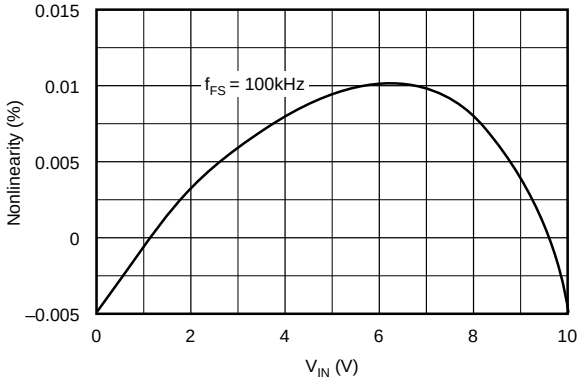
REFERENCE VOLTAGE vs REFERENCE LOAD CURRENT



NONLINEARITY AND GAIN ERROR
vs FULL-SCALE FREQUENCY



NONLINEARITY vs V_{IN}



THEORY OF OPERATION

The VFC101 voltage-to-frequency converter provides digital output pulses with an average frequency proportional to the analog input voltage. The output is an active low pulse of constant duration, with a repetition rate determined by the input voltage. Falling edges of the output pulses are synchronized with rising edges of the clock input.

Operation is similar to a conventional charge-balance VFC. An input operational amplifier (Figure 1) is configured as an integrator so that a positive input voltage causes an input current to flow in C_{INT}. This forces the integrator output to ramp negatively. When the output of the integrator crosses the reference voltage (5V), the comparator trips, activating the clocked logic circuit. Once activated, the clocked logic awaits a falling edge of the clock input, followed by a rising edge. On the rising edge, switch SW_1 is closed for one complete clock cycle, causing the reset current, I_1, to switch to the integrator input. Since I_1 is larger than the input current, I_{IN}, the output of the integrator ramps positively during the one clock cycle reset period. The clocked logic circuitry also generates a VFC output pulse during the reset period.

Unlike conventional VFC circuits, the VFC101 accurately derives its reset period from an external clock frequency. This eliminates the critical timing capacitor required by other VFC circuits. One period (from rising edge to rising edge) of the clock input determines the integrator reset period.

When the negative-going integration of the input signal crosses the comparator threshold, integration of the input signal will continue until the reset period can start (awaiting the necessary transitions of the clock). Output pulses are thus made to align with rising edges of the external clock. This causes the instantaneous output frequency to be a subharmonic of the clock frequency. The average frequency, however, will be an accurate analog of the input voltage.

A full-scale input causes a nominal output frequency equal to one-half the clock frequency. The transfer function is $f_{OUT} = (V_{IN}/2V_{FS})\ f_{CLOCK}$.

Input voltages greater than V_{FS} cause the output frequency to limit at half the clock frequency. Negative inputs cause all output pulses to cease. The full-scale input voltage, V_{FS}, is determined by the input pin used—see Figure 1.

One of the useful functions made possible by the VFC101's multiple input resistors is shown in Figure 2. By connecting one 10V input to the 5V V_{REF} output, the other 10V input pin functions as a bipolar input. A –5V to +5V input range causes a zero to $f_{CLOCK}/2$ output frequency range. Accurate ratio matching and temperature tracking of the input resistors provides improved stability of the half-scale offset.

INPUT Pin Number	FULL-SCALE VOLTAGE V_{RS}
8	10V
10	10V
9	8V
7	5V
7(1)	2.5V

NOTE: (1) Pin 8 connected to pin 5.

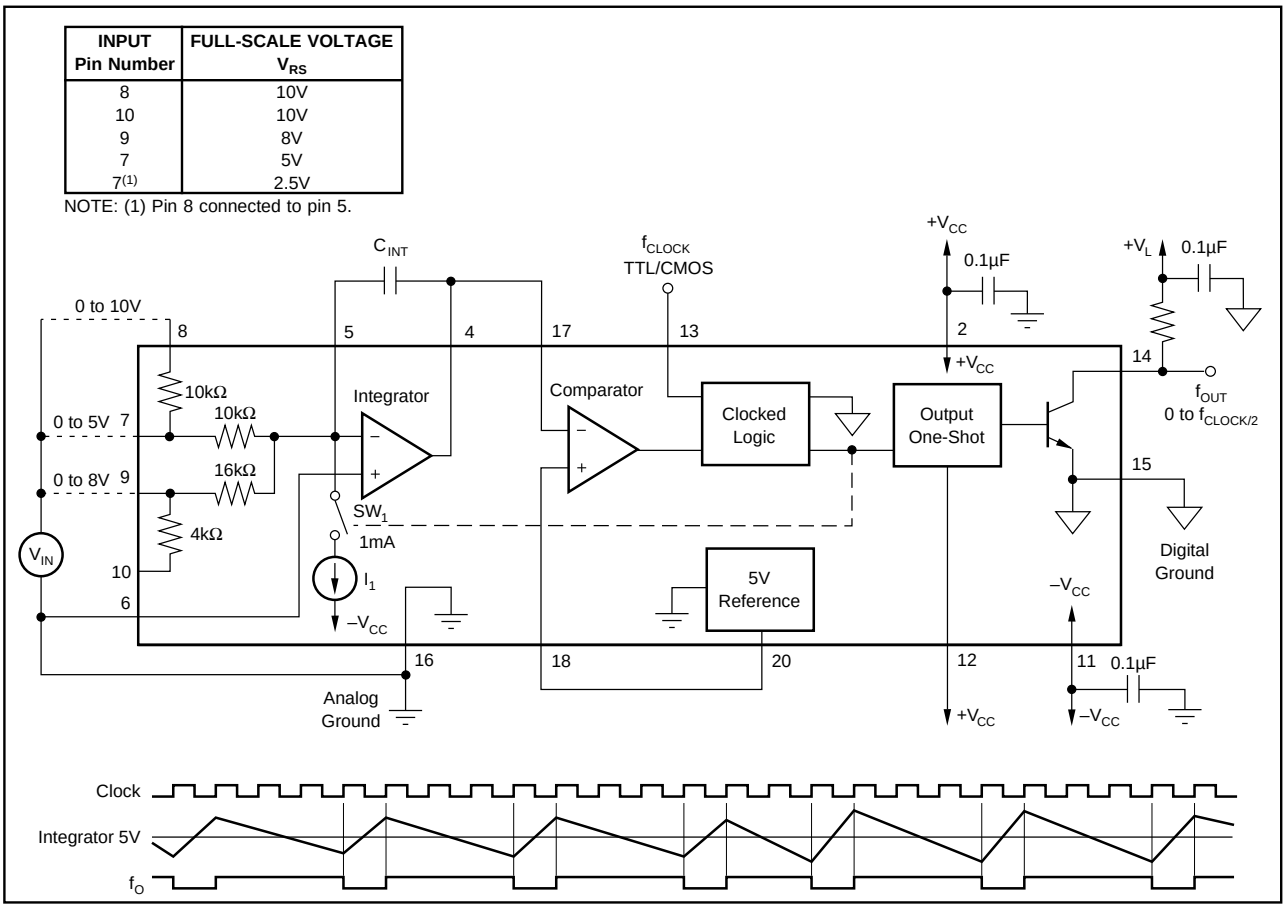


FIGURE 1. Basic Voltage-to-Frequency Operations.

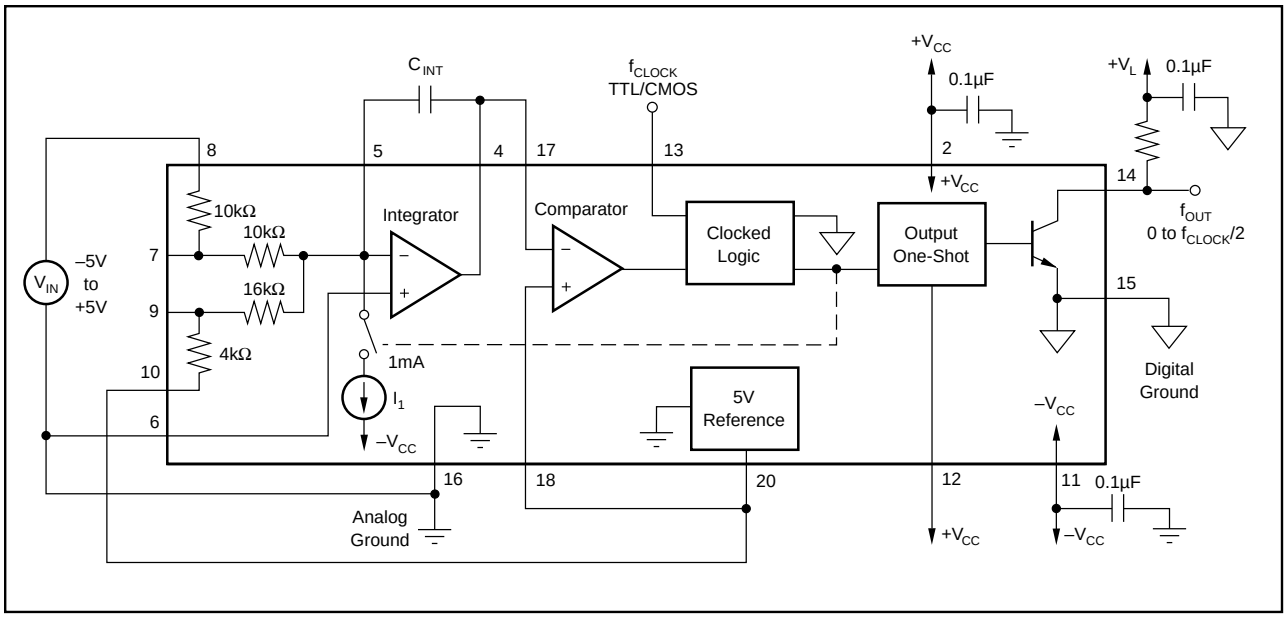


FIGURE 2. Offset for Bipolar Input Voltages.

INSTALLATION AND OPERATING INSTRUCTIONS

The integrator capacitor C_{INT} (see Figure 1) affects the magnitude of the integrator voltage waveform. Its absolute accuracy is not critical since it does not affect the transfer function. Figure 3 facilitates choosing an appropriate standard value to assure that the integrator waveform voltage is within acceptable limits. Good dielectric absorption properties are required to achieve best linearity. Mylar™, polycarbonate, mica, polystyrene, Teflon™ and glass types are appropriate choices. Choice will depend on the particular value and size. Ceramic capacitors vary considerably from type to type and some produce significant nonlinearities. Polarized capacitors should not be used.

Deviation from the nominal recommended +1V to –0.75V integrator voltage (as controlled by the integrator capacitor value) is permissible and will have a negligible effect on VFC operation. It may be desirable to deviate from the suggested value. Smaller integrator voltages, for instance, allow more "headroom" for averaging noisy input signals. The VFC is a fully integrating input converter, able to reject large levels of interfering noise. This ability is limited only by the output voltage swing range of the integrator amplifier. By setting a small integrator voltage swing using a large C_{INT} value, larger levels of noise can be integrated without integrator output saturation and loss of accuracy.

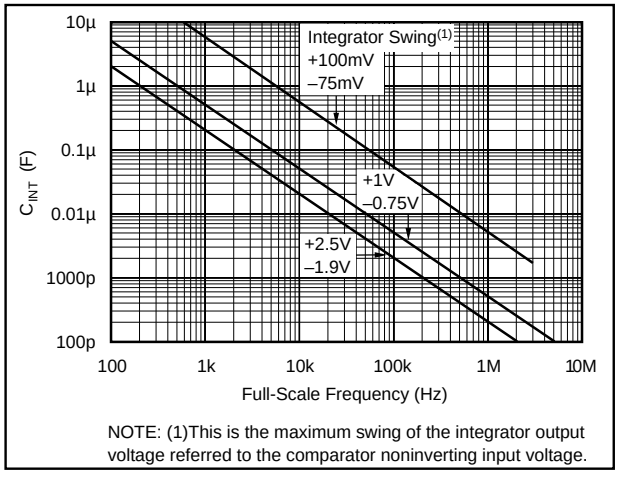


FIGURE 3. Integrator Capacitor Selection Graph.

The maximum integrator voltage swing requirement is nearly symmetrical about the comparator threshold voltage (see Figure 5.) One-third greater swing is required above the threshold than below it. Maximum demand on positive integrator swing occurs at low scale, while the negative swing is greatest just below full scale.

CLOCK INPUT

The clock input is TTL- and CMOS-compatible. Its input threshold is approximately 1.4V (two diode voltage drops) referenced to digital ground (pin 15). The clock "high" input may be standard TLL or may be as high as $+V_{CC}$. The clock input has a high input impedance, so no special drivers are required. Rise time in the transition region from 0.5V to 2V must be less than 2µs for proper operation.

OUTPUT

The frequency output is an open collector current-sink transistor. Output pulses are active-low during the reset integration period (see "Shortened Output Pulses".)

Interface to a logic circuit normally uses a pull-up resistor to the logic power supply. Selection of the pull-up resistor should be made such that no more than 15mA flows in the output transistor. The actual choice of the pull-up resistor may depend on the full-scale frequency and the stray capaci-

Mylar™, Teflon™ E. I. du Pont de Nemours & Co.

tance on the output line. The rising edge of an output pulse is determined by the RC time constant of the pull-up resistor and the stray capacitance.

The synchronized nature of the VFC101 makes viewing its output on an oscilloscope somewhat tricky. Since all output pulses align with the clock, it is best to trigger and view the clock on one of the input channels and the output can then be viewed on another oscilloscope channel. Depending on the VFC input voltage, the output waveform may appear as if the oscilloscope is not properly triggered. The output might best be visualized by imagining a constant output frequency which is locked to a submultiple of the clock frequency with occasional extra pulses or missing pulses to create the necessary average frequency. It is these extra or missing pulses that make the output waveform appear as if the oscilloscope is not properly triggered. This behavior amounts to a frequency or phase jitter in the output, making frequency detection with most phase-locked loop circuitry impractical. For the same reason, fast period measurement (ratiometric counting) will not provide a stable reading. The output frequency must be measured (averaged) for N counts of f_{CLOCK} to achieve a stable N counts of resolution.

SHORTENED OUTPUT PULSES

With pin 12 connected to $+V_{CC}$, the negative output pulse duration is equal to one period of the clock input. Shorter output pulses may be useful in driving optical couplers or transformers for voltage isolation or noise rejection. This can be accomplished by connecting capacitor C_{OS} as shown in Figure 4. Output pulses cannot be made to exceed one clock period in duration. Thus, a C_{OS} value which would create an output pulse which is longer than one period of the clock will have the same effect as disabling the one-shot, causing the output pulse to last one clock period. The minimum practical pulse width of the one-shot circuit is approximately 100ns. Using C_{OS} to generate shorter output pulses does not affect the output frequency or the gain equation.

REFERENCE VOLTAGE

Low gain drift is achieved with a precision internal 5V reference. This reference is brought to an external pin and can be used for a variety of purposes. It is used to offset the noninverting comparator input in voltage-to-frequency mode (although a precise voltage is not required for this function). It is very useful in many other applications such as offsetting the input to accept bipolar input signals. It can source up to 10mA and sink 100µA. Heavy loading of the reference will change the gain of the VFC. A 10mA load interacting with a 0.5Ω typical output impedance will change the VFC gain equation and reference voltage by 0.1%.

LINEARITY PERFORMANCE

The linearity of the VFC100 is specified as the worst-case deviation from a straight line defined by low scale and high scale end point measurements. This worst-case deviation is expressed as a percentage of the 10V full-scale input. All units are tested.

Linearity performance and gain error change with full-scale operating frequency as shown in the typical performance curves. Integrator voltage swing (determined by C_{INT}) has a minor effect on linearity. A small integrator voltage swing typically leads to best linearity performance.

The best linearity performance at high full-scale frequencies (above 500kHz) is obtained by using short output pulses

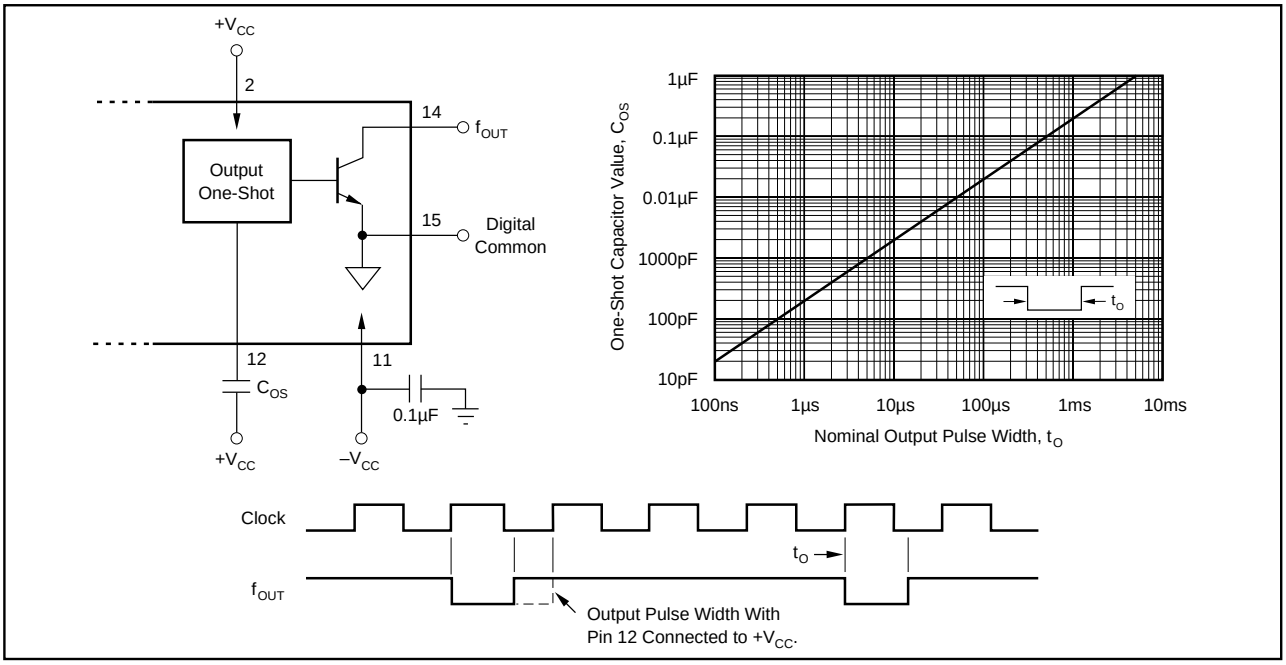


FIGURE 4. Circuit and Timing Diagram for Shortened Output Pulses.

with a one-shot capacitor of 60pF. As with any high-frequency circuit, careful attention to good power supply bypassing techniques (see "Power Supplies and Grounding") is also required.

TEMPERATURE DRIFT

Conventional VFC circuits are affected significantly by external component temperature drift. Drift of the external input resistor and timing capacitor required with these devices may easily exceed the specified drift of the VFC itself.

When used with its internal input resistor, the gain drift of the complete VFC101 circuit is totally determined by the performance of the VFC101. Gain drift is specified at a full-scale output frequency of 100kHz. Gain drift remains excellent at higher operating frequency, typically remaining within specifications at f_{FS} = 1MHz.

Drift of the external clock frequency directly affects the output frequency, but by using a common clock for the VFC and counting circuitry, this drift can be cancelled.

POWER SUPPLIES AND GROUNDING

Separate analog and digital grounds are provided on the VFC101 and it is important to separate these grounds to attain greatest accuracy. Logic sink current flowing in the f_{OUT} pin is returned to the digital ground. If this "noisy" current were allowed to flow in analog ground, errors could be created. Although analog and digital grounds may eventually be connected together at a common point in the circuitry, separate circuit connections to this common point can reduce the error voltages created by varying currents flowing through the ground return impedance. The +5V V_{REF} pin is referenced to analog ground.

The power supplies should be well bypassed using capacitors with low impedance at high frequency. A value of 0.1µF is adequate for most circuit layouts.

The VFC101 is specified for a nominal supply voltage of ±15V. Supply voltages ranging from ±7.5V to ±18V may be used. Either supply can be up to 28V as long as the total of both does not exceed 36V. Steps must be taken, however, to assure that the integrator output does not exceed its linear range. Although the integrator output is capable of 12V output swing with 15V power supplies, with 7.5V supplies, output swing will be limited to approximately 4.5V. In this case, the comparator input cannot be offset by directly connecting to the 5V reference output pin. The comparator input must be connected to a lower voltage point (approximately 2V.) This allows the integrator output to operate around a lower voltage point, assuring linear operation. This threshold voltage does not affect the accuracy or drift of the VFC as long as it is not noisy. It should not be made too small, however, or the negative output limitation of the integrator (–0.2V) may cause saturation. Also, a large integrator capacitor may be used to limit the required integrator waveform swing to approximately 100mV (see Figure 3.)

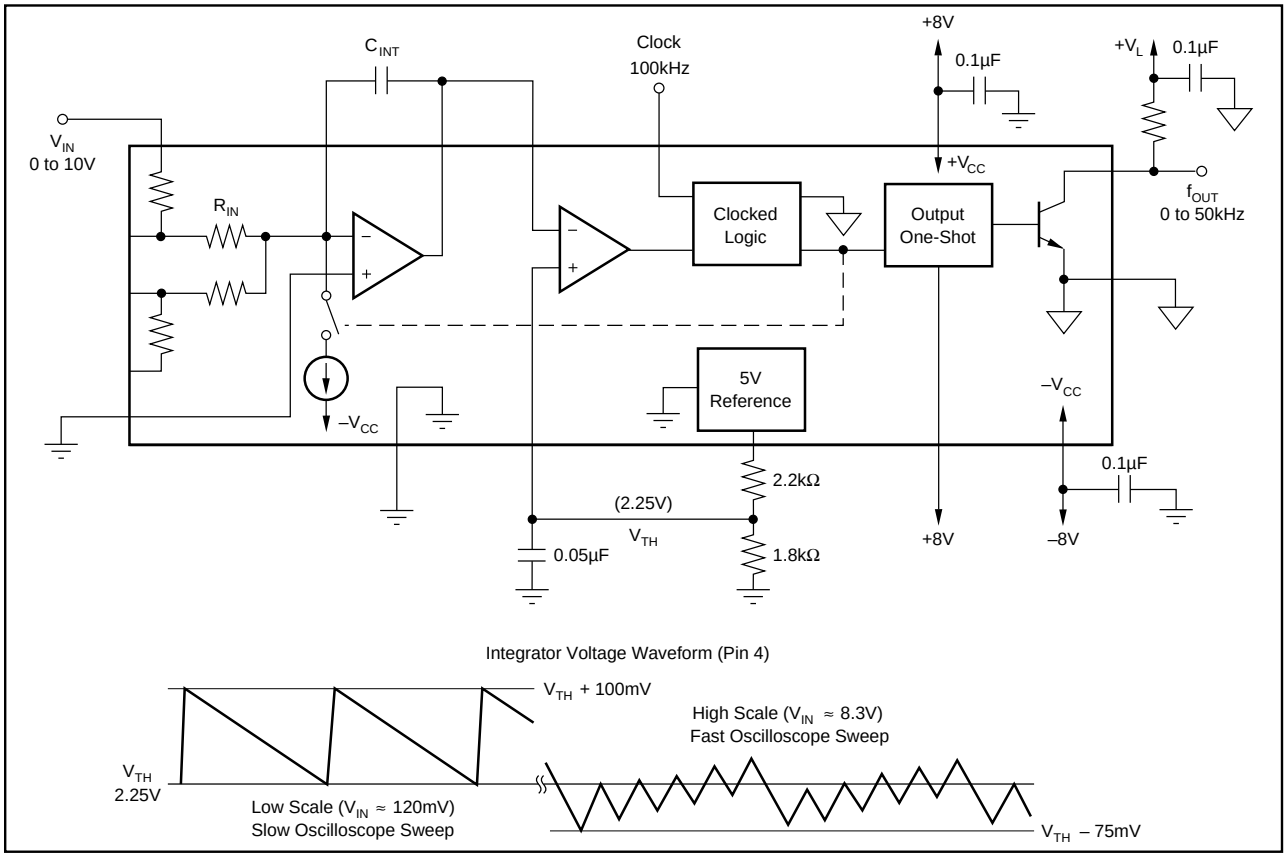


FIGURE 5. Circuit Diagram and Integrator Voltage Waveform for Low Power Supply Voltage Operation.

The circuit in Figure 5 operates from the minimum power supplies, avoiding saturation of the integrator amplifier and loss of accuracy. C_{INT} is chosen for a +100mV to –75mV integrator voltage swing (referred to the noninverting comparator input). The offset voltage applied to the comparator's noninverting input is derived from a resistive voltage divider from V_{REF}.

The relationship of the allowable operating voltage ranges on important pins is shown in Figure 6. Note that the integrator amplifier output cannot swing more than 0.2V below ground. Although this is not "normal" for an operational amplifier, a special design of this type optimizes high-frequency performance. It is this characteristic which requires offsetting the noninverting comparator input in voltage-to-frequency mode.

FREQUENCY-TO-VOLTAGE MODE

The VFC100 can also function as a frequency-to-voltage converter by supplying an input frequency to the comparator input as shown in Figure 7. The input resistor, R_{IN}, is connected as a feedback resistor. The voltage at the integrator amp output is proportional to the ratio of the input frequency to the clock frequency. The transfer function is:

$$V_{OUT} = (f_{OUT}/f_{CLOCK})\ 20V.$$

This transfer function is complementary to the voltage-to-frequency mode transfer function, making voltage-to-frequency-to-voltage conversions simple and accurate.

Direct coupling of the input frequency to the comparator is easily accomplished by driving both comparators with complementary frequency input signals. Alternatively, one of the comparator inputs can be biased at half the logic voltage (using V_{REF} and a voltage divider) and the other input driven directly.

The proper timing of the input frequency waveform is shown in Figure 7. The input pulse should go low for one clock cycle, centered around a falling edge of the clock. The minimum acceptable input pulse width must fall no later than 200ns before a negative clock edge and rise no sooner than 200ns after the falling clock edge. An input pulse which remains low for more than one falling edge of the clock will produce incorrect output voltages. Positive (active high) input pulses can be accepted by reversing the connections to pins 14 and 15.

The integrator amplifier output is designed to drive up to 10,000pF and 5kΩ loads in frequency-to-voltage mode. This allows driving long lines in a large system.

Ripple voltage in the voltage output is unavoidable and is inversely proportional to the value of the integrator capacitor. Figure 8 shows the output ripple and settling time as a function of the C_{INT} value.

The ripple frequency is equal to the input frequency. Its magnitude can be reduced by using a large integrator capacitor value, but with the tradeoff of slow settling time in response to an input frequency change. The settling time constant is equal to $R_{IN} \times C_{INT}$. A better compromise between output ripple and settling time can be achieved by using a moderately low integrator capacitor value and adding a low-pass filter on the analog output. The cutoff frequency of the filter should be made below the lowest expected input frequency to the frequency-to-voltage converter.

NOTE: Several useful applications circuits may be found in the VFC100 product data sheet. These require only minor adaptation to the different pinout and input resistor configurations of the VFC101.

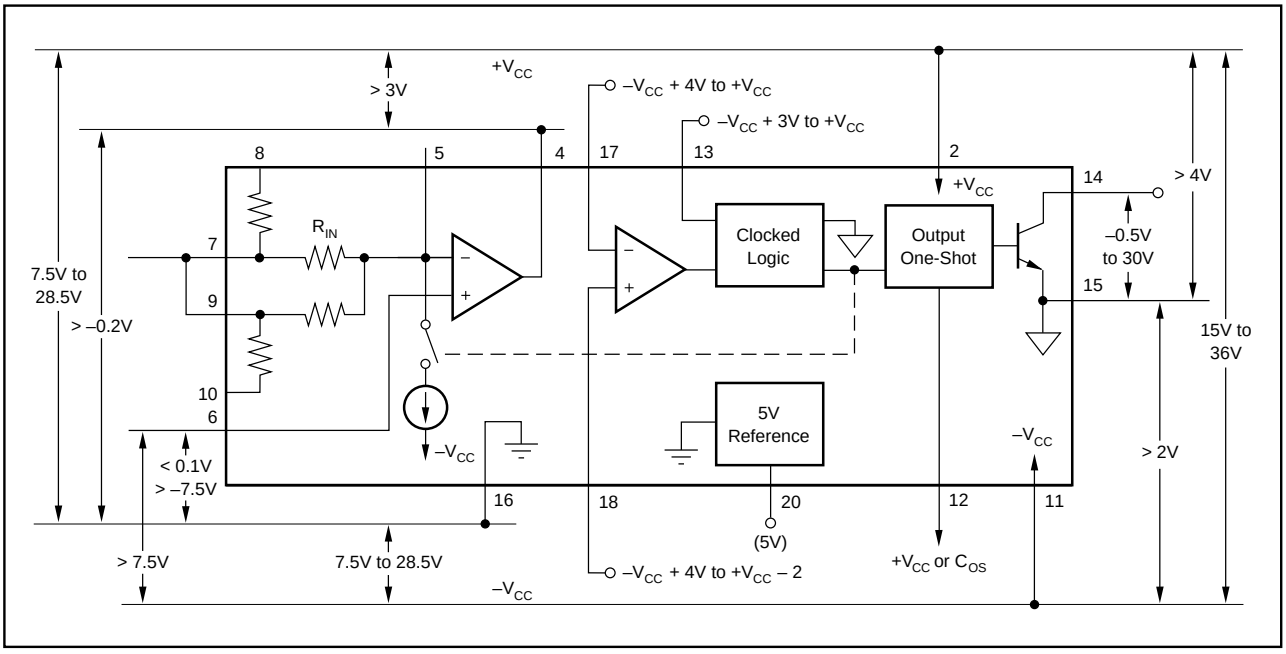


FIGURE 6. Relationships of Allowable Voltages.

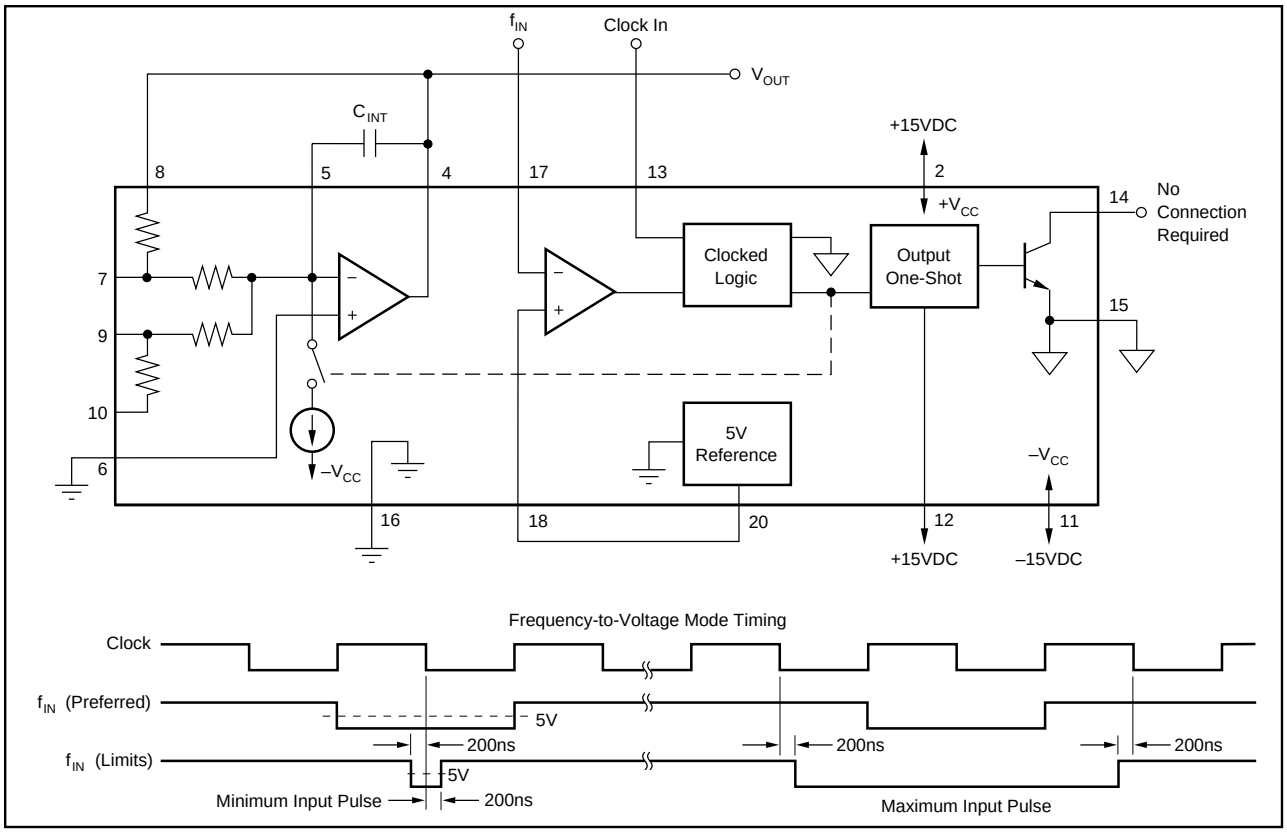


FIGURE 7. Circuit and Timing Diagram of a Frequency-to-Voltage Converter.

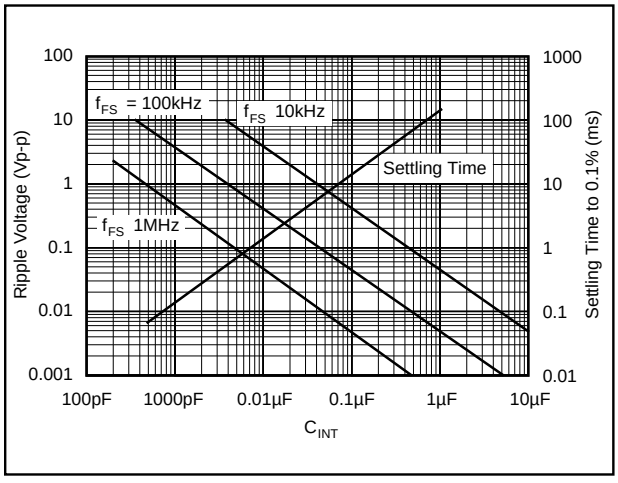


FIGURE 8. Frequency-to-Voltage Mode Output Ripple and Settling Time vs Integrator Capacitance.