TOSHIBA TC9400F/N

TENTATIVE

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9400F, TC9400N

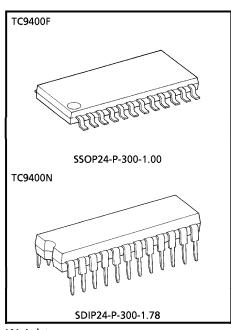
Σ - Δ MODULATION SYSTEM DA CONVERTER WITH A BUILT-IN 8-TIMES OVER SAMPLING DIGITAL FILTER/DIGITAL ATTENUATOR

The TC9400F and TC9400N are a 2'nd order Σ - Δ modulation system 1-bit DA converter incorporating an 8-times oversampling FIR type digital filter and digital attenuator developed for digital audio equipment. Because the IC is small package (SSOP24, SDIP24) and the de-emphasis filter has been incorporation, it is possible to

constitute reducing the size and cost of the DA converter.

FEATURES

- Built-in 8-times over sampling FIR type digital filter
- DA converter over sampling ratio (OSR): 192 fs
- Built-in digital de-emphasis filter
- In serial control mode, output amplitude can be set in 128 steps of resolution using microcontroller commands
- In parallel control mode, soft mute can be set for the output signal in 128 steps in 20 ms
- Simultaneous outputs Left and Right channel
- Sampling frequency: 44.1 kHz, 32 kHz, 48 kHz
- Support double speed operation
- Built-in digital zero detection output circuit
- Characteristics of the digital filter and DA converter are as follows :



Weight

SSOP24-P-300-1.00 : 0.31 g (Typ.) SDIP24-P-300-1.78 : 1.2 g (Typ.)

Digital filter

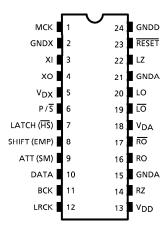
	DIGITAL FILTER	PASS-BAND RIPPLE	TRANSIENT BAND WIDTH	STOP-BAND SUPPRESSION
Standard Operation	8 fs	± 0.15 dB	20 k~24.1 kHz	– 40 dB
Double Speed Operation	8 fs	± 0.15 dB	20 k~24.1 kHz	– 40 dB

DA converter $(V_{DD} = 5 V)$

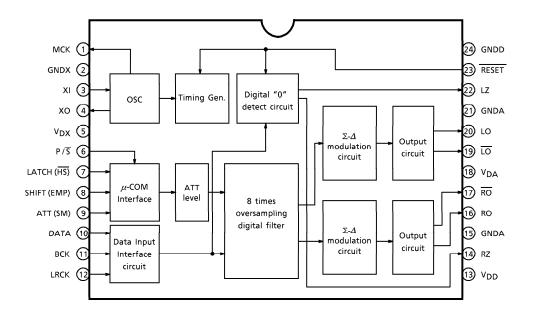
	OSR	NOISE DISTORTION	S/N RATIO	
Standard Operation	192 fs	– 90 dB (Typ.)	100 dB (Typ.)	
Double Speed Operation	192 fs	– 87 dB (Typ.)	98 dB (Typ.)	

• 2 kinds of package, Pin 24 flat package and Pin 24 DIP shrunk package.

PIN CONNECTION

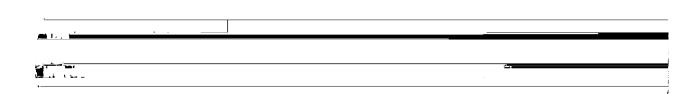


BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	1/0	FUNCTION & OPERATION	REMARKS
1	MCK	0	System clock output pin	
2	GNDX	_	Crystal oscillator GND pin	
3	ΧI	I	Crystal oscillator connecting pins.	
4	хо	0	Generate the clock required by the system.	
5	V _{DX}	-	Crystal oscillator power supply pin	
6	P/S	ı	Parallel/serial mode select pin	Shumitt input Pull-up resister
7	LATCH (HS)	I	Serial mode : Data latch signal input pin Parallel mode : Standard / Double speed operation control pin	Shumitt input Pull-up resister
8	SHIFT (EMP)	1	Serial mode : Shift clock input pin Parallel mode : De-emphasis filter ON/OFF control pin	Shumitt input Pull-up resister
9	ATT (SM)	1	Serial mode : Data input pin Parallel mode : Soft mute control pin	Shumitt input Pull-up resister
10	DATA	I	Audio data input pin	Shumitt input
11	ВСК	I	Bit clock input pin	Shumitt Input
1.7	IRCY		LR clock input ain	Shumitt input



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERI	STIC	SYMBOL	RATING	UNIT		
		V_{DD}	-0.3~6.0			
Power Supply Vol-	tage	V_{DA}	-0.3~6.0	V		
		V_{DX}	-0.3~6.0	1		
Input Voltage		Vin	-0.3~V _{DD} + 0.3	V		
Power Dissipation	TC9400F	PD	200	mW		
Power Dissipation	TC9400N	ן אט	300	11100		
Operating Temper	ature	T _{opr}	- 35~85	°C		
Storage Temperat	ure	T _{stg}	- 55∼150	°C		

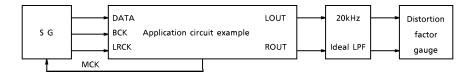
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta = 25° C V_{DD} = V_{DX} = V_{DA} = 5 V) DC CHARACTERISTICS

CHARACT	CHARACTERISTIC		TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
		V_{DD}			4.5	5.0	5.5	
Power Supply Voltage		V_{DX}	—	Ta = −35~85°C	4.5	5.0	5.5	V
		V_{DA}				5.0	5.5	
Power Dissipation		I _{DD}	_	XI = 16.9 MHz	_	30	40	mA
Input Voltage	"H" Level	VIH			$V_{DD} \times 0.7$	_	V_{DD}	V
Imput voitage	"L" Level	V _{IL}	_		0	_	$V_{DD} \times 0.3$	•
Input Current	"H" Level	lіН			- 10		10	
Input Current	"L" Level				- 10	_	10	μ A

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN	TYP.	MAX	UNIT
Noise Distortion	THD + N	1	1 kHz Sine wave, full-scale input	_	- 90	- 80	dB
S/N Ratio	S/N	1		90	100	_	dB
Dynamic Range	DR	1	1 kHz Sine wave, – 60 Input conversion	90	95	_	dB
Cross-talk	СТ	1	1 kHz Sine wave, full-scale input	_	- 95	- 90	dB
Operating Frequency	f _{opr}	_		12	16.9344	18.5	MHz
Input Fraguency	fLR		LRCK duty cycle = 50%	30	44.1	100	kHz
Input Frequency	fBCK	_	BCK duty cycle = 50%	1.0	2.1168	6.2	MHz
Rise Time	t _r		LDCK DCK (10, 000/)	_	_	15	nS
Fall Time	t _f] -	LRCK, BCK (10~90%)	_	_	15	nS
Delay Time	t _d	—	BCK LEdge → LRCK, DATA	- 50	_	50	nS

• TEST CIRCUIT-1: With the use of a sample application circuit

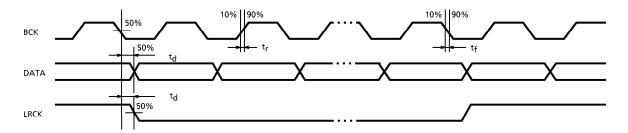


SG : ANRITSU : MG-22A or equivalent LPF : SHIBASOKU : 725C internal filter DISTORTION : SHIBASOKU : 725C or equivalent

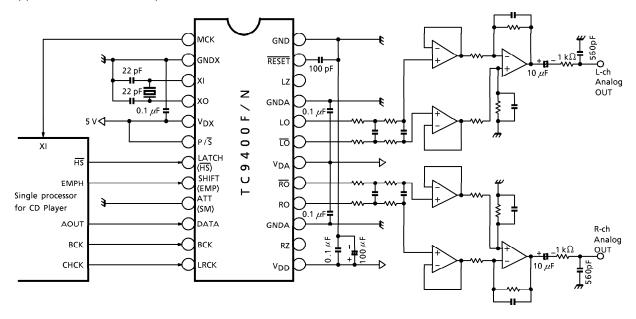
MEASURING ITEM	DISTORTION FACTOR GAUGE FILTER SETTING A WEIGHT
THD + N, CT	OFF
S/N, DR	ON

A weight: IEC-A or equivalent

• AC CHARACTERISTICS STIPULATED POINT : (Input signal stipulation : LRCK, BCK, DATA)

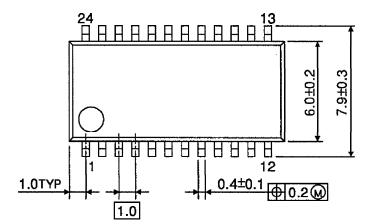


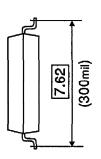
Application Circuit Example

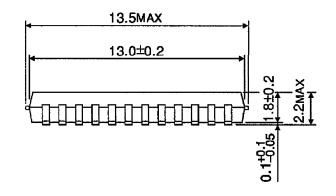


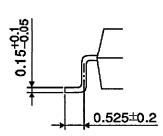
Unit: mm

PACKAGE DIMENSIONS SSOP24-P-300-1.00







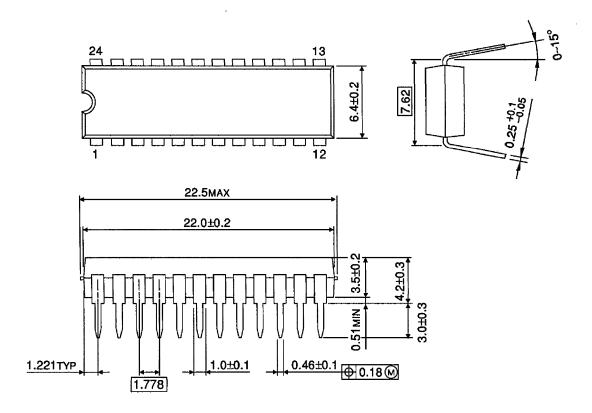


Weight: 0.31 g (Typ.)

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PACKAGE DIMENSIONS SDIP24-P-300-1.78

Unit: mm



Weight: 1.2 g (Typ.)

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